A new Auxiliary Converter Topology with SiC Components for Railway Applications

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A new Auxiliary Converter Topology with SiC Components for Railway Applications

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Abstract

Smaller size and lower weight are always the targets of the power electronic product development. This work introduces two new topologies of auxiliary converters which have the feature of fewer components and fewer number of energy conversion stages comparing with the conventional auxiliary converter used in railway applications.

The initial proposal of the proposed new topology is based on the idea which converts the high frequency current pulses into low frequency AC voltages without rectification stages. This thesis starts with theoretical analysis of the initial ideas with the conclusion of two versions of new topology converter proposal: inductive link auxiliary converter and resonant link auxiliary converter. The modulation method strategy for both of those two versions of auxiliary converters are developed within this thesis, the equations for dimensioning the passive components are also given. Simulation shows that the output voltage waveform has very low THD (Less than 3%).The output waveform is similar to a multilevel converter with 'infinite' number of levels.

The inductive link auxiliary converter is able to deliver power with unsymmetrical load due there is no energy stored in the inductive link circuit between two adjacent current pulses. The semiconductor switches have to turn off at high current peaks which introduce high switching losses. To solve this issue the resonant link auxiliary converter is proposed. Due to the added resonant capacitor the resonant link converter is able to store energy in the resonant link circuit between two adjacent current pulses which reduce the total numbers of hard turn off in the semiconductor switches which will reduce the switching losses. On the other hand the resonant link auxiliary converter suffers with output voltage distortion with unsymmetrical load.

In order to verify the theory which is developed by the theoretical analysis step, prototypes are designed and tested for the inductive link auxiliary converter. A scaled down version prototype is designed to develop the

control software and validate the idea of generating low frequency AC voltage from high frequency current pulses. A three phase 80 kW inductive link auxiliary converter is designed and tested. The measured waveforms agree with the simulation model. The measured THD is less than 1% at all measured output power range. The measured efficiency on the complete system is 86% at 50kW output power.

Acknowledgements

First of all, I would like to thank my supervisor Dr. Hans Bängtsson for all the help he provided during this period and for his trust and encouragement. His suggestions, guidance, advice and comments have been of major importance for me.

I would like to thank Professor Mats Alaküla for accepting me as a Ph.D. student and his encouragements during this period.

I would like also to thank all my colleagues at IEA LTH, Lund University for all the interesting discussions. Special thanks to Getachew Darge for helping me out in the lab. I am also grateful to Dr. Per Karlsson for answering all my power electronics related questions. I wish to express my sincere gratitude to my office mate Conny Högmark for the friendly atmosphere he created and the interesting discussions.

I also would like to thank Tommy Lundberg and Ulf Baly at Bombardier Transportation AB for their kind support during the prototype development. I am also grateful to Tommy Andersson at Infineon for the support of component samples.

Finally, I want to dedicate this thesis to my wife Sijia and to my parents.

Mölndal, March 2016
Luyu Wang

Notation

Frequently used acronym and with name and definition is shown in list below. Acronyis only presented in one chapter are not included in this list.

PF	Pulse frequency, The frequency of current pulses
HFAC	High frequency AC
FPGA	Field Programmable Gate Array
SiC	Silicon Carbide
HF	High Frequency

Contents

Chapter 1
Introduction

1.1 Background and Objective

Public railway transportation is playing an important role in people's daily life in several ways. Especially high speed train is changing people's life. Reduced travel time, town center to town center connection expand people' living area. The author has an experience with high speed trains from Beijing China to his hometown (more than 400km), and the travel time now is one and half hours which was 4 hours before and 3 hours if we chose airplane. At present the highest wheel-rail speed, which is recorded by TGV is 574.8 km/h [1] (Figure 1.1).

Figure 1.1 Example of TGV

The development of modern train is not only focused on the speed but also on the comfortable levels. Lots of auxiliary equipment is needed, such as lighting, fans, air condition machine, and passenger's own devices etc. All these lead to increased power requirement of the auxiliary converter, which normally is a three phase 230/400V 50 Hz power supply.

The function of the auxiliary converter is to generate three phase 230/400V

50 Hz power from the train internal DC links, and to provide isolation between the train high voltage side and the consumer side. The power rating of the auxiliary converter can normally vary in several tens of kW. Figure 1.2 shows the position of the auxiliary converter in trains.

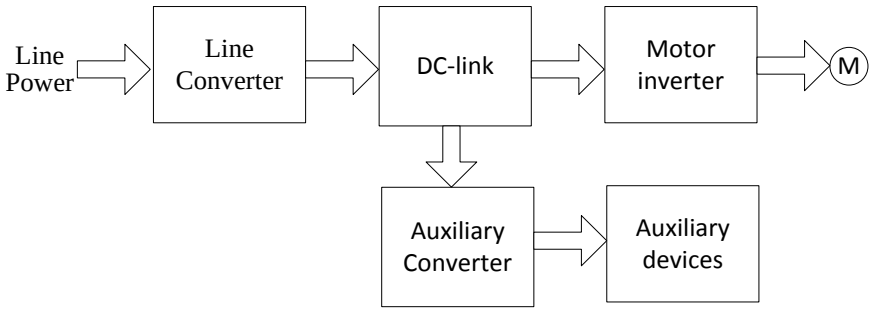


Figure 1.2 Position of Auxiliary Converter in Trains

Conventional auxiliary converter needs a 50 Hz transformer and output filters for isolation and for sinusoidal output respectively, which both are bulky components. Reducing volume and weight of the transformer means cost reduction both for the train manufacturer and for their customers. This work focuses on developing a new auxiliary converter topology to reduce the weight and volume of the auxiliary converter.

1.2 Previous work

Conventional Auxiliary converter

Current design of an auxiliary converter for railway traction application is to use a two level, hard switching three phase inverter [38 39]. The output from the three phase inverter is filtered with a low pass filter to generate sinusoidal output voltage. After the filter a low frequency transformer is used to adapt the voltage and for isolation purpose. Figure 1.3 is the block diagram of conventional Auxiliary Converter.

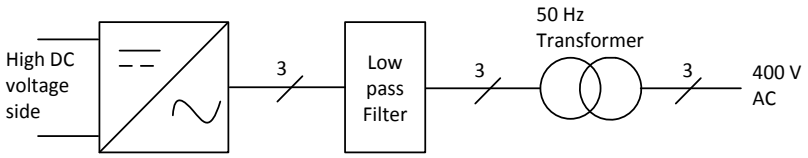


Figure 1.3: Conventional Auxiliary Converter

The low frequency transformer is a bulky component which needs to be replaced.

DC-DC type auxiliary converter

Newer supply system [2-4] [40-42], consisting of redundant resonant DC-DC converter as input and diverse output modules supplied by a common dc intermediate circuit. The input and output side are electrically separated by a light weight high frequency (HF) transformer. See Figure 1.4. Similar activities have been going on to remove the low frequency transformers [5][6] from trains.

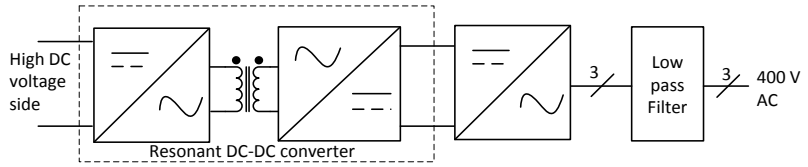


Figure 1.4: DC-DC type Auxiliary Converter

This type of converter has 3 energy conversion stages (DC-AC-DC-AC) which results in reduced system efficiency due to the additional losses caused by redundant energy conversions. High frequency link cycloconverters [7, 28-35] have been developed for different supply applications which try to omit redundant energy conversion stages and increase efficiency. The work in [7, 28-36] generates output AC voltage directly from a high frequency AC voltage, which is the output from an H-bridge. The output stage contains 12 transistors and diodes and will have an increased cost on semiconductor devices.

1.3 Main contributions

The results and contributions of this thesis are presented in chapter 2 to 4 and discussed in chapter 6. The main contributions of the thesis can be summarized as follow:

- A hard switched new topology of auxiliary converter with reduced number of components is presented.
- A control method for controlling the hard switched new topology converter is developed. The possibility to implement the control algorithm in FPGA is verified.
- The energy balance method for controlling the proposed resonant auxiliary converter is given and analyzed and the control algorithm is implemented in simulation model.
- Prototypes are designed and implemented for studying the proposed auxiliary converter.
- A new base drive topology for SiC BJT are developed.

1.4 Outline of the thesis

Chapter 1 is devoted to a brief outline of this thesis and a short introduction to each chapter is given. This thesis focuses on developing new auxiliary converter topologies for railway applications, which covers concept validation with circuit simulation, hardware implementation and laboratory test.

In this thesis two new topologies are introduced. Chapter 2 introduces the proposed hard switched auxiliary converter. The control method, selection of passive components and losses estimations are included in chapter 2

To reduce the switching losses, one way is to reduce the number of switching times or introducing zero current/voltage switching. The possibility to implement soft switching technique is investigated in chapter 3, and as a result a resonant version of the proposed auxiliary converter is presented. The development is based on simulation. The controlling method is thoroughly investigated in this chapter, and the converter concept is

validated by circuit modeling in LTspice [10].

Development of converter prototypes is the next steps after modeling in the simulation software. In this thesis two converters prototyped are presented. A small down sized prototype are implemented for developing the control software for the proposed hard switched converter. Then a bigger prototype is implemented to study how the new topologies converter behaves in practice. This part of the work is included in chapter 4

Chapter 5 has investigated how to control Silicon carbide BJT with high efficiency. A new drive circuit topology is developed in chapter 5.

The thesis ends with some concluding remarks and suggestions for future research in Chapter 6.

1.5 Publications

Part of the work presented in this thesis has been presented in the following publications:

Wang, L., Karlsson, P, Bängtsson, H. (2013), "A new isolated, output filter free DC-AC converter topology". 15th Conference on Power Electronics and Applications (EPE13), Lille, France, Sept. 3-5, 2013.

Wang, L., Bängtsson, H. (2012), "How to control SiC BJT with high efficiency?". 7th International Conference on Integrated Power Electronics Systems (CIPS2012), Nuremberg, Germany, March 6-8, 2012.

Ottosson, J., Wang, L. (2012), "Comparison of cooling requirements for Si and SiC based inverters in a hybrid vehicle application". International Conference and Exhibition for Power Electronics, Intellegent Motion, Renewable Energy and Energy Management, Power Electroncis South America 2012, Sao Paulo, Brasil, Sept. 11-13, 2012

Chapter 2
Proposed Inductive Link Auxiliary Converter

2.1 Introduction

As stated in the previous chapter the DC/DC type auxiliary converter has 3 energy conversion stages: A full bridge converts the DC link voltage to a HFAC (high frequency AC), this conversion provides isolation between input and output. The HFAC is converted to a DC voltage by a rectifier circuit. The DC voltage is then converted in a three phase inverter to an AC voltage with the 50 Hz fundamental frequency. These three stage energy conversion are considered as redundant. Redundant energy conversions not only cause more losses but also require additional components, the system becomes bulky. The idea of this work is to omit the redundant conversion stage and to generate the 50Hz AC output voltage directly from the intermediate product HFAC.

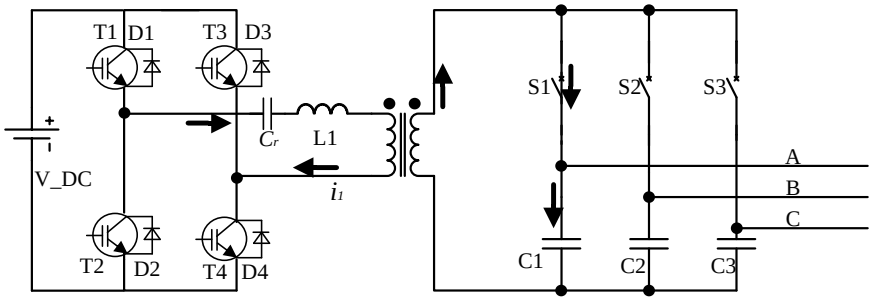


Figure 2.1a Proposed resonant auxiliary converter topology

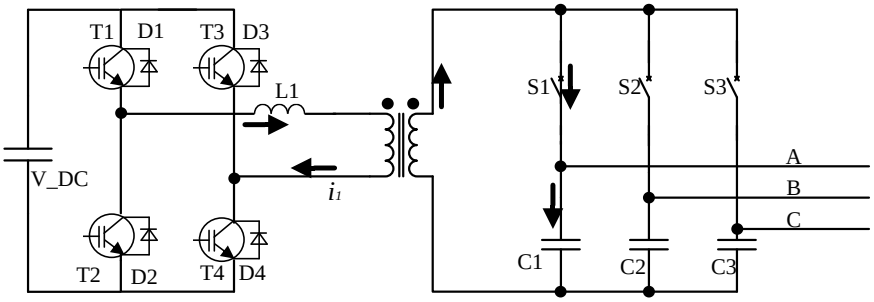


Figure 2.1b Proposed inductive link auxiliary converter topology

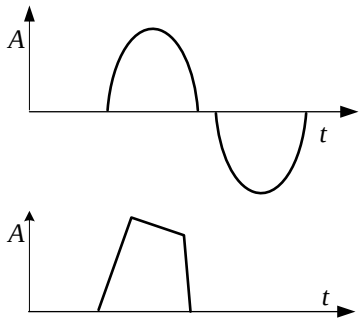


Figure 2.1c Example of current pulses

The proposed auxiliary converter topologies are shown in Figure 2.1a&b. The input stage is a 4-quadrant converter and is connected with either an inductor (inductive link) or series resonant circuit (resonant link). A high frequency transformer is used for galvanic isolation. The output stage is formed by bidirectional switches and output capacitors. The function of the input stage is generating high frequency current pulses; either positive or negative depending on the need of the output stage. The current pulses can be selected by the bidirectional switches to charge/discharge the output capacitors. Arrows in Figure 2.1a&b is an example showing the current path when the output capacitor of phase A is charged.

There are several ways to generate the HFAC pulses. The first thought is using a series resonant circuit to generate the resonant current pulses which is shown in the upper part of Figure 2.1c. The working principle of the

resonant link for creating current pulses is similar to a load resonant converter [8][9], and it has a potential to reduce losses by using soft switching technique. However, this method cannot be applied directly to our application since the voltage over the series resonant circuit and especially the voltage on the output side, both are AC voltages, which is different from load resonant converters. A dedicated modulation method is needed for controlling the resonant circuit. One drawback of the resonant circuit is that there is always a negative current pulse followed by a positive pulse since the polarity of the current pulse are related to the polarity of the resonant capacitor. This limits the freedom for selecting the polarity of the required current pulses, thereby creating problems when the three phase loads are not symmetrical.

By removing the resonant capacitor of the series resonant circuit, the HFAC pulses could be generated by the inductive link method. With the inductive link method, the polarity of the current pulses can be either way. This feature guarantees that the converter can work with unsymmetrical loads. The drawback of this method is that hard switching at peak current might cause more losses. The inductive link method is thoroughly investigated in this chapter, and the resonant method will be analyzed in chapter 3.

The proposed auxiliary converter topologies require less components both active and passive compare to the DC-DC type auxiliary converters since it has lower number of energy conversion stages. The saved components and added components are summarized in Table 2.1.

Table 2.1: Saved and added components

Saved components	Added components
4 rectifier diodes	3 bidirectional switches
2 DC link capacitors	3 output capacitors
Three Phase IGBT module	
Three phase output filter	

The calculated output voltage is shown in Figure 2.2. This is to verify the possibility to generate the requested output ac voltages with current pulses. This verification is using simplified resonant current packages (Figure 2.1c) which are formed from a constant resonant current source and without load (Figure 2.2a) and with resistive loads (Figure 2.2b) on the three phase side.

Sinusoidal output voltage with a reduced amount of low order harmonics is a feature of our proposed topology.

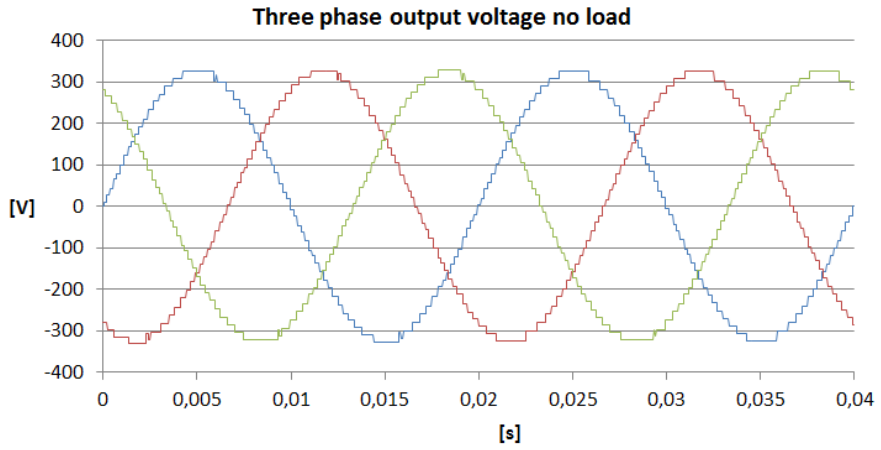


Figure 2.2a Calculated no-load output voltage

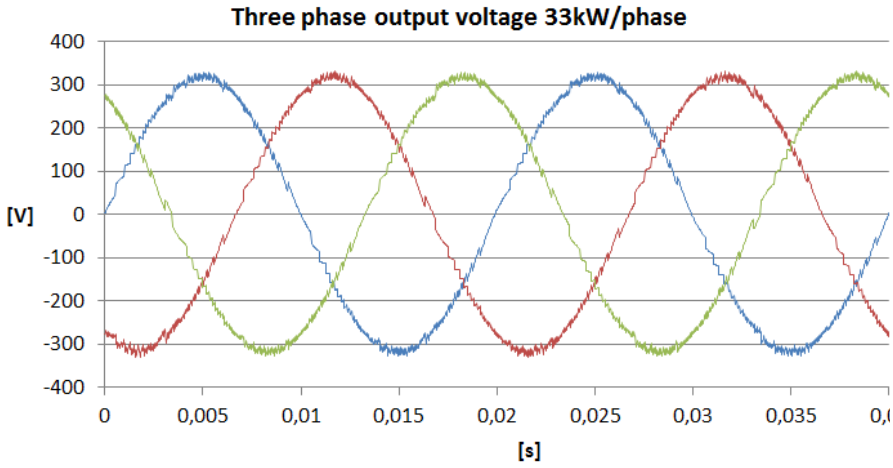


Figure 2.2b Calculated full load output voltage

2.2 Control Algorithm and Modulation

This section focuses on developing the control algorithm and modulation method for the inductive link version auxiliary converter. The generation of current pulses, the calculation of the transistor duty ratios based on the need from the outputs, are investigated. The modulation and the control algorithm are also thoroughly discussed.

The current pulses

The intermediate product HFAC is the high frequency current pulses (see Figure 2.3). The current pulses can be considered as discrete charge carriers. These discrete charge carriers are selected and delivered to the output capacitors via bidirectional switches to generate the sinusoidal output voltages.

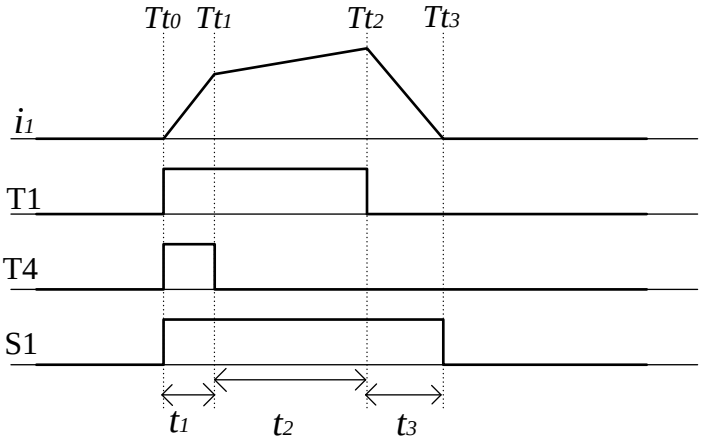


Figure 2.3 Operational waveform

Figure 2.3 gives the operational key waveform for generating the current pulses. Assume a positive charge is required for C_1, the transistors T1 T4 and S1 in Figure 2.1b shall be switched on to start generating the current pulse. One switching period T is divided into 3 time intervals labeled t_1, t_2 and t_3, respectively. At t_0 transistors T1, T4 and S1 are turned on. The current i_1 starts to increase from zero. During this time interval the energy is fed from dc-link to the inductor L1 and to the output capacitor

C1.Transistor T4 is switched off at time Tt_1 and the current starts freewheeling via T1 and D3. During this time interval the energy is transferred between L1 and the output capacitor C1. After Tt_2 transistor T_1 is turned off, the current starts to decrease via D3 and D2 until it reaches zero at Tt_3. In this period the energy is fed from $L_1$to the DC-link and the capacitor C_1.

The current pulses are charge carriers, it is essential to study the charge carry ability of a single current pulse. Figure 2.4 shows examples of 3 types of current pulses. The charge Q that is carried by the current pulses is equal to the area of the current package.

Here are the inputs to calculate the charge Q:

I) The current pulse interval has a length of T, T is the same for all current pulses and T is defined as the pulse period in this work.

II) Assuming the variation of the output voltage and the DC link voltage during one current pulse interval is small and can be neglected. The current derivatives a, b and c can be considered as constant during one current pulse.

III) V_{dc} , V_{out} , and L are the DC-link voltage, the output voltage and the inductance of L1respectively.

IV) Assuming a positive charge is needed from an output phase A as shown in Figure 2.1b.

There are three types of current pulses, shown in Figure 2.4, depending on when the transistors are turned off and turned on:

1) If two transistors in Figure 2.3 and 2.1 are turned off at the same time (t_2 is zero), the shape of the current pulse is a triangle (triangle 1-5-6) and the area within the current envelope is the largest in all those three type of current pulse described in this section. This type of current pulse carries the most charge among those three type of current pulses.

2) If only one transistor has been turned on at the beginning (t_1 is zero), the shape of the current pulse is a triangle (triangle 3-5-6) and has

the smallest area. This type of current pulses carries the least charge among those three types of current pulses.

3) If two transistors are not turned off at the same time as shown in Figure 2.3. The current pulse has a shape of quadrilateral (2-5-6-4). The size of the area is between type 1 and 2.

The maximum value Q_{max} can be given by calculating the area of triangle from type 1) which gives (2.1). The minimum charge Q_{min} is more complex than the calculation of Q_{max}. In the situation which is shown in Figure 2.4a, the Q_{min} can be calculated by (2.2).

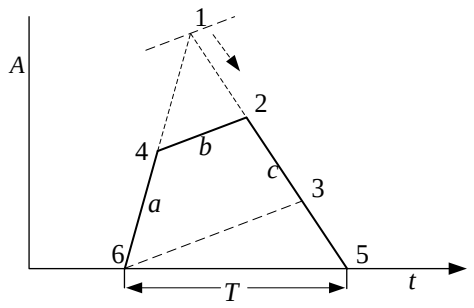


Figure 2.4a Example of a current pulse

$$Q_{max} = \frac{V_{dc}^2 - V_{out}^2}{4 V_{dc} L} T^2 \tag{2.1}$$

$$Q_{min} = \frac{-bc}{2(b-c)} T^2 \tag{2.2}$$

(2.2) gives the equation of how to calculate the minimum charge of the inductive link topology. However (2.2) is only applicable for one special condition. Actually the current pulses can be classified in two conditions as described below:

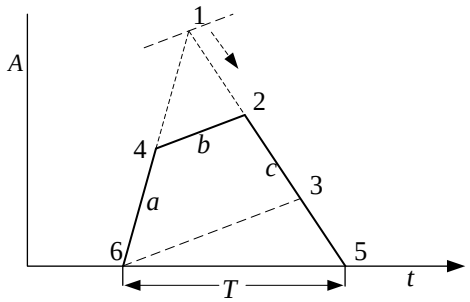


Figure 2.4b Example of a current pulse

Figure 2.4b shows a current pulse, which has the same polarity as the output voltage. In this case Q_{min} equals to the area of the triangle and the value is given by.

$$Q_{min} = \frac{-bc}{2(b-c)} T^2 \tag{2.18}$$

Figure 2.4c shows the case when the current pulse has the opposite polarity as the output voltage. Q_{min}can be calculated as (2.19)

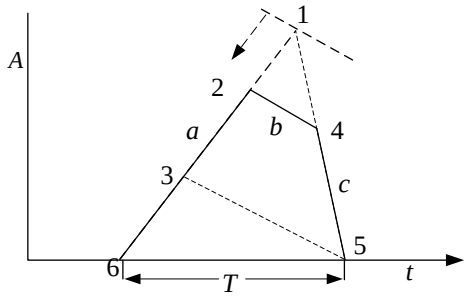


Figure 2.4c Example of a current pulse

$$Q_{min} = \frac{-ab}{2(a-b)} T^2 \tag{2.19}$$

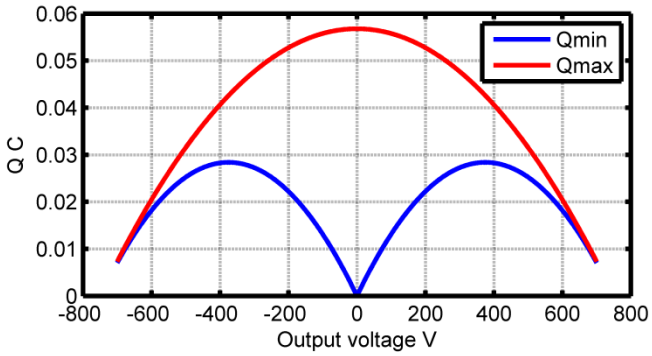


Figure 2.5 Calculate Q_{max} and Q_{min}

Figure 2.5 shows the calculated Q_{max} and Q_{min} for a 100 kW auxiliary converter The Q_{max} reaches its peak when the output voltage is zero and drops with increased absolute value of the output voltage. The charge carry ability is related to the voltage difference between the DC-link voltage and the absolute value of output voltage according to (2.1). The output voltage must be lower than the DC link voltage to transfer power from input to outputs.

Calculating transistor duty ratios

The duty ratio of each transistor is calculated from t_1 t_2 and t_3 which is shown in Figure 2.3. The duty ratios of transistor T_1, T_4/ T_2, T_3 are given in (2.3) and (2.4) respectively

$$D_1 = \frac{t_1}{T} \tag{2.3}$$

$$D_2 = \frac{t_1 + t_2}{T} \tag{2.4}$$

The calculation of t_1, t_2 and t_3 is described here. Assuming that the current pulse period is T; a, b and c are the current derivatives during the time intervals t_1, t_2 and t_3, respectively. Q is the charge which is required by capacitor C_1 from the load. The sum of t_1, t_2 and t_3 should be equal to T which gives (2.5).The current i_1 starts at zero and ends at zero which gives (2.6). The time integration of the current pulse equals to the required charge Q which is shown in (2.7).

$$t_1, + t_2 + t_3 = T \tag{2.5}$$

$$at_1 + bt_2 + ct_3 = 0 \tag{2.6}$$

$$\frac{1}{2}at_1^2 + \frac{1}{2}ct_3^2 + \frac{1}{2}(at_1 - ct_3)t_2 = Q \tag{2.7}$$

Table 2.2 gives the solutions of these second order equations. According to Table 2.2, at least one square root function is needed by the controller, which requires more computation resource to implement the control algorithm. A pre-calculated look-up table might be a good way to reduce the requirement on the micro controller side.

Table 2.2 Solutions of switching profiles

	Solution 1	*Solution 2*
	$Q>0$	$Q<0$
t_1	$t_1 = -\frac{F+Tc}{a-c}$	$t_1 = \frac{F-Tc}{a-c}$
t_2	$t_2 = \frac{F}{a-b}$	$t_2 = -\frac{F}{a-b}$
t_3	$t_3 = -\frac{F-Ta}{a-c}$	$t_3 = \frac{F+Ta}{a-c}$
$F = \sqrt{-(acT^2 + 2Qa - 2Qc)}$		

Control algorithm

Figure 2.6 shows a simplified control chart. The output voltage and the voltage reference are measured and sampled prior to the beginning of each switching period. Calculation of the new duty ratios is done in a short time interval. New calculated duty ratios are updated to the transistors and are kept unchanged in the coming switching period. The calculation time shall be kept as short as possible to reduce the delay time which requires a fast micro controller. If the controller is slow, a compensation for the calculation time delay shall be taken in to account.

Computer technique has developed substantially in the last decades. With powerful micro controllers, and fast control algorithm can be implemented for today power electronic converter. Reference [9] is an example of direct current control implemented in Field Programmable Gate Array (FPGA).

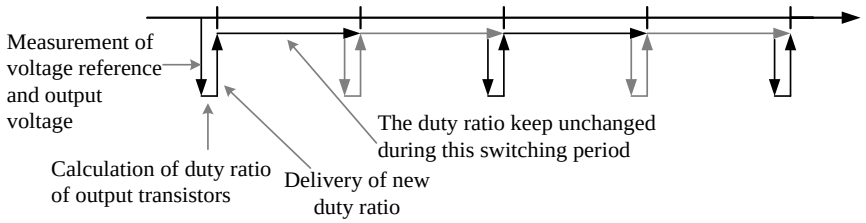


Figure 2.6 Time chart of control algorithm

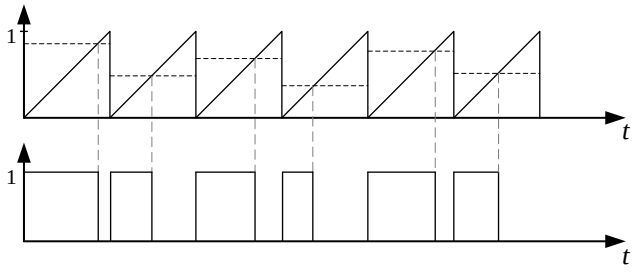


Figure 2.7 Carrier waveforms and transistor gate signals

The generation of a current pulse is shown in Figure 2.1c, transistors T1 and

T4 shall be turned on at the same time but be turned off at different time. Saw tooth carrier with positive slope is selected for this purpose. Figure 2.7 explains how the gate signal is generated by carrier waves and transistor duty ratios.

Until now we have collected enough information to control our proposed hard switched auxiliary converter. Prior to each switching period, voltage references and output voltages of three output phases are measured and sampled. Based on the sampled data, the required charges Q, Q_{max} and Q_{min} can be calculated afterwards for all three phases.

There are mainly two ways to decide which phase that shall be charged. It is a nature thought to treat output phases equally and each output phase is charged/discharged every third switching period. A more optimal way is to charge/discharge the phase that has the largest voltage error. In our simulation models the first method is chosen to reduce system complexity.

The next coming step is to define the input for calculation of the duty ratios of the output transistors. The details of how to define Q based on the sampled data is shown in Figure 2.8.

Calculation of the duty ratio is done in the next step by using the equation from Table 2.2 and (2.3) and (2.4). After that the duty ratio is calculated and applied to the transistor.

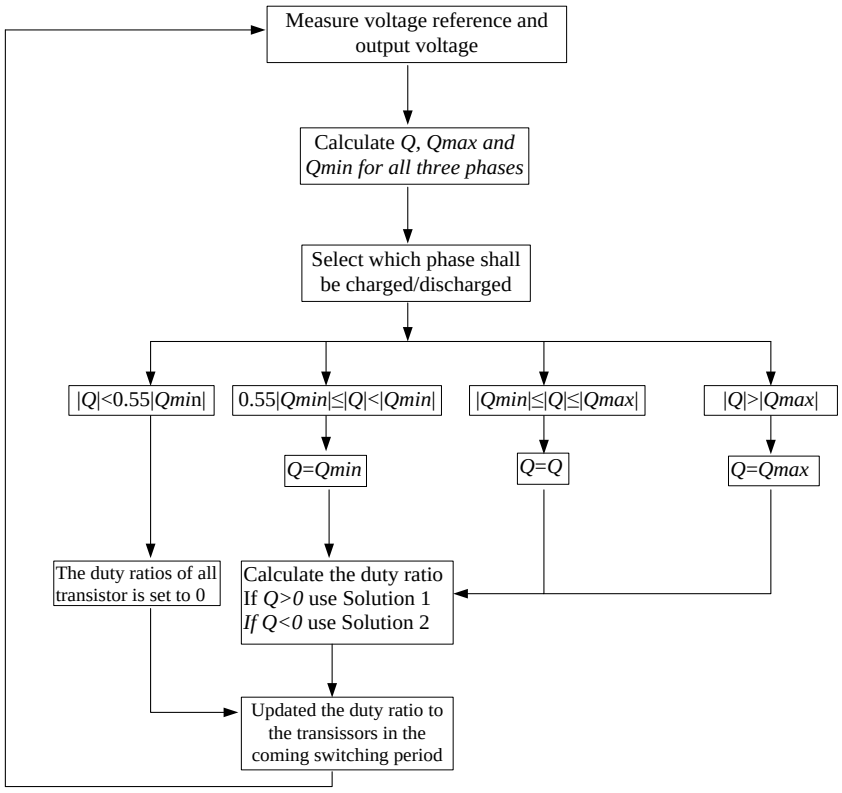


Figure 2.8 Control flow chart for inductive link auxiliary converter

2.3 Analysis and Design Consideration

Value of passive components

The function of the output capacitor is similar to an output filter and an energy buffer. It converts the current pulses to sinusoidal voltages. The capacitance of the capacitor is related to the maximum output voltage ripple and the THD (total harmonic distortion). Larger output capacitor reduces the output voltage ripple and the THD. For a three phase converter as shown in Figure 2.1b, three output phases share the current pulses, in average for

one output phase the capacitor is charged every third pulse period. Assuming the output capacitor is charged every third pulse period. In most severe conditions which correspond to the moment when the load current reaches its peak value, the output capacitor should keep the output voltage neither to drop or increase more than the maximum allowed voltage ripple between two current pulses. Assuming $Current_{amp}$, T_{charge} , ΔV and V_{rms} is the maximum output current amplitude, the charging period of each single output phase, the maximum allowed voltage ripple and the nominal output voltage respectively. The value of the output capacitor can be calculated as below.

$$\Delta V \geq \frac{Current_{amp} \times T_{charge}}{C} \tag{2.8}$$

Rewriting (2.8) gives (2.9)

$$C \geq \frac{Current_{amp} \times T_{charge}}{\Delta V} \tag{2.9}$$

Since:

$$Current_{amp} = \sqrt{2}\frac{P_{max}/3}{V_{rms}} \tag{2.9a}$$

$$T_{charge} = \frac{3}{F} \tag{2.9b}$$

The output capacitance is given by (2.10)

$$C \geq \frac{\sqrt{2}\frac{P_{max}}{V_{rms}}}{\Delta V \times F} \tag{2.10}$$

The inductance of inductor L_1 in Figure 2.1 is related to the amplitude of the current pulses. Larger inductance reduces the amplitude of the current pulse for the same pulse period. Considering the most severe conditions, which are when the output current reaches its peak value, the charge removed by the output current shall be compensated by the charge delivered by current pulse which gives (2.11)

$$Q_{max} \geq Current_{amp} \times T_{charge} \tag{2.11}$$

Substitute (2.1) into (2.11) will give:

(2.12)

$$L \leq \frac{(V_{dc}^2 - V_{out}^2) V_{rms}}{4\sqrt{2} V_{dc} P_{max} F}$$

Reactive current

There are current pulses circulating between output capacitor and DC-link capacitor to maintain the output voltages. The output capacitor can be considered as a capacitive load of the converter, the corresponding load current can be calculated by (2.13), where V and f are the amplitude and the frequency of the output voltage respectively. The current is 90 degree heading the output voltage. This reactive current is the main root causes losses of the proposed auxiliary converter during standing still. It is essential to keep the output capacitance as low as possible to reduce the reactive current and the losses.

$$I_{rea} = V \times 2\pi f C \tag{2.13}$$

Amplitude of current pulses

Current pulses are the intermediate product in the proposed auxiliary converter energy conversion stage. The amplitude of the current pulses affects the total switching loss and the rms value of the current pulses affects total conduction loss. Those two parameters are essential for dimensioning the semiconductor power module and the transformer.

See (2.14), assuming that the reactive current we have discussed in last subsection is smaller than the amplitude of the load current and thus can be neglected. The current pulses compensate the charge which is removed by the load current.

$$\int_0^T I_{pulse}\, dt = \int_0^{3T} I_{load} dt \tag{2.14}$$

The shape of a current pulse is either a triangle or a trapezoid. The load current I_{load} is a low frequency current, it can be considered as constant during one switching period. (2.14) can be rewritten as (2.15) and (2.16). (2.15) and (2.16) correspond to a triangle shaped current pulse and a trapezoid shaped current pulse respectively, where I_{amp} is the amplitude of the current pulse. Combining these two equations together gives (2.17).

$$I_{amp} = I_{load} \times 6 \tag{2.15}$$

$$I_{amp} > I_{load} \times 3 \tag{2.16}$$

$$I_{load} \times 3 < I_{amp} \leq I_{load} \times 6 \tag{2.17}$$

According to (2.17) the amplitude of the current pulses is much larger than the amplitude of the output current. In the proposed inductive link auxiliary converter the transistor needs to switch off at peak current of the current pulses. The switching losses are one of the main loss sources of the proposed inductive link auxiliary converter.

For delivering the same amount of charge, a current pulse with high big peak

value has higher rms value comparing to continuous constant current. For the same principle, narrow current pulse with bigger peak value has higher rms value than a wide current pulse but with low peak value. So the amplitude of current pulses shall be kept as low as possible to reduce the conduction losses. In other words, for transfer the same amount of charge, several small current pulses with low current peaks are better than single pulses with high peak in order to reduce the conduction losses.

2.4 Simulations and Calculations

Simulations are used to evaluate the control algorithm which is discussed in section 2.2. Parameters of passive components are calculated by using the equation developed in section 2.3. The Simulations are used to simulate the spectrum of output waveform and to optimize the dimension of the output capacitors and the inductor. The simulation is implemented in LTspice [10]. The Calculation which is done in Matlab is used to estimate the semiconductor losses based on silicon IGBTs.

General simulation model

The general simulation model used throughout in all simulations is shown in Figure 2.9. Note that the loads is not included in this circuit, they are formed by three sinusoidal current sources which are connected to nod A, B and C respectively. The amplitude and the phase of the load is adjustable and can simulate different load conditions.

To reduce the complexity of the model, ideal switches and diodes are used for all transistors and diodes. Since ideal components are used, simulation of the converter losses is not included in this simulation model. The losses estimation of the semiconductor devices is carried out by using Matlab.

The function of the sample and hold block is to sample the output voltages, the voltage references and the DC link voltage with a sample frequency equal to switching frequency. It guarantees that the inputs of the controller and the modulation block are not changed during the entire switching period. It is important since the duty ratios for all transistors shall be kept unchanged during one switching period, as stated in section 2.3.

The capacitors in this simulation model are also ideal components. The

value is defined by the equation developed in section 2.3. The parameters of the transformer used in the simulation are from an HF transformer of an auxiliary converter. The inductor is formed of the leakage inductance of the transformer and an ideal inductor L1.

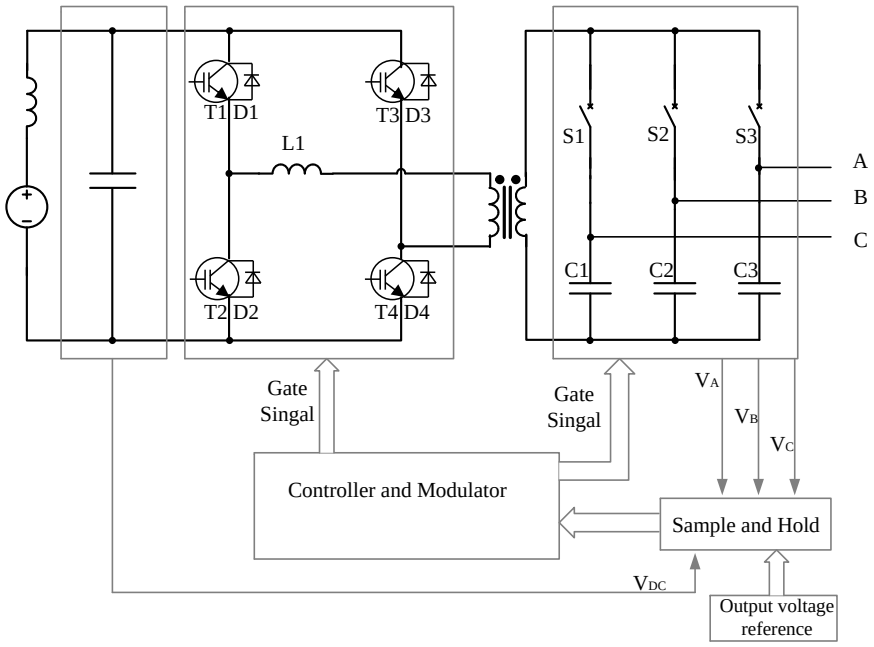


Figure 2.9 Simulation model

Pulse Frequency

The pulse frequency is an essential parameter and is defined as *1/T*, where *T* is the current pulse period. In one pulse period only 2 transistors out of four in the 4-quadrant converter, and 1 bidirectional switch out of 3 in the output phases have switched.

(2.10) and (2.13) tell that higher pulse frequency will result in a reduced output capacitor and a reduced reactive current. Higher pulse frequency also has advantages like the transformer will be lighter and smaller. On the other hand, higher pulse frequency causes higher switching losses, and

commercial semiconductor devices have their own limitation on switching frequency [11]. The maximum switching frequency for a 1200V Silicon IGBT is around 10/20 kHz. For Silicon Carbide (SiC) transistors: JFET, MOFET, BJT, up to 100 kHz switching frequency is reported [12].

Table 2.3 shows the selected pulse frequency (PF) and the corresponding capacitance of the output capacitor and the inductance of the inductor L_1 for a converter with 100kW peak power and 750V DC link voltage. At 10 kHz the output capacitor is 1.53 mF, the reactive current has amplitude of 156A which is 75% of output peak current, this is a high value and leads to high no load losses. With a doubled pulse frequency, the reactive current is reduced to 78A and the value is 39A at 40k Hz, Another way to reduce the reactive current is to reduce the quality of output voltage by using a smaller output capacitor. This will be discussed in next sub section.

Table 2.3 Pulse frequency (PF) vs passive components

PF	Output capacitor	Inductor	Reactive current	Output Current
10 kHz	1.53 mF	17.3 µH	156A	204 A
20 kHz	768 µF	8.67 µH	78A	204 A
40 kHz	384 µF	4.33 µH	39A	204 A

Output wave form vs output capacitances

The output voltage supposes to have sinusoidal waveform with a high frequency voltage ripple as shown in Figure 2.2. The amplitude of the high frequency voltage ripple shall increase with a decreased output capacitance. This high frequency voltage ripple has harmonics with a fundamental frequency of *PF/3*. In this sub sections simulated output waveforms with different output capacitors value are shown. The capacitance is calculated by (2.10) with different ΔV. V_{rms}, P_{max} and *PF* is select as 230*V*, 100 *kW* and 20 *kHz* respectively.

If ΔV is selected to 20V the output capacitor will have a value of 1.53 mF. The no load output waveform looks like the output from a multilevel

converter with lots of levels as shown in Figure 2.10. Figure 2.11 shows the main harmonic. The amplitude of the harmonics is much lower comparing to 230V 50 Hz fundamental frequency (not shown in Figure 2.11). There are also low frequency harmonics below 6 kHz as shown in the Figure 2.11.

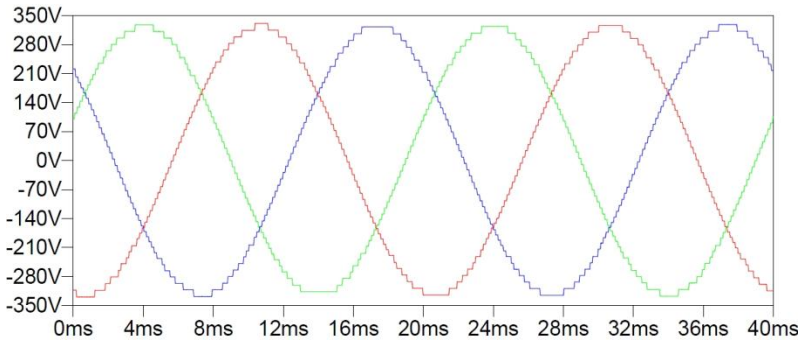


Figure 2.10 No load output wave form with 1.53 mF output capacitors

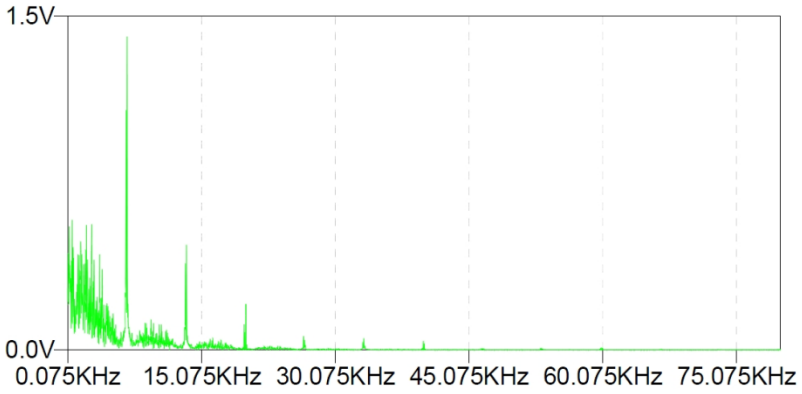


Figure 2.11 No load output harmonics with 1.53 mF output capacitors

Figure 2.12 and Figure 2.13 show the output waveform with 100 kW resistive load. The output voltage is sinusoidal shaped plus small high frequency saw tooth signals. In frequency domain comparing to no load waveforms, low frequency harmonics has a decreased value, but high frequency harmonics above 6 kHz are increased. High output current requires more high frequency current pulses, which increases the high frequency harmonics.

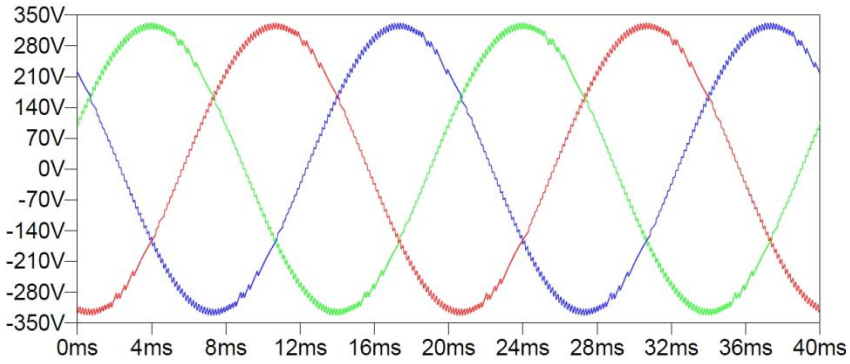


Figure 2.12 Full load output waves with 1.53 mF output capacitors

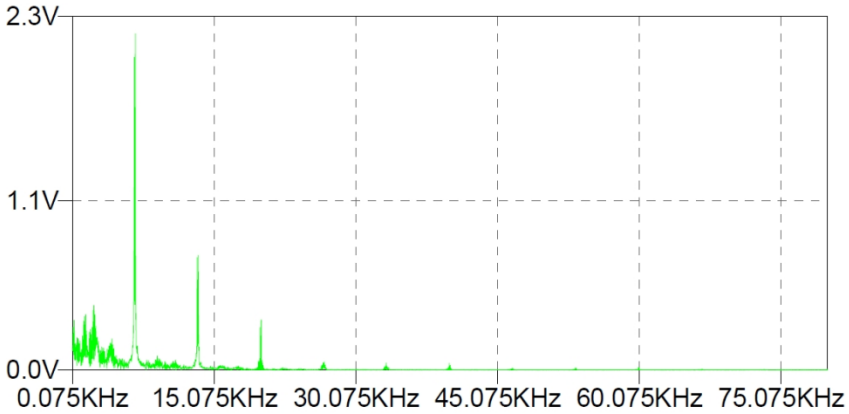


Figure 2.13 Full load harmonics with 1.53 mF output capacitors

It is beneficial to use smaller output capacitors: Lower cost, smaller reactive current, lower weight and volume. Especially the capacitors in mF range are bulky components. It is essential to use optimal output capacitors. The capacitance of the output capacitor will decrease to half, to 768 μF, if ΔV is selected to 40V. The no load and full load waveform are shown from Figure 2.14 to 2.17. Compare Figure 2.10 to Figure 2.13, in frequency domain with reduced output capacitances. For the no load case, harmonics below 6 kHz have increased dramatically, the high frequency component above 6 kHz has similar amplitude. For the full load case, the high frequency harmonics above 6 kHz is increased dramatically.

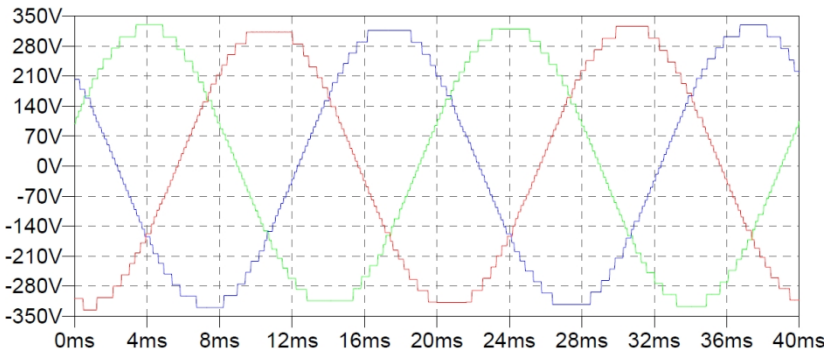


Figure 2.14 No load output wave form with 768 µF output capacitors

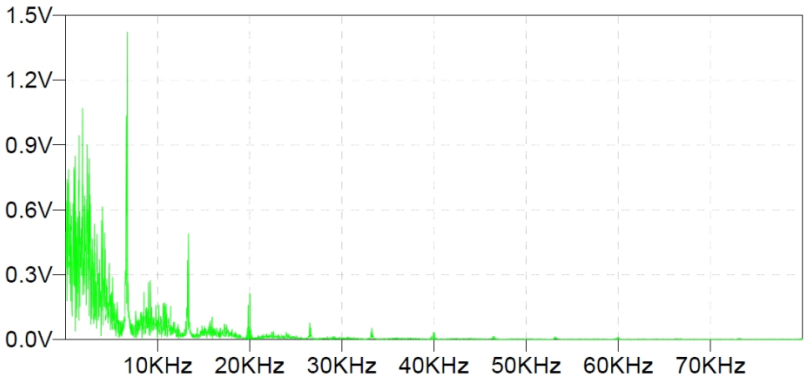


Figure 2.15 No load harmonics with 768 µF output capacitors

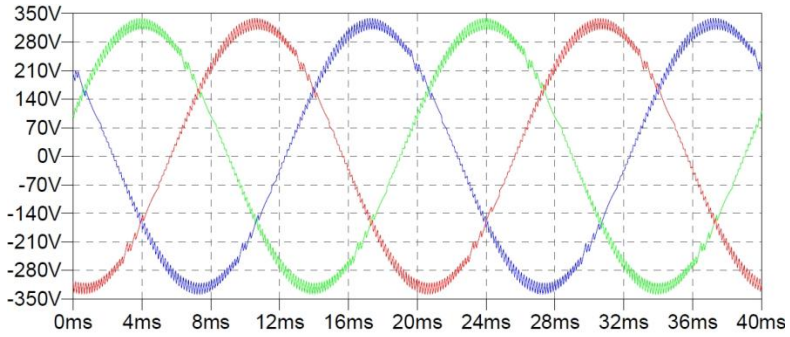


Figure 2.16 Full load output wave form with 768 µF output capacitors

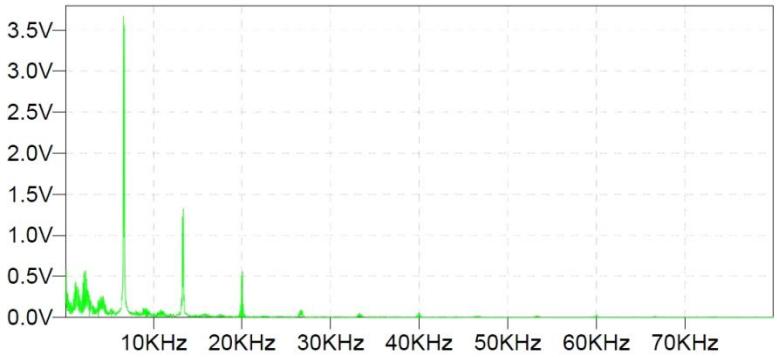


Figure 2.17 Full load output harmonics with 768 µF output capacitors

The output capacitance can be further decreased to 512 µF, if ΔV is chosen to 60V. Figure 2.18 to Figure 2.21 shows the output curves. The voltage step in Figure 2.18 is high with high output voltage. This phenomenon can be explained by Figure 2.5: at low output voltage, Q_{min} is lower than in the high output voltage cases which results in smaller output voltage steps. This phenomenon can also be found in full load cases, the saw tooth signal has smaller voltage ripple with low output voltage. In frequency domain, the no load trend is that the harmonics below 6 kHz are increased, due to that the step chair curve has higher voltage steps. For the full load conditions, higher frequency harmonic is increased because the saw tooth voltage ripple has higher value.

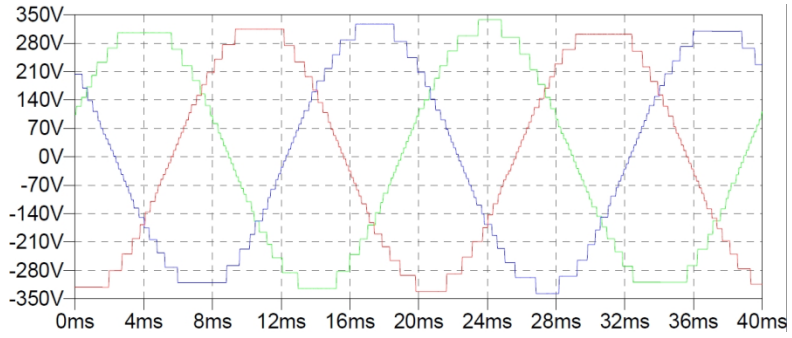


Figure 2.18 No load output wave form with 512 µF output capacitors

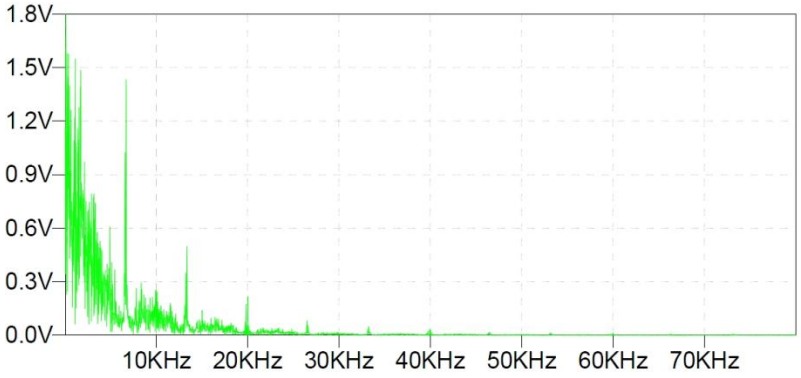


Figure 2.19 No load harmonics with 512 µF output capacitors

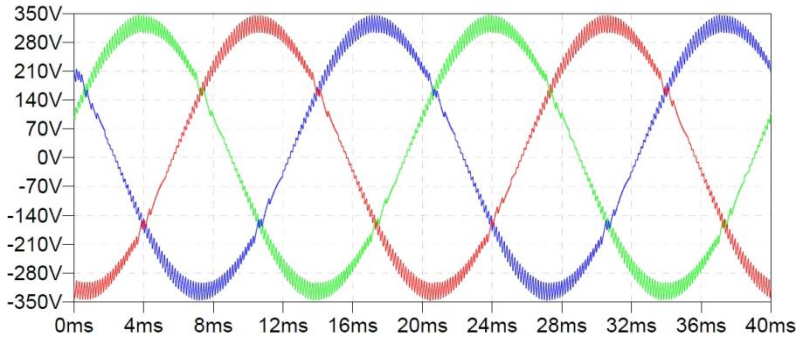


Figure 2.20 Full load output wave form with 512 µF output capacitors

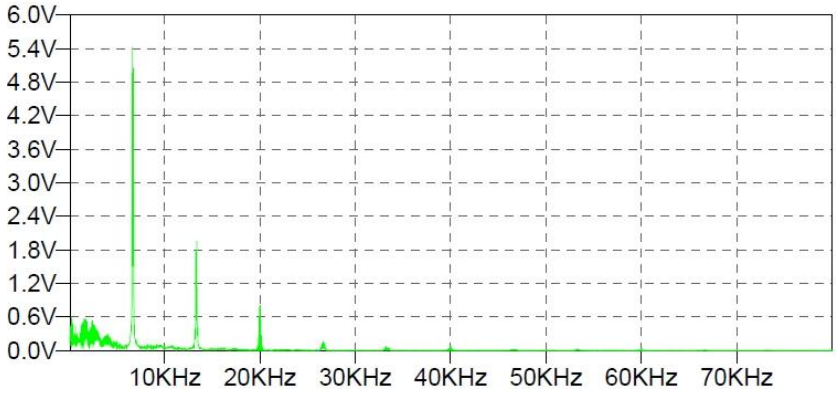


Figure 2.21 Full load output harmonics with 512 µF output capacitors

Simulated high frequency pulses

Figure 2.17 shows that the full load amplitude of the high frequency current pulses are high and it results in high rms value of the current pulses. Figure 2.22 is the simulated current of the transformer primary. The upper side figure is the current pulses in one electrical period (50 Hz); the lower side figure is the zoom in time domain to show the details of the current pulses. The amplitude of the current pulses agrees with the result from figure 2.17, the rms value of the current pulses is simulated as 535A.

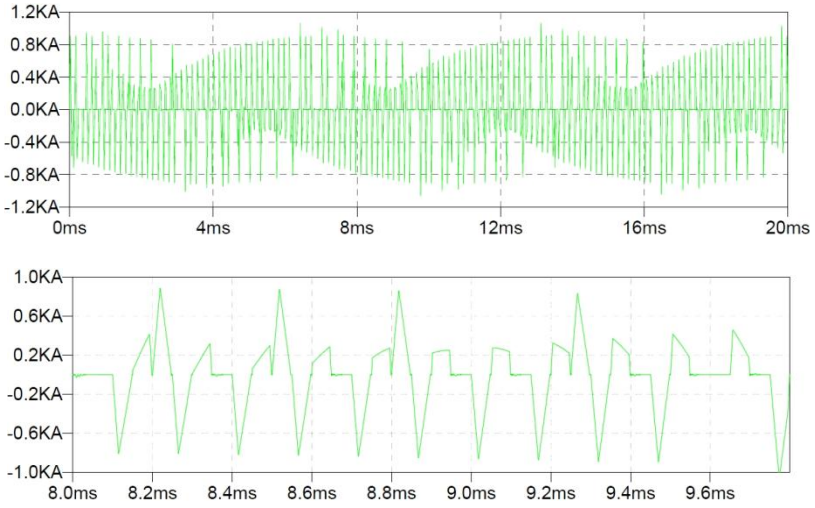


Figure 2.22 Current wave form of transformer primary.

Losses calculation

Losses are always an important issue in converter design. In this sub section, semiconductor losses are calculated based on the commercial available components. The purpose of this losses calculation is to have a figure to show how the losses are generated and how the losses are distributed between different parts of the converter main circuit. The losses that are generated by the output capacitors, the transformer, and the cable copper are not included in this investigation. The losses calculation is carried out by a Matlab m.file. The main reason not including the losses estimation in LTspice is that it is difficult to find spice model for most IGBTs, and the system will become complex with real semiconductor models.

The turn-on losses of the transistors in the input 4-quadrant converter are neglected since they are turned on at zero current. Switching losses of the diodes in the 4-quadrant converter can also be neglected due to the zero current switch-off of the diodes. The switching losses of the transistors and diodes in the output transistor are neglected since all these components are zero current switching.

The losses included in this calculation are: Conduction losses of all the transistors and diodes and turn off losses of the transistor in the input 4-quadrant converter. Figure 2.23 shows the simplified key steps of the losses calculation for one output phase. The load current contains two parts: output current and reactive current that circulates between the output capacitors. The sum of these two current times the charging interval will be the required charged *Q*. Using *Q* the switching profiles (t_1,t_2 ,t_3 in the Figure) of the transistor can be calculated. The next step is to calculate the losses based on the losses data and the losses model of the proposed auxiliary converter. The input parameters for calculation of the semiconductor losses are shown in Table 2.3.

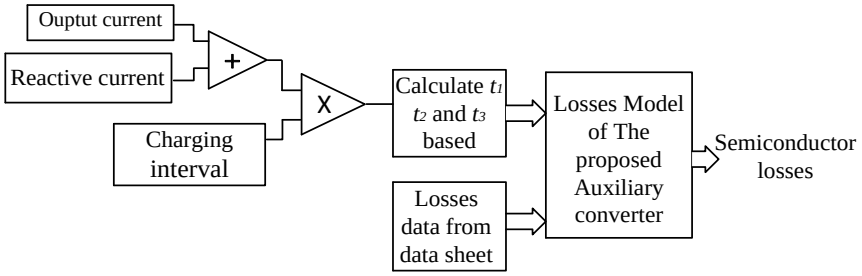


Figure 2.23 Simplified losses calculation model

Table 2.3 Parameters of calculation and key components

DC link voltage	750 V
Maximum power	100 kW
Switching freq.	20 kHz
Output voltage	230 Vrms
Output capacitor	768µF
Inductor L_1	9.9 µH
Bidirectional switch	FS600R07A2E3
H-Bridge	FF600R12IP4

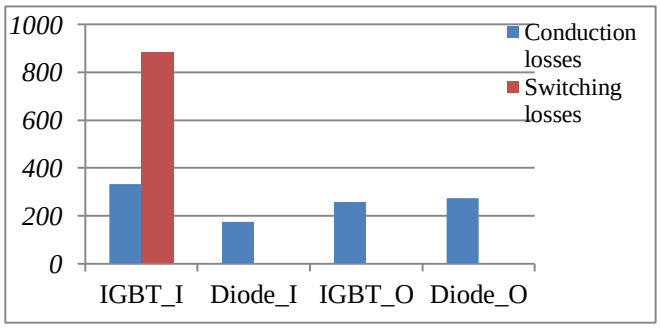


Figure 2.24a Calculated full load losses

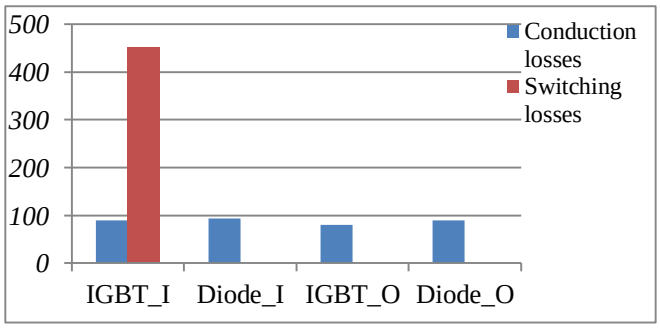


Figure 2.24b Calculated no load losses

See Figure 2.24 for the calculated semiconductor losses. IGBT_I and Diode_I means IGBT and diode that belongs to the input stage. IGBT_O and Diode_O means IGBT and diode that belongs to the output stage. The switching losses are around 50% of the total losses, even if only the turn off losses of the transistors in the input stage is involved. One reason for high switching losses is that the transistors are always turned off when the current is high. The total semiconductor loss is 5.77 kW for 100 kW resistive loads with silicon IGBTs. The no-load losses are calculated to 2.41 kW (see Figure 2.24b).

2.5 Summary

In this chapter an inductive link auxiliary converter topology is introduced. The calculation of passive components values are given. Methods for generating current pulses and modulation method are investigated. The control algorithm are given and implemented in LTspice. The simulated output voltages are sinusoidal shaped with very low amount of harmonics. The calculation of the semiconductor losses is given for estimating the losses distribution with active devices.

Chapter 3
Proposed Resonant Link Auxiliary Converter

3.1 Introduction

A resonant converter topology is introduced to reduce switching losses which are caused by simultaneous high voltage across and high current through the semiconductor devices, when the device changes from conducting to blocking state or vice versa. Another feature of resonant converters is the ability to control the time derivative of the voltage and/or the current. According to the results from the end of chapter 2 switch losses contribute around 50% of total semiconductor losses. Reduction of the switch losses is the main purpose to investigate the resonant version of the proposed auxiliary converter. This chapter starts with a study of the series load resonant converter, and then investigate the proposed resonant auxiliary converter thoroughly.

3.2 Load resonant converters

Three types of resonant converters have the feature of zero voltage or zero current switching [13]: load resonant converters, resonant switch DC/DC converters, resonant dc link and forced commutated converters. The proposed resonant DC ac converter has a similar operation principle as load resonant converter (The load is part of the resonant tank). In this sub section, the basic operation principle of the load resonant converter is investigated. In the following sections, the resonant DC/DC converter and resonant DC/AC converter are referring to as series load resonant DC/DC converter and series load resonant dc ac converter respectively.

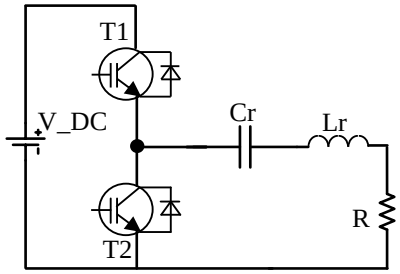


Figure 3.1a Resonant DC/AC converter

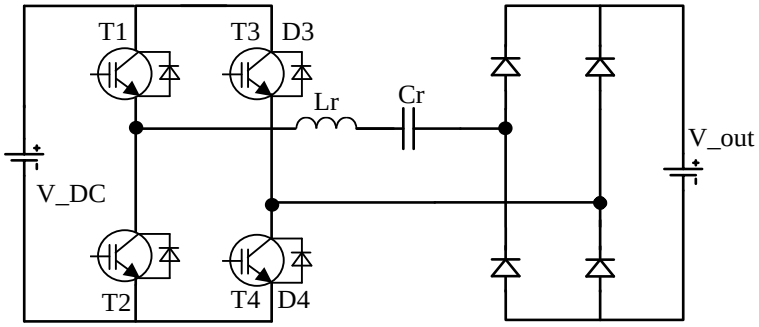


Figure 3.1b Resonant DC/DC converter

Load resonant converter contains either one/two phase legs. The output of the phase leg is connected to a series/parallel resonant tank which contains a capacitor, an inductor and the load. Normally the load is a resistor and may contain part of the inductor and the capacitor. This type of converter is delivering only ac current to the load, and with this feature it is also called a resonant dc ac converter (See Figure 3.1a). This type of converter is used in induction heating applications [13]. If a DC output voltage is needed, a rectifier is connected at the output. The converter then becomes a resonant DC/DC converter. In some applications a transformer is connected between the rectifier and the rest of the converter for galvanic isolation.

Control of the resonant DC/DC converter

Frequency control and phase shift control are the two common methods for controlling the load resonant converter. Frequency control: the resonant current is controlled by changing the impedance of the resonant tank. This is achieved by changing the switching frequency. The second method is phase shift control: the resonant current is controlled by changing the input voltage of the resonant tank. This is done by changing the phase shift angle between the converter phase legs.

When using varying frequency for controlling the resonant current, the frequency is mainly operating at two areas [14]: either above or below the resonant frequency of the resonant tank. The resonant frequency is calculated as

$$\omega_r = 2\pi f_r = \frac{1}{\sqrt{L_r C_r}} \tag{3.1}$$

If the converter operates above the resonant frequency, the resonant tank will appear inductive due to the inductor reactance dominates. The resonant current lags the output voltage of the phase terminals. As shown in Figure 3.2 transistors are turned on at zero current and zero voltage since the current is fed through the anti-parallel diode during turn on of the transistor. While the turn off of the transistor is hard turn off with inductive load. By adding a capacitor snubber between the transistor collector and the emitter makes the turn off of the transistor a zero voltage switching in heavy load conditions [15]. On the other hand at lower load condition it introduces additional losses at turn on of the transistor [15]. By changing the switching frequency the impedance of the resonant tank varies thereby the resonant current varies, and this is the principle to control the resonant current.

If the converter operates below the resonant frequency (See Figure 3.3), the resonant tank appears as a capacitive load. The resonant current is leading the output voltage of phase legs. The transistor experiences hard turn on with capacitive load and zero current/voltage turn off. Capacitor snubber is not suitable in this case since it introduces high collector current peak during turn on of the transistor.

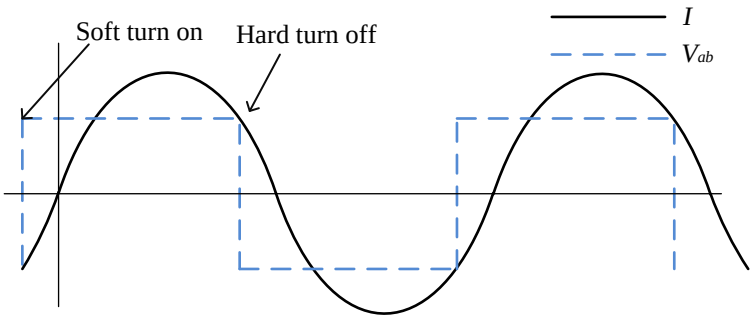


Figure 3.2 Current lagging the converter output voltage

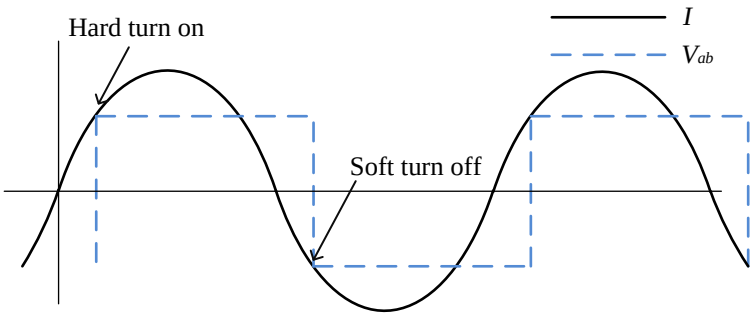


Figure 3.3 Current leading the converter output voltage

The basic principle of phase shift control is described here. The output voltage from an H-bridge V_{ab} is the voltage difference between phase output voltage V_a and V_b. It relates to the state of the switch in the H-bridge. If T1 is on T2 is off, T3 is off and T4 is on, V_{ab} will equal to V_{dc}. If T1 is on and T3 is on, V_{ab} will be equal to zero. Assume the two bridge legs are operating at the same switching frequency and the duty ratio is 50%. The waveform of V_{ab} with phase shifted angle is shown in Figure 3.4. The $V_{ab}$is increasing with increased phase shifted angle, by changing the phase angle,

the output voltage is changed, and thereby the resonant current is controlled. The phase shift angle is defined according to (3.2)

$$\alpha = \frac{T_p}{T_s} \times 360^o \qquad 3.2$$

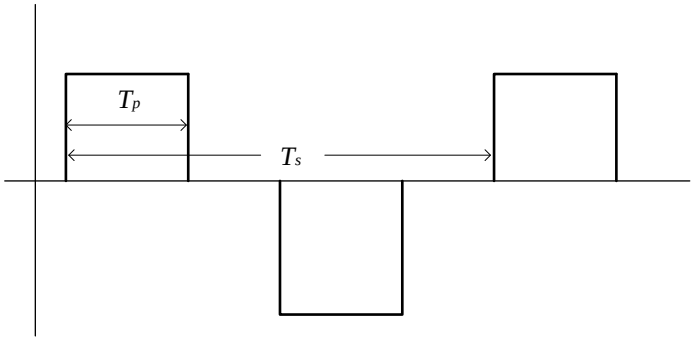


Figure 3.4 Input voltage of a phase shift control

Energy analysis of resonant DC/DC converter

Assuming a resonant DC/DC converter is operating at steady state with frequency control and the switching frequency is above the resonant frequency. In steady state for the same output voltage and output current, the amplitude of the resonant current and the switching frequency shall also be in steady state. In a half switching period, the resonant current starts from zero and ends with zero ampere, the voltage over the resonant capacitor varies from $-V_r$ to V_r. After this half electrical period, the energy which is stored in the resonant tank is not changed. And this means that the input energy of the resonant tank equals the output energy of the resonant tank, see (3.5). The input energy and the output energy are calculated with (3.3) and (3.4) respectively. If the switching frequency is increased, which causes an increased phase shift angle between V_{ab} and I_r. This leads to $E_{in}<E_{out}$, which leads to that the energy stored in the resonant tank decreases and the amplitude of resonant current decreases.

For phase shift control in steady state operation, the same principle applies,

when the phase shift angle varies, the input power of the resonant tank varies, thereby the energy that is stored in the resonant tank varies, and this leads to that the output power also varies.

$$E_{in} = \int_0^{t_1} (V_{dc} - V_{out}) \times I_r \, dt \tag{3.3}$$

$$E_{out} = \int_{t_1}^{t_2} (-V_{dc} - V_{out}) \times I_r \, dt \tag{3.4}$$

$$E_{in} = E_{out} \tag{3.5}$$

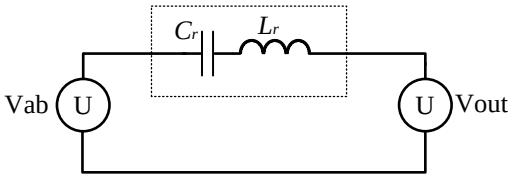


Figure 3.5 Simplified circuit of a resonant DC/DC converter

3.3 Proposed resonant auxiliary converter

The schematic circuit of the proposed resonant auxiliary converter is shown in Figure 3.6. Comparing to the resonant DC DC converter, the rectifier is replaced by three phase bidirectional switches and the output capacitors. The function of the proposed resonant auxiliary converter is providing an output filter free DC to AC conversion, galvanic isolation between input voltage and output AC voltage and omitting the redundant energy conversion stage to reduce components.

Similar to the proposed inductive link auxiliary converter presented in previous chapter, there are two energy conversions in the proposed resonant

auxiliary converter. The first energy conversion is from input DC voltage to high frequency AC current pulses. This is done by the resonant tank and the H-bridge. The second one, which converts the high frequency AC current pulses to three low frequency AC voltages, is done by the bidirectional switches and the output capacitors. The high frequency current pulses are selected by bidirectional switches to charge/discharge the output capacitors to form sinusoidal output voltages.

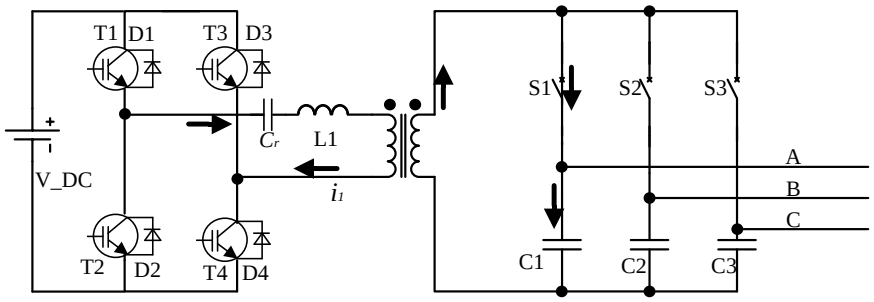


Figure 3.6 Proposed resonant auxiliary converter

Controlling the resonant current pulses is different from controlling the resonant current of the resonant DC/DC converter. See Figure 3.5, for the resonant DC/DC converter the excitation voltage over the resonant tank contains two parts: the converter output voltage and the output voltage of H-bridge. In steady state operation the converter output voltage can be considered as a constant voltage, and the input voltage is changing by phase shift control or frequency control, as stated in previous chapter.

For the proposed resonant auxiliary converter the output voltage is varying all the time and this introduce additional difficulties for controlling the energy of the resonant tanks.

3.4 Modulation and Control Algorithm

As stated in section 3.3, controlling the proposed resonant auxiliary converter has more difficulties than controlling the resonant DC/DC converter. The challenges are caused by the continuously changing output voltages of the converter and the connection between the resonant tank and the converter outputs which is switched between different output phases via

bidirectional switches. Between different switching period, the output voltages of the resonant tank is different from each other, in order to keep the energy stored in the resonant tank stable and to fulfill equation (3.5), the input voltage of the resonant tank have to change accordingly (the input voltage of the resonant tank is the output voltage of the H-bridge, and the output voltage of the resonant tank is the output phase voltages).

The output voltages of the H-bridge is $+V_{dc}$, $-V_{dc}$ and zero. Consider a condition which is shown in Figure 3.6. A positive current pulse is needed by phase A and the output voltage of phase A is larger than zero. First the transistor T1 and T4 shall be turned on. The current starts to increase from zero, during this time the voltage over the resonant tank is V_{dc}-V_{out}, and the energy that flows into the resonant tank is given by equation (3.3). After a while, at time t_1 in Figure 3.9 in order to keep the stored energy of the resonant tank stable, another voltage over the resonant tank shall be applied. Two different voltages can be applied by turning off either T1 and T4, or T1 only. These two voltages are $-V_{dc}$-V_{out} and -V_{out} respectively. Turn off T1 and T4 cause hard turned off of two transistors while Turn off T1 only requires one hard turn off. The switching time t_1 is chosen according to (3.5).

Series resonant circuit

In order to find the t_1 to fulfill the (3.5), it is necessary to investigate the series resonant L-C-R circuit. The series L-C-R circuit is shown in Figure 3.7. The capacitor voltage for a step voltage V_s with initial current i_o and initial capacitor voltage V_{cr} is given by [13].

$$i(\omega t)=\frac{V_s\text{-}V_{cr}}{\omega l}e^{-\alpha t}\sin(\omega t)+i_o e^{-\alpha t}\frac{\omega_o}{\omega}\cos(\omega t+\Phi) \tag{3.6}$$

$$V_c(\omega t)=V_s\text{-}(V_s\text{-}V_{cr})\frac{\omega_o}{\omega}e^{-\alpha t}\cos(\omega t\text{-}\Phi)+\frac{i_o}{\omega C}e^{-\alpha t}\sin(\omega t) \tag{3.7}$$

Where the $\omega^2=\omega_o^2(1\text{-}\zeta^2)=\omega_o^2\text{-}\alpha_o^2$, $\omega_o=\frac{1}{\sqrt{LC}}$, $\alpha=\frac{R}{2L}$, $\xi=\frac{R}{2\omega_o L}$, $\tan\Phi=\frac{\alpha}{\omega}$.

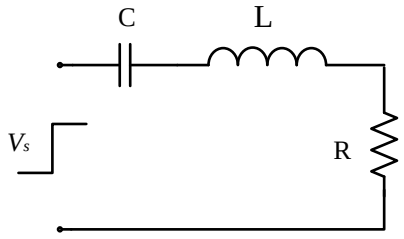


Figure 3.7 Series L-C-R circuit

Assuming the resistor R to be small and that it can be neglected, (3.6) and (3.7) can be rewritten as:

$$i(\omega_o t)=\frac{V_s-V_{cr}}{\omega_o l}\sin(\omega_o t)+i_o\cos(\omega_o t) \tag{3.8}$$

$$V_c(\omega_o t)=V_s-(V_s-V_{cr})\cos(\omega t)+\frac{i_o}{\omega_o C}\sin(\omega t) \tag{3.9}$$

At the beginning of each half cycle the initial value of i_o is zero (3.8) and (3.9) can be rewritten as

$$i(\omega_o t)=\frac{V_s-V_{cr}}{\omega_o l}\sin(\omega_o t) \tag{3.10}$$

$$V_c(\omega_o t)=V_s-(V_s-V_{cr})\cos(\omega_o t) \tag{3.11}$$

Energy balance of proposed resonant auxiliary converter

The voltage over the resonant tank is the converter output voltage plus the output voltage from the H-bridge. The converter output voltage is a 50 Hz AC voltage; during the one pulse period the converter output voltage can be considered as a constant voltage since variation of the voltage in one pulse period is small comparing to output voltage amplitude. The output voltage of the H-bridge has three values: V_{dc} , $-V_{dc}$ and 0. The combination of those three value results in variation of the H-bridge output voltages. The voltage transition between V_{dc} and $-V_{dc}$ results in a hard turn off of two transistors

and the voltage transition from either V_{dc} or $-V_{dc}$ to zero results in a hard turn off of only one transistor. In order to reduce the switch losses and the stress on the switches, the transition between V_{dc} and $-V_{dc}$ should be avoided.

To fulfill the equation (3.5), V_{ab} and V_{out} in Figure 3.8 shall have the same polarity which indicates that for example when the output voltage V_{out} is larger than zero, the voltage V_{ab} should be a combination of V_{dc} and 0. Calculation of the transition time t_1 in Figure 3.9 is the key. The initial state of the resonant capacitor defines the polarity of the current pulses. For example, the resonant capacitor initial voltage has a polarity that is as shown in Figure 3.8, the current pulse polarity is from the input side to the output side, after half the electrical period the resonant capacitor voltage has the same absolute value but the polarity has been changed, the next current pulse will have a reversed polarity.

Calculation of the voltage transition time t_1 is given here. Consider a general condition that is shown in Figure 3.8 and in Figure 3.9. At the initial state the polarity of the resonant capacitor voltage V_{cr} is shown in Figure 3.8. The current start to increase at t_0 when V_1 is applied over the resonant tank, and at t_1 the voltage over the resonant tank is transferred to V_2, The input energy and the output energy of the resonant tank can be easily calculated with (3.12) and (3.13), where A1 and A2 are the area that is covered by the current pulses before and after the transition time t_1.

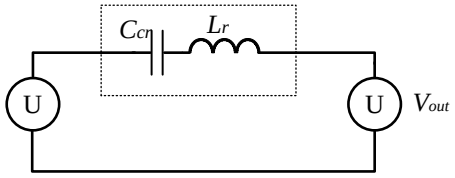


Figure 3.8 Simplified circuit of the proposed resonant auxiliary converter

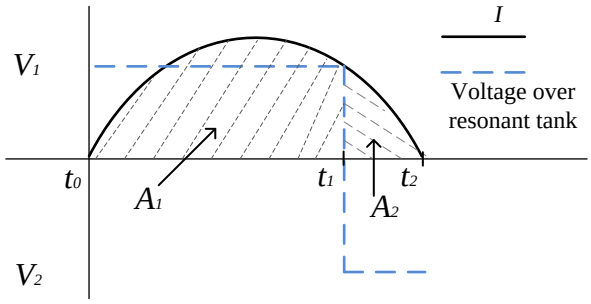


Figure 3.9 Current pulses of half the electrical period.

$$E_{in}=V_1 \times A_1 \tag{3.12}$$

$$E_{out}=V_2 \times A_2 \tag{3.13}$$

At t_0 the initial current of the resonant inductor is zero and the initial voltage of capacitor is V_{ci}. The resonant current between t_0 and t_1 can be given by (3.14)

$$i_t = \frac{V_1 - V_{ci}}{\omega_o l}\sin(\omega_o t) \tag{3.14}$$

The integration of i_t from t_0 and t_1 is given by (3.15) where $\theta_1$is given by $\omega_o t_1$

$$A_1=\int_{t_0}^{t_1}\frac{V_1 - V_{ci}}{\omega_o l}sin(\omega_o t)dt=\frac{V_1 - V_{ci}}{\omega_o^2 l}(1-\cos\theta_1) \tag{3.15}$$

After t_1 the voltage over the resonant tank is changed to V_2 and the initial condition of the resonant tank at t_1 is given by equation (3.16) and (3.17).

$$V_{t1}=V_1 - (V_1 - V_{ci})cos(\omega_o t_1) \tag{3.16}$$

$$i_{t1} = \frac{V_1 - V_{ci}}{\omega_o l}sin(\omega_o t_1) \tag{3.17}$$

Substitute (3.16) and (3.17) into (3.8) gives the current during the time

interval t_1 and t_2 as shown in equation (3.18).

$$i_t = \frac{(V_2 - V_1) + (V_1 - V_{ci})\cos(\omega_o t_1)}{\omega_o l} sin(\omega_o (t - t_1)) + \frac{V_1 - V_{ci}}{\omega_o l} \sin(\omega_o t_1)\, cos(\omega_o (t - t_1)) \tag{3.18}$$

The integration of i_t from t_1 and t_2 is given by (3.19) where θ_2 is given by $\omega_o t_2$.

t_2 is the time when the resonant current becomes zero. And the relation between t_2 with a given t_1 is given by (3.20)

$$A_2 = \int_{t_1}^{t_2} i_t dt = \frac{(V_2 - V_1) + (V_1 - V_{ci})cos\theta_1}{\omega_o^2 l}(1 - cos(\theta_2 - \theta_1) + \frac{(V_1 - V_{ci})}{\omega_o^2 l} sin\theta_1 sin(\theta_2 - \theta_1) \tag{3.19}$$

$$\tan(\theta_2 - \theta_1) = \frac{-(V_1 - V_{ci})sin\theta_1}{(V_2 - V_1) + (V_1 - V_{ci})cos\theta_1} \tag{3.20}$$

Substitute (3.19) (3.15) into (3.12), (3.13) and (3.5), the voltage transition time can be calculated together with (3.20). Solving such equations involves trigonometric functions is complicated!

For any given θ_1 there is a corresponding θ_2 that can be calculated by (3.20) in the interval [0, 180], and with this given θ_1 and calculated θ_2 the corresponding input energy and output energy of the resonant tank can be calculated by (3.15), (3.19), (3.12) and (3.13). If we chose all the possible θ_1 from 0 to 180 degree and calculate all the corresponding input energy and output energy of the resonant tank, there should be a pair of input energy and output energy that have the closest value to each other and fulfills (3.5). By using this method the solving of the equations with trigonometric functions is avoided. This method requires quite a lot computation resources and long computation time for the controller. A pre-calculated look-up table

is a good solution for this.

Look-Up Table

To generate the lookup table more details of the resonant behavior shall be investigated. According to (3.12), (3.13), (3.15), and (3.20) the input parameters for finding θ_1 and θ_2 are the DC-link voltage, the output voltage of the converter and the initial voltage of the resonant capacitor.

For the same resonant current direction, the direction of the energy flow depends on the polarity of the output voltages. For an output voltage with a polarity is shown in Figure 3.8, if the current pulse flows from the input H-bridge to the output, the energy is flowing from H-bridge to the output. The main operating curve is plotted in Figure 3.10. Transistor T1 and T4 and S1 is turned on at the beginning of the switching period, the voltage over the resonant tank is V_{dc} -V_o. The current starts to increase from zero, after a while when *t1* is reached either transistor T1 or T4 is switched off. During this time interval the voltage over the resonant tank is –Vo. The current becomes zero at the time t_2 and after t_2 the other transistors are turned off. In the case when the output voltage has a different polarity other than the case that is shown in Figure 3.8, with the same direction of the current pulse the energy is flowing from the load to the DC-link. In this case only one transistor of T1 and T4 is turned on together with S1 at the beginning, and the transistor T1 or T4 is turned off at *t1* and the current becomes zero at t_2, S1 is switched off at t_2.

In the case that the initial state of resonant capacitor is changed to another polarity, other than the case that is shown in Figure 3.8, the direction of current pulse is flowing from the load to the DC-link. Instead of turning on T1 and T4 to conduct the current pulse, the transistors T2 and T3 are involved. The main operating waveform of T2 and T3 is similar to T1 and T4.

To generate the look up table, the calculation of the input/output energy and the $\omega_o^2 l$ product vs θ_1 and output voltage is calculated and plotted according to Figure 3.12 and 3.13. Figure 3.12 is the case when the output voltage is larger than zero and Figure 3.13 is the case when the output voltage is smaller than zero. The input parameters are V_{dc}=750, V_c= 600 where V_{dc} and V_c are the dc link voltage, the initial voltage of the resonant capacitor

respectively.

The two curved surface is corresponding to the input energy and the output energy. The crossing line between these two curved surfaces is the line along which the input energy equals the output energy. The θ_1 and θ_2 which fulfills the (3.5) can be extracted from these crossing lines. Figure 3.14 shows the extracted θ_1 and θ_2 vs output voltages.

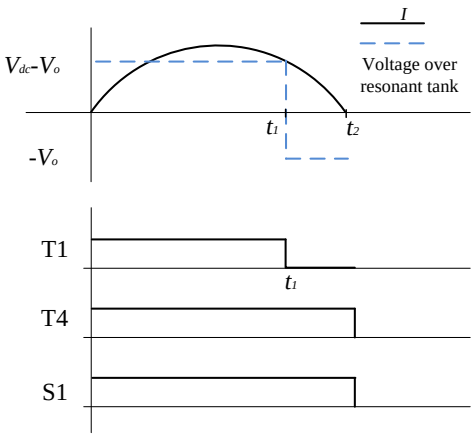


Figure 3.10 Operating waveform

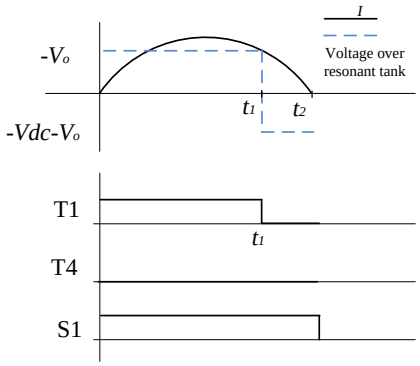


Figure 3.11 Operating waveform

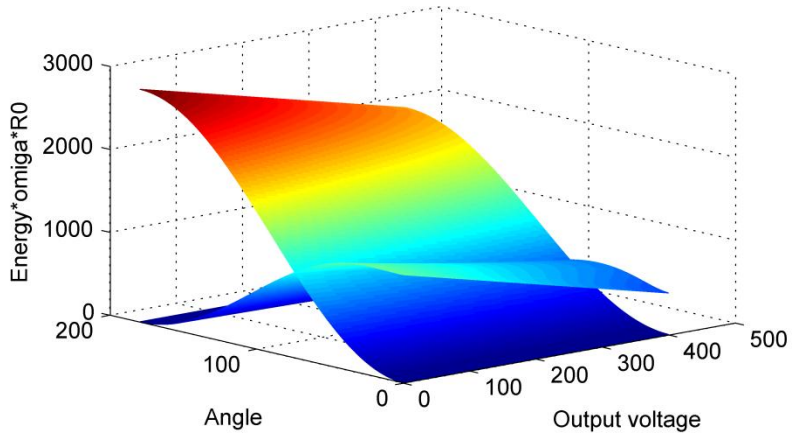


Figure 3.12 Input and output energy when output voltage is larger than zero

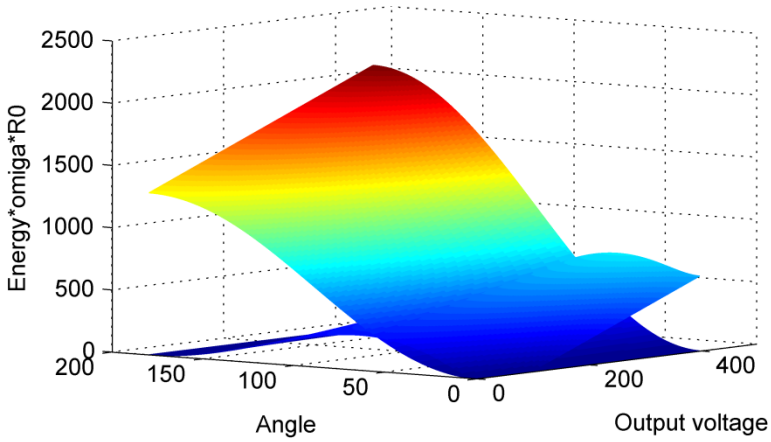


Figure 3.13 Input and output energy when output voltage is smaller than zero

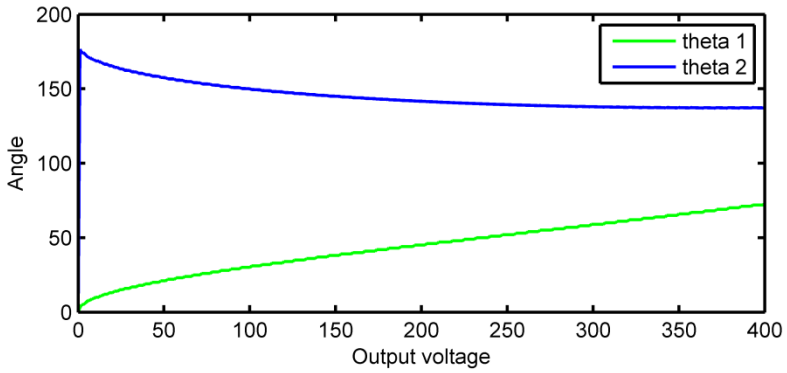


Figure 3.14a Extracted θ_1 and θ_2 (V_o>0)

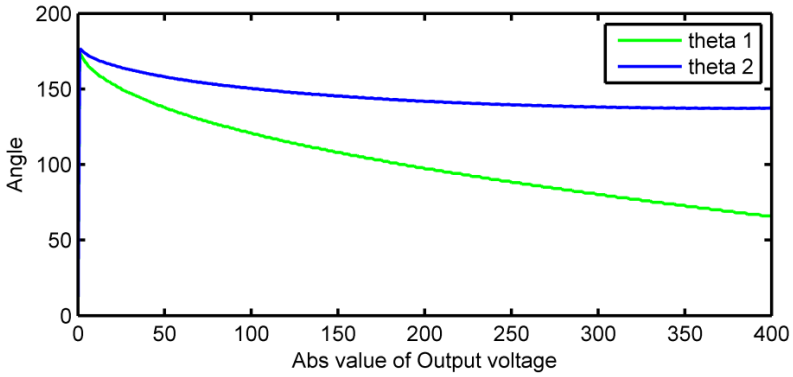


Figure 3.14b Extracted θ_1 and θ_2 (Vo<0)

In the case when the output voltage is larger than zero (Figure 3.14a), θ_1 is low when the output voltage is close to zero, and close to half of θ_2 when the output voltage is high. Higher output voltage cause higher energy to be delivered to the output in one switching period, and thus requires more input energy to compensate the energy loss of the resonant tank. Thereby θ_1 increases with an increased output voltage. When θ_1 is larger the transistor T1/T4 needs to turn off at a higher current peak.

In the case when the output voltage is smaller than zero. The output voltage is the source of input energy of the resonant tank in a half resonant cycle. When the absolute value of the output voltage is low, θ_1 has to be large to compensate the energy loss of the resonant tank. And θ_1 decreases to almost

half of θ_2 when the abs value of the output voltage is 400 V. In this case when θ_1 is close to θ_2 either transistor T1/T4 needs to turn off at higher current.

Stability investigation

The method that has been discussed in this section for finding θ_1 is based on the assumption that the amplitude of the voltage over the resonant capacitor is not changing between different electrical cycles. In reality the amplitude of the voltage over the resonant capacitor may vary, and it is important that, the control algorithm itself can push the amplitude of the resonant voltage back to the desired value when there are variations in the amplitude of the resonant capacitor voltage. In other words the control algorithm should be stable regarding to the controlling of the resonant energy inside the resonant tank. For example the initial value of the amplitude of the resonant voltage is zero at the initial state, the control algorithm shall have the ability that to increase the amplitude of the resonant voltage to the desired value after several pulse period. See Figure 3.15 for θ_1 vs output voltage and the amplitude of the resonant capacitor voltage. For the same output voltage, as shown in Figure 3.15, with increased capacitor voltage, the angle θ_1 is also increased. In other words, a higher resonant capacitor voltage requires higher input voltage to fulfill (3.5).

For each current pulse, the charge delivery ability can be calculated with (3.19). With increased resonant voltage, the charge delivery ability is also increased. This requires more energy in order to deliver more charge. If the charge is delivered from input DC-link to the output side which corresponds to Figure 3.15a, θ_1 shall be larger than before to deliver more energy to the output side. If the charge is delivered from output to the DC-link, $\theta_1$shall also be larger to deliver more energy back to the DC-link side. To fulfil (3.5) θ_1 has a positive coefficient with the resonant voltage.

This is a very nice feature: for example at the initial state of the converter, the amplitude of the resonant voltage is zero, if the look-up table is made based on the assumption that the resonant voltage is 600 V, for the first several periods, the $\theta_1$does not fulfill (3.5) and $E_{in}>E_{out}$, and this situation will continue until the desired resonant capacitor voltage is build up to the desired value. It is also helpful to reduce the requirement for monitoring the resonant voltage of the resonant capacitor. The control method itself, as we

have mentioned, can ensure that the resonant voltage comes back to the desired value. In other words, the accuracy of the voltage sensor of the resonant capacitor is not important, only the polarity of the resonant voltage is needed.

$$Q_d=2CV_{ini} \tag{3.19}$$

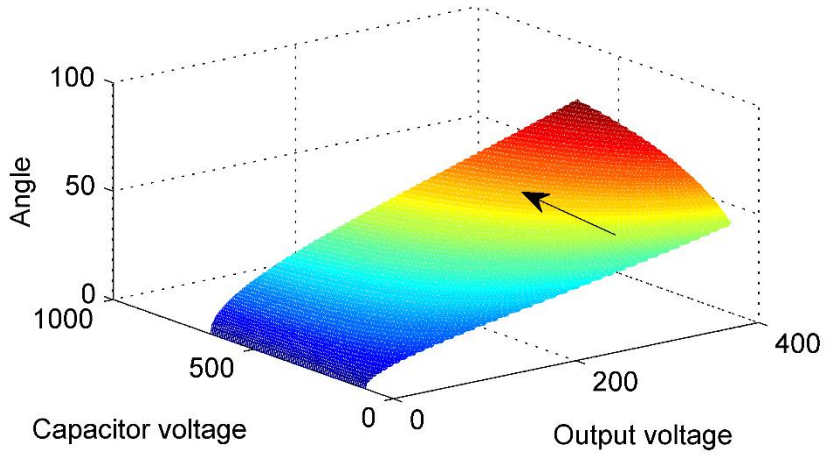


Figure 3.15a θ_1 vs output voltage and resonant voltage

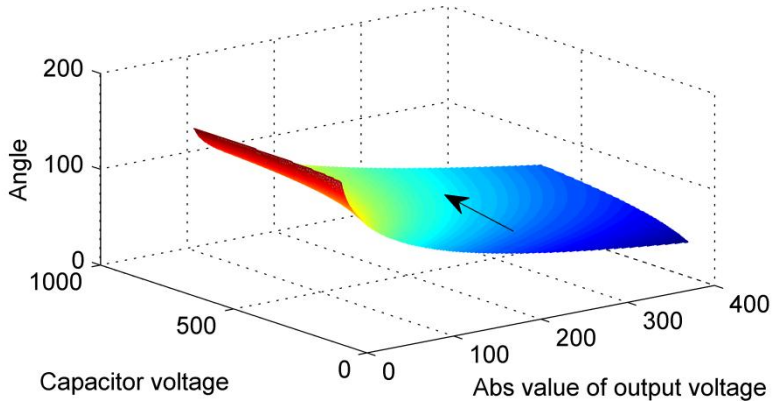


Figure 3.15b θ_1 vs output voltage and resonant voltage

Based on the discussion in this section, the input data for generating a lookup table are, the DC-link voltage, the amplitude of the resonant capacitor voltage and the output voltage range. The outputs are 1-D

s of θ_1 and θ_2 vs output voltages. It does not need the details of the parameters like the capacitance of resonant capacitor and resonant inductance which gives a large freedom for setting the parameter of resonant components.

Parameters of passive components

The selection of output capacitor is similar to the proposed hard switched auxiliary converter. The value of output capacitor can be calculated by using (2.10)

The capacitance of resonant capacitor is related to the charging carry ability according to (3.19). Substituting (2.9a) and (2.9a) into (3.19) gives the capacitance of resonant capacitor

$$C_{ron} = \frac{P_{max}}{\sqrt{2} V_{rms} F V_{ini}} \tag{3.20}$$

Here P_{max} ,V_{rms}, V_{ini} F are maximum output power, rms value of output voltage, the amplitude of resonant capacitor voltage, and the pulse frequency respectively.

The value of resonant inductor can be calculated by

$$\omega_0^2 = \frac{1}{C_{ron} L_{ron}} \tag{3.21}$$

One current pulse period corresponding to half resonant period, then (3.21) can be rewritten as

$$L_{ron} = \frac{1}{C_{ron} F^2 \pi^2} \tag{3.22}$$

Here F is the current pulse frequency.

Control algorithm and discussions

The controlling method from the proposed inductive link auxiliary converter could be adapted for controlling the proposed resonant auxiliary converter. The same carrier wave, same modulation method, and fast computer control can be inherited from the proposed inductive link auxiliary converter.

Different from the proposed inductive link auxiliary converter, the flexibility of the polarity of current pulses are limited due to the property of the resonant circuit. There is always a negative current pulse followed by a positive current pulse. The polarity of current pulses is defined by the initial polarity of the resonant capacitor voltage. An additional voltage sensor or polarity monitor is needed for monitoring the polarity of resonant capacitor voltage to decide the polarity of the current pulses. This feature that the two adjacent current pulses must have opposite polarity, requires symmetrical load on the output side.

The control flow chart is shown in Figure 3.16. It starts by measuring the current state of the converter: voltage references, output voltages and polarity of the resonant capacitor voltage. Based on these measured data, the polarity of next current pulse and which output phases that should receive the current pulse can be decided.

There are three output phases, but only one output phase can be charged/ discharged by the current pulse at a time. Each output phase voltage is compared to its reference voltage. The output phases that require a current pulse that has the same polarity as the next current pulse will be the candidates. If there is more than one candidate, the one that has the largest voltage error has the highest priority. To avoid over charging and to reduce losses, if all voltage errors are smaller than the predefined voltage band, none of these three output phases will be charged.

The output voltage of the selected outputs and the polarity of the resonant capacitor voltage are sent to the lookup-table to calculate the duty ratios of the transistors. The calculated duty ratios of the transistors are applied to the transistor at the beginning of the next switching period.

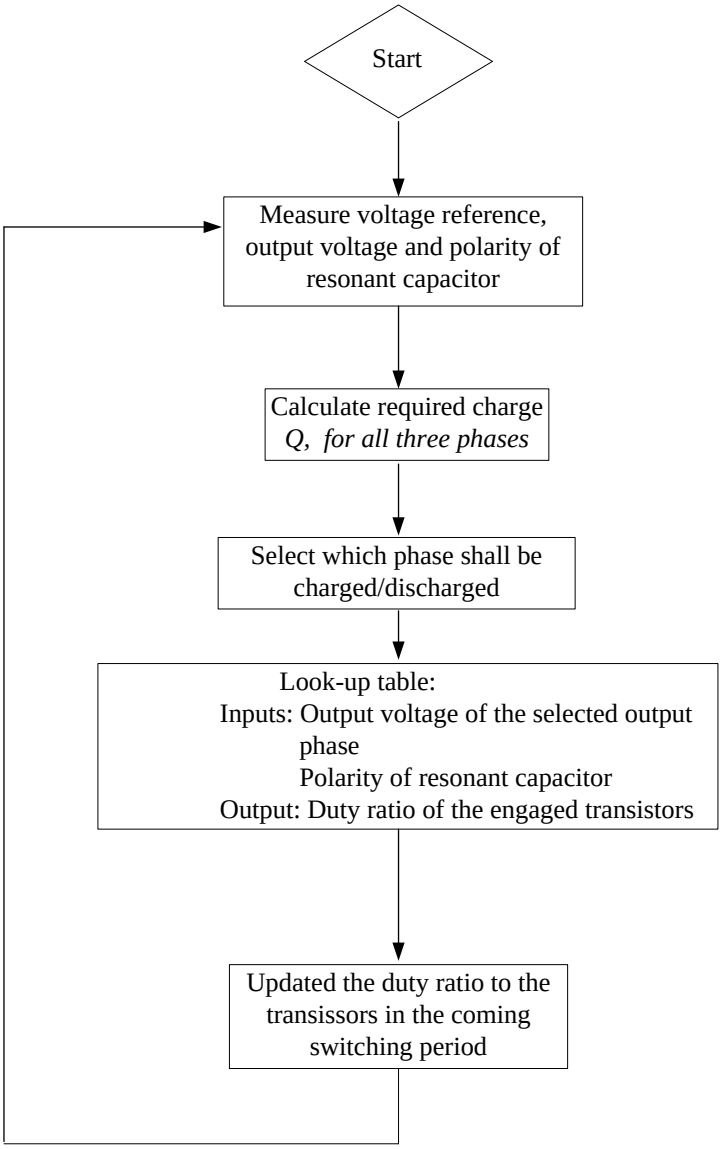


Figure 3.16 Control loop of resonant auxiliary converter

3.5 Simulation

Simulations are done to verify the energy balance theory of the resonant auxiliary converter and to develop the control algorithm for converter prototypes. All the simulations are done in LTspice. Figure 3.17 shows the simplified simulation model.

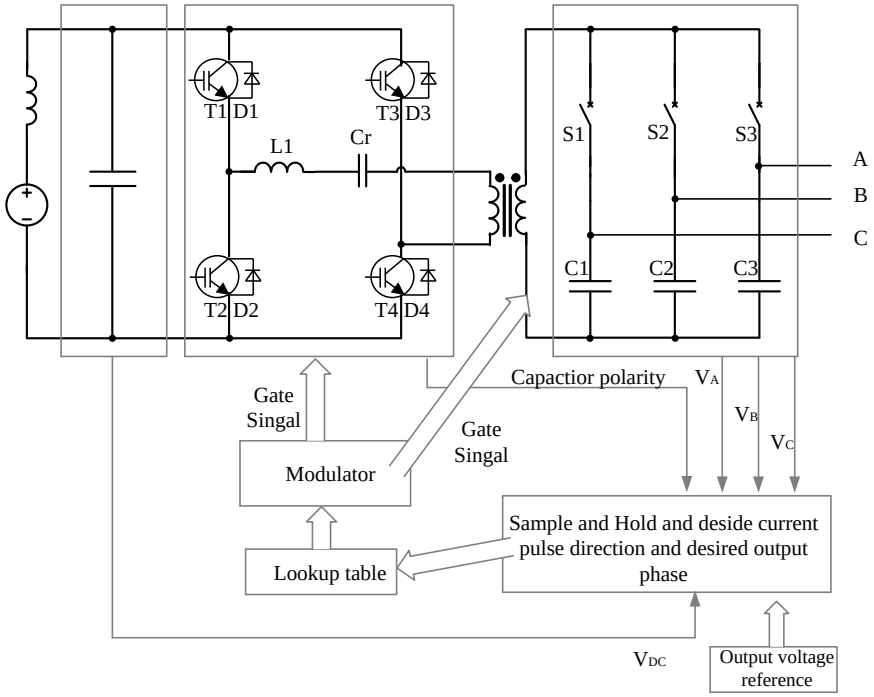


Figure 3.17 Simplified simulation model

The switches T1 to T4 and S1 to S3 are ideal switches. The diodes D1 to D4 are ideal diodes. Note that the load is not included in this circuit, it is formed by three sinusoidal current sources that are connect to nod A, B and C. The amplitude and phase are adjustable to simulate different load conditions.

The output capacitor in this simulation model is also an ideal component. The value is defined by (2.9) which is developed in section 2.3. The

parameter of the transformer that is used in the simulation is from an HF transformer from an auxiliary converter. The resonant inductance is formed by the leakage inductance of the transformer and an ideal inductor L1. The resonant capacitor is an ideal capacitor with the value that is calculated by (3.20)

Pulse frequency is set to 20 kHz. One current pulse occupy one pulse period which means the resonant frequency equals to 10 kHz. The output capacitor is selected to 768 μF.

Simulated resonant voltage

The voltage will be built up to the desired value after several half resonant periods due to the feature of the control algorithm we have discussed in section 3.4. The initial resonant voltage is zero, and in the first several pulse periods before the resonance capacitor voltage reaches its desired value, the input energy of the resonant circuit is higher than the output energy of the resonant circuit. The excess energy is stored in the resonant circuit and the voltage of the resonance capacitor is increased. When this voltage reaches its desired value the input energy is equal to the output energy of the resonant circuit, and the amplitude of the resonance capacitor voltage is stable. Figure 3.18 shows the simulated resonance capacitor voltage.

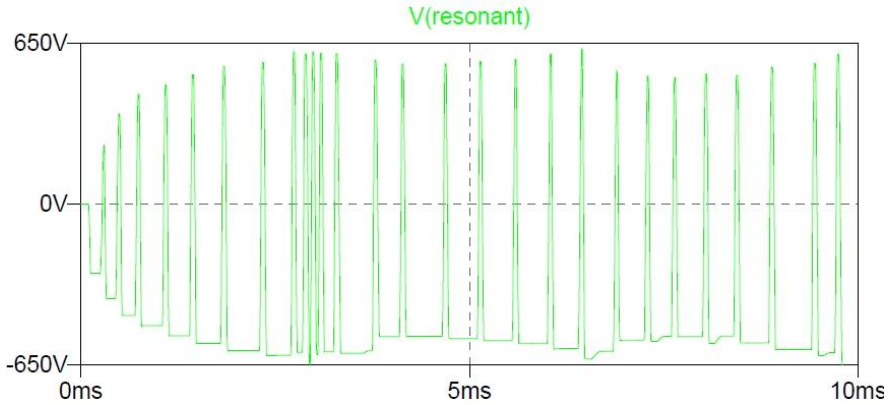


Figure 3.18 Simulated resonance capacitor voltage

Simulated Current Pulse

The current pulses are charge carriers. It transfers energy between inputs and outputs. Similar to the inductive link version of the proposed auxiliary converter the amplitude of the current pulses are high, and the transistor may need to switch off at high current. As stated in section 3.4, when the output voltage is high, the transistor has to switch off at high current. Figure 3.19a and 3.19b shows a current pulse when the corresponding output voltage is 195V and -302 V respectively. At high output voltages, the current pulse are more like a triangle rather than sinusoidally shaped!

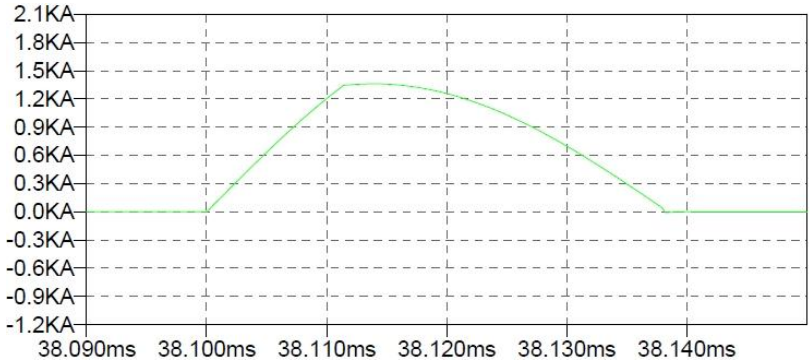


Figure 3.19a Current pulse when output voltage is 195V

Figure 3.19b Current pulse when output voltage is 302V

At low output voltages the current has a sinusoidal shape and the transistor

is turned off at low current as stated in previous section. Figure 3.20a and 3.20b shows the simulated current pulse when output voltage is low.

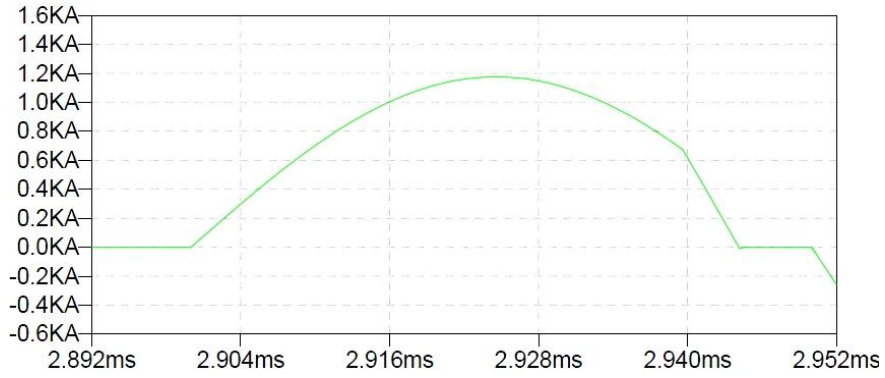


Figure 3.20a Current pulse when output voltage is -77V

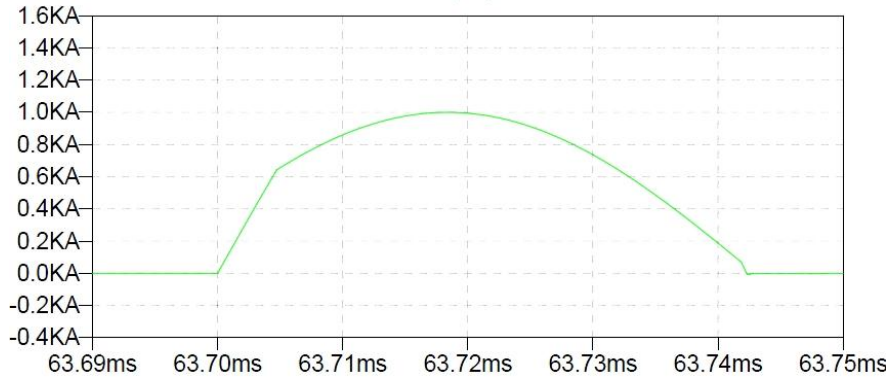


Figure 3.20b Current pulse when output voltage is -63V

Simulated output waveforms

The output waveforms are similar to the output waveform of the proposed hard switch auxiliary converter. In no load conditions, the output wave form has a staircase wave form. In the case of an inductive link auxiliary converter, the depth of the staircase varies due to the charge *Q* which is

carried by the current pulse varies between Q_{max} *and* Q_{min}. The value of Q_{max} and Q_{min} also varies with different output voltage. In the proposed resonant auxiliary converter, the charge Q which is carried by the current pulse is the same for all current pulses. Thereby the depth of the staircase is not changed. Figure 3.21 and Figure 3.22 show the output waveforms and harmonics respectively. In frequency domain, the harmonics are mainly below 10 kHz and the peaks are located below 3 kHz, but there are also harmonics around the current pulse frequency 20 kHz. Unlike the proposed hard switched auxiliary converter, there are no significant harmonics around one third of current pulse frequency since the modulation methods are different from each other.

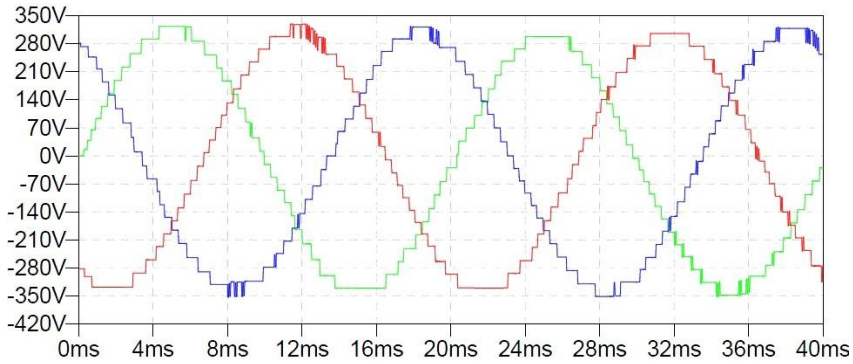


Figure 3.21 No load output waveform

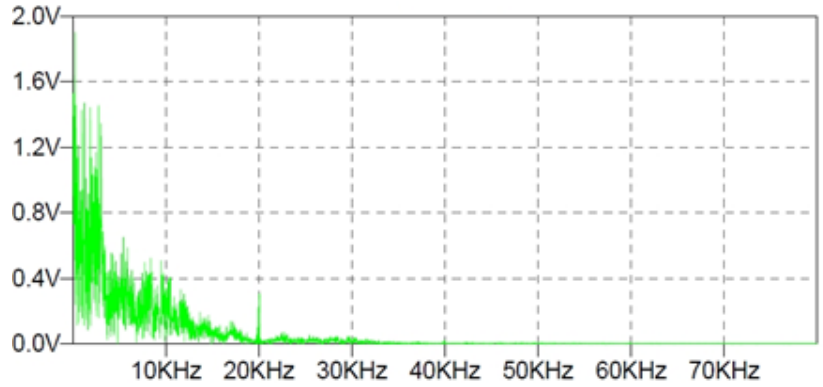


Figure 3.22 No load harmonics

Figure 3.23 and Figure 3.24 show the output waveform with a 100 kW resistive load. Similar to the no load case, in frequency domain, there are no significant harmonics with a fundamental frequency of one third of current pulse frequency.

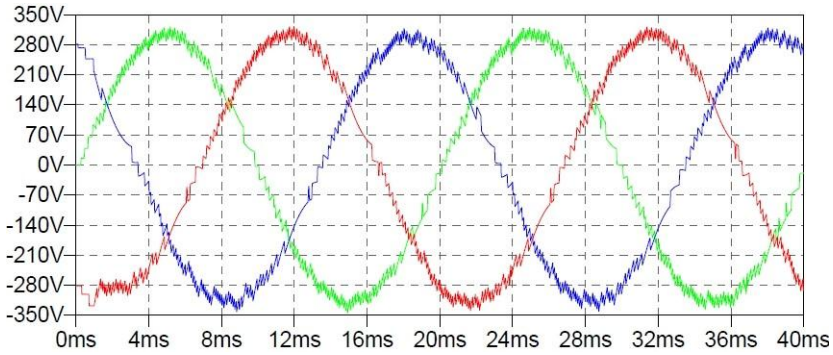


Figure 3.23 Output waveform with 100 kW resistive load

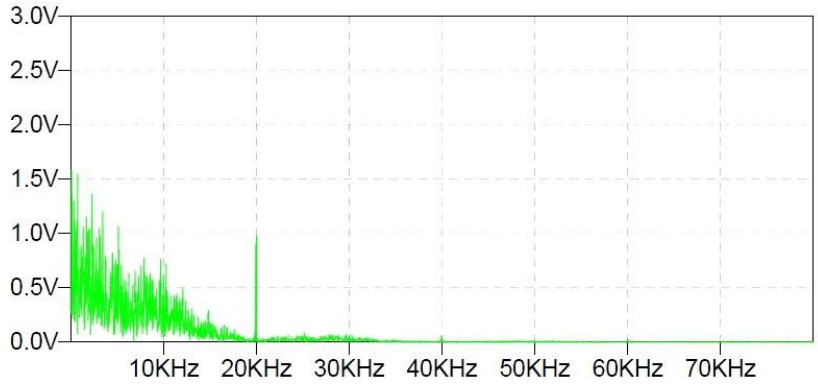


Figure 3.24 Harmonics with 100 kW resistive load

Unbalanced load

It is quite often that the loads are not symmetrical. It is important to know the behavior of the proposed resonant auxiliary converter under unbalanced

load conditions. In this proposed converter, two adjacent current pulses have opposite polarity, with symmetrical loads, the number of required positive current pulses approximately equals to the number of required negative current pulses. With unsymmetrical loads the balance between the positive and negative current pulses are broken, there is a risk that one or more of the output phases are not charged as it should be and the voltage cannot follow the voltage reference. In the following simulations unbalanced loads are introduced, and the output waveforms are plotted. Figure 3.25 and Figure 3.26 shows the output waveform with 5% unbalance in one output phases. With 5% unbalance in one output phase, there is a slight voltage mismatch in the phase with green color.

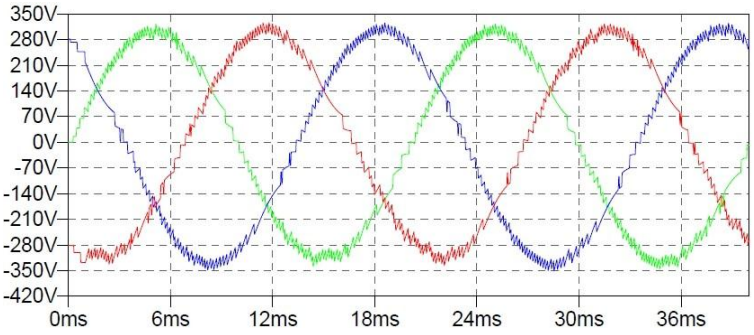


Figure 3.25 Output waveform with 24.5 kW(green), 23.3 kW and 23.3 kW resistive load

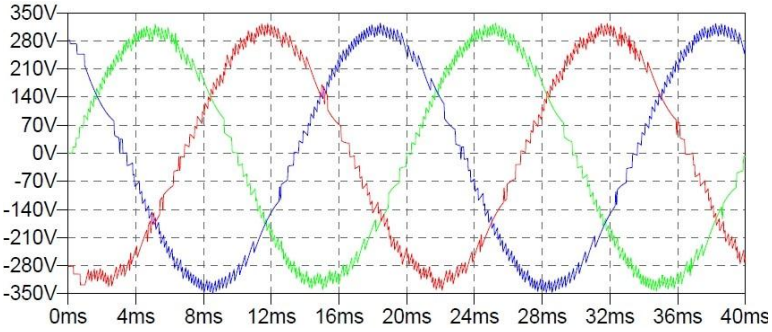


Figure 3.26 Output waveform with 22.2 kW(green), 23.3 kW and 23.3 kW resistive load

Figure 3.27 and Figure 3.28 show the output waveform with 10% unbalance

in one output phase. With the case where the output power of the phase with green color is 10% lower than the other two phases, the output voltage of the phase with blue color has a voltage error about 100 V around 8 ms and 28 ms. In the case of Figure 3.28 there are voltage errors in phases with green and blue color.

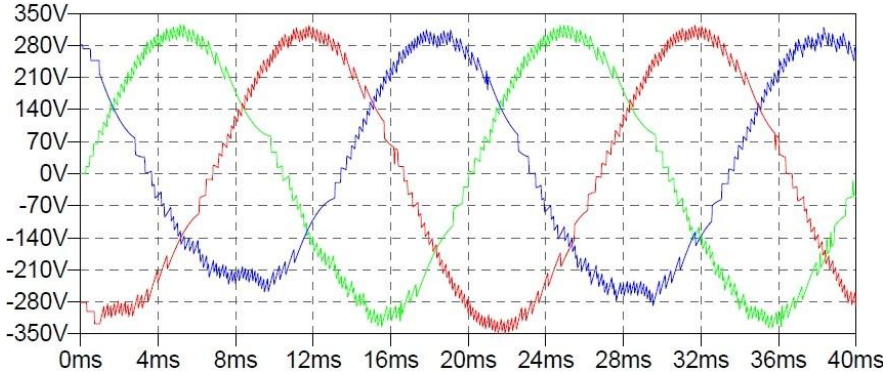


Figure 3.27 Output waveform with 21 kW(green), 23.3 kW and 23.3 kW resistive load

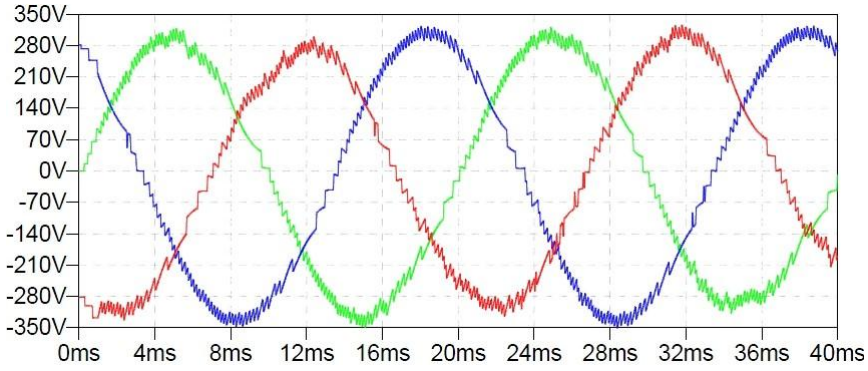


Figure 3.28 Output waveform with 25.7 kW(green), 23.3 kW and 23.3 kW resistive load

When there is a mismatch in all three channels, as shown in Figure 3.29 and Figure 3.30, with 5% output power variation there is a slight voltage distortion in the phase with red color. With 10 % more output power variation on the green phase and 10% less output power on blue phase. The

voltage distortion in the phase with red color is increased.

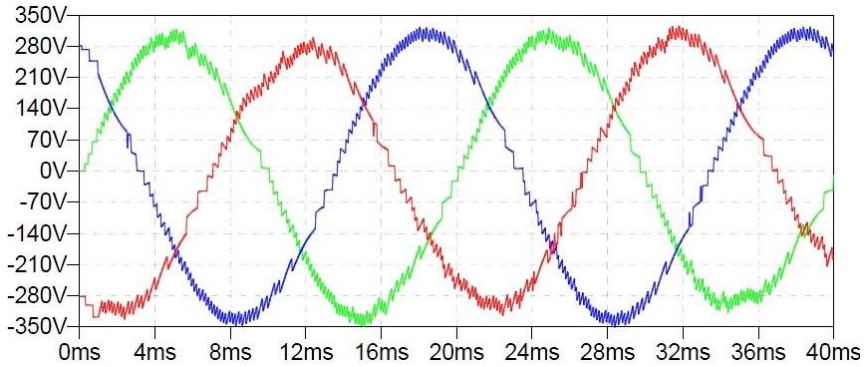


Figure 3.29 Output waveform with 22.2 kW(green), 24.5 kW(blue) and 23.3 kW resistive load

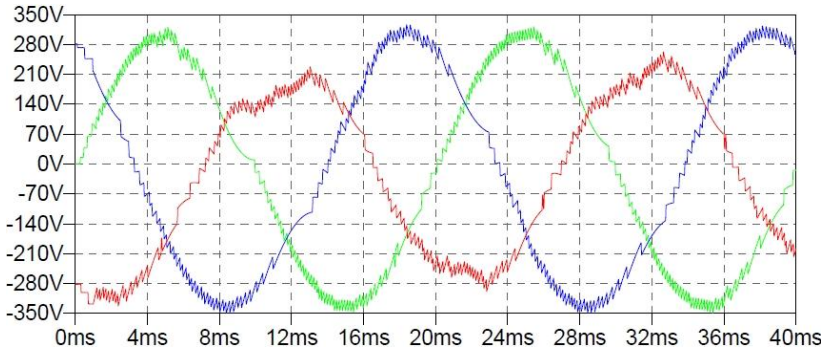


Figure 3.30 Output waveform with 25.7 kW(green), 21 kW(blue) and 23.3 kW resistive load

3.6 Summary

In this chapter, a control concept for control of the proposed resonant auxiliary converter is thoroughly investigated. The calculation of passive components values is given. Methods for generating current pulses and modulation method are investigated. The control algorithm is given and is implemented in LTspice. The simulated output voltages are sinusoidal shaped with very low amount of harmonics.

Chapter 4
Prototype development

This chapter focuses on the design and implementation of the proposed auxiliary converter. Due to limited project time only the inductive link auxiliary converter is designed and validated in the lab. The converter prototype design is divided into two steps, the first step is to develop the control software based on a down scaled single phase inductive link auxiliary converter. With the down scaled single phase version the control algorithm is validated. The second step is the development of an 80 kW three phase converter prototype based on the findings and the software from the first step.

4.1 First prototype

The purpose of the design and the implementation of the first prototype is to validate the concept of generating the sinusoidal voltage output wave form by using discrete current pulses, and to develop the control software of the proposed inductive link auxiliary converter. The galvanic isolation may not be needed or is not interesting in this down scaled version. In order to reduce the system complexity a single output phase might be good enough for validating the charging concept.

The down scaled version of the proposed hard switched auxiliary converter is implemented as in Figure 4.1, which shows the power electronic main circuit of this first prototype. Table 4.1 and 4.2 show the parameters of the converter prototype. Note that only one output phase is implemented in the this prototype, but the control software and all the analog I/O, digital I/O prepared for a three phase auxiliary converter.

Converter components

An output birdirectional switch is formed by two series connected IGBTs, of which one connected in reverse direction as shown in Figure 4.1. To simplify the complexity of the control circuit and the control algorithm, these two IGBTs are controled with the same gate control signal, the IGBTs are thereby turned on and off at the same time regardless of the direction of the current flow through them.

The inductance of L_1 in Figure 4.1 can be calculated by using (2.12). In this design the inductance is selected to 27 µH. For a 27 µH power inductor, if the volume is not critical, the easiest way is to use an air coil. By using an air coil the selection procedure of inductor core material can be avoided and the inductance is independed of bias current and frequency.

The capacitance of the output capacitor C_1 can be calculated by using (2.9). In this prototype the capacitance is selected to 0.35 mF. Five 70µF AC power capacitors are connected in parallel to form the 0.35 mF output capacitor.

Table 4.1 Prototype parameters

DC link voltage V_DC	300 V
Maximum power	2.3 kW
Switching freq.	20 kHz
Output voltage	115 Vrms

Table 4.2 Key components of the prototype

Output capacitor C1	0.35 mF
Inductor L_1	27 µH
Bidirectional switch S1	50MT060WHTAPBF
H-Bridge (T1 to T4)	FS150R12PT4

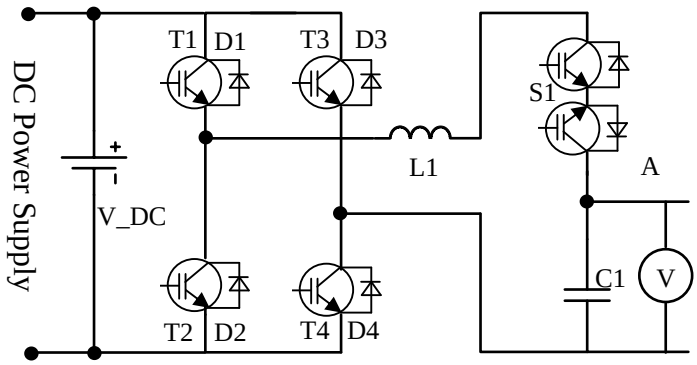


Figure 4.1 Power electronics main circuit of the first prototype

Control algorithm

The control algorithm which has been discussed in chapter 2 is implemented with Labview graphic programming language on the National Instruments CompactRIO cRIO-9022 system. The control algorithm is implemented in a Field-programmable gate array (FPGA).

The scheme for the implementation of the control strategy by using FPGA is shown in Figure 4.2. As discussed in Chapter 2, the converter control algorithm is a direct voltage control: The measured output voltages are compared with the internal voltage references, the semiconductor duty ratio is calculated based on the voltage errors. The control strategy is designed for a three phase inductive link auxiliary converter even though only one output phase is connected in the system.

The three output capacitors are charged alternatively, each output capacitor should be charged once in every 3 pulse periods. This is done by using a phase selector. The output of the phase selector is changing alternatively from 0 to 2 for every 3 pulse periods. The value 0, 1 and 2 means that the current pulse period is dedicated to phases A, B and C respectively, it guarantees that each output phase is charged only once in every three pulse period.

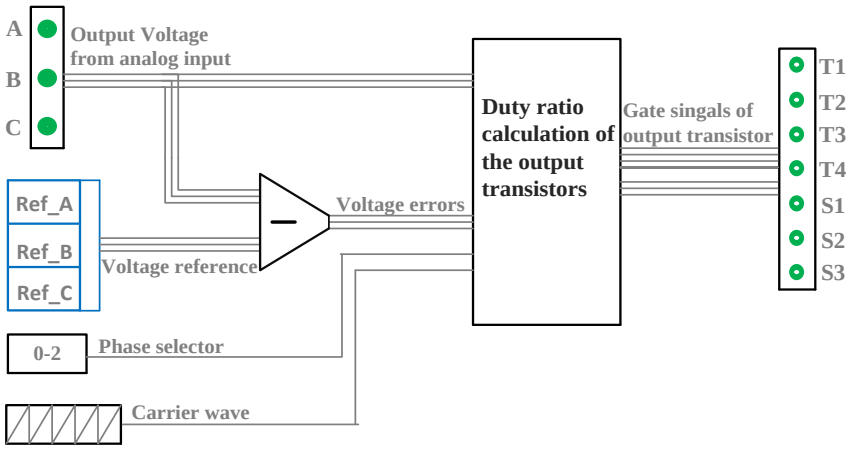


Figure 4.2 FPGA implementation of the control in hard switched auxiliary converter

The duty ratio of the output transistors is calculated based on the method and the equations which are described in chapter 2. As stated in chapter 2 the control shall be fast, and the calculation time shall be much shorter than the switching frequency period time.

The carrier wave is a saw tooth signal with positive slope. In the CompactRIO cRIO-9022 system the clock frequency is 40 MHz, the saw tooth period is defined as 2048 clock periods which corresponds to a 19.5 kHz current pulse frequency.

Figure 4.3 Lab setup

Measurements

The first interesting thing to investigate is how fast the FPGA is. In this prototype the calculation time is measured as 268 clock periods in the CompactRIO cRIO-9022 system which is approximately one eighth of the switching period. This is really a great feature.

Another important thing to look into is the output waveforms. The no load and the resistive load (25 ohm) output wave form are shown in Figure 4.4 and Figure 4.5 respectively.

The no load output waveform as shown in Figure 4.4 has a shape like a sinusoidal waveform with stair steps. These stair steps are caused by the charging pulses sent into and taken out of the output capacitor. In the output waveform which is shown in Figure 4.5, the stair steps are replaced by saw tooth signals, the reason for this is that the output capacitor voltage is not only affected by the current pulses but also by the load current. Comparing with the corresponding simulation from Chapter 2, the measured result and the simulated wave form agree with each other. This validates the idea of forming the sinusoidal with discrete current pulses.

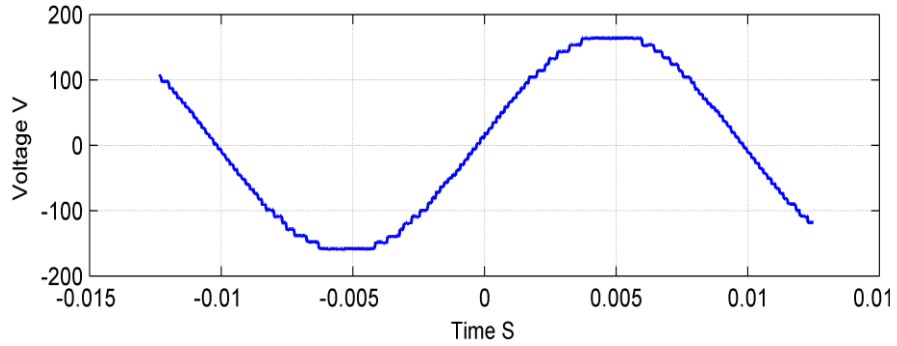


Figure 4.4 Measured no load output voltage

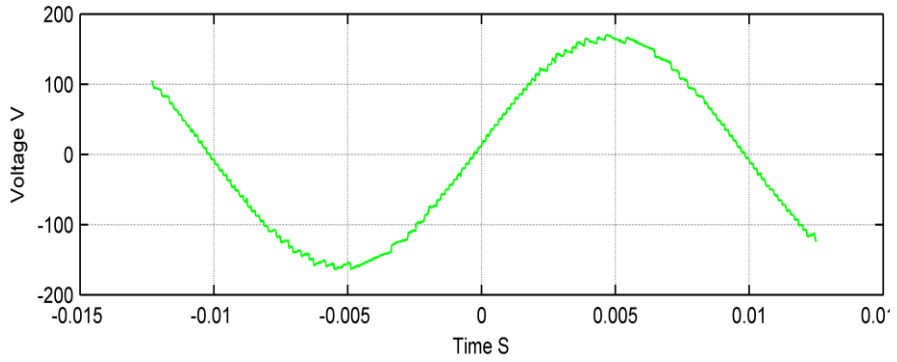


Figure 4.5 Measured output voltage with 25 Ω resistive load

4.2 Three phase prototype with increased power

The control software which is developed for the first converter is a good base for building a new prototype with all three output phases. The target is to build a power auxiliary converter in 100kW range with galvanic isolation between input and output.

Lab Setup

The main purpose of this first prototype is to validate the concept of a new auxiliary converter topology and to study how to design this type of converter. The prototype is not optimized either for efficiency, power density or EMC etc. The functionality is more important than an optimized

design. Lots of components (HF transformers JFETs, output capacitors etc.) are borrowed from previous projects to speed up the project.

A prototype with similar parameters as we have discussed in chapter 2 is presented in this chapter. Figure 4.6 shows the schematic of the lab-setup. The inverter was intended to be equipped with silicon carbide JFET semiconductor switches from Semisouth in USA. However, this company stopped their production, and it was not possible to receive the requested number of components from them. Instead we managed to get some JFET components from Infineon, but not the sufficient number.

Two silicon IGBTs are connected in series, one in reverse direction, to form an output bidirectional switch. These two IGBTs share the same gate signal from the CompactRio and they are switched on and off at the same time regardless the current pulse polarity. In the input H-bridge the transistors have to be turned off at high peak current which introduces high switching losses. The SiC JFET transistors are used here to reduce the switching losses. The output bidirectional switches are operating at zero current switching conditions and the switching losses can be neglected comparing to the conduction losses.

The HF transformer has a leakage inductance of 5.8 µH and 1 mH magnetizing inductance. The ratio is 1:1 and the rated power is 600 kW.

The inductance of inductor L_1 is formed of two parts: the leakage inductance of the transformer in series with two parallel connected 8 µH air core inductors (3.5 µH in total). The inductance of the inductor L_1 is 9.3 µH in total. Each output capacitor is a power capacitor bank with a total capacitance of 0.823 mF.

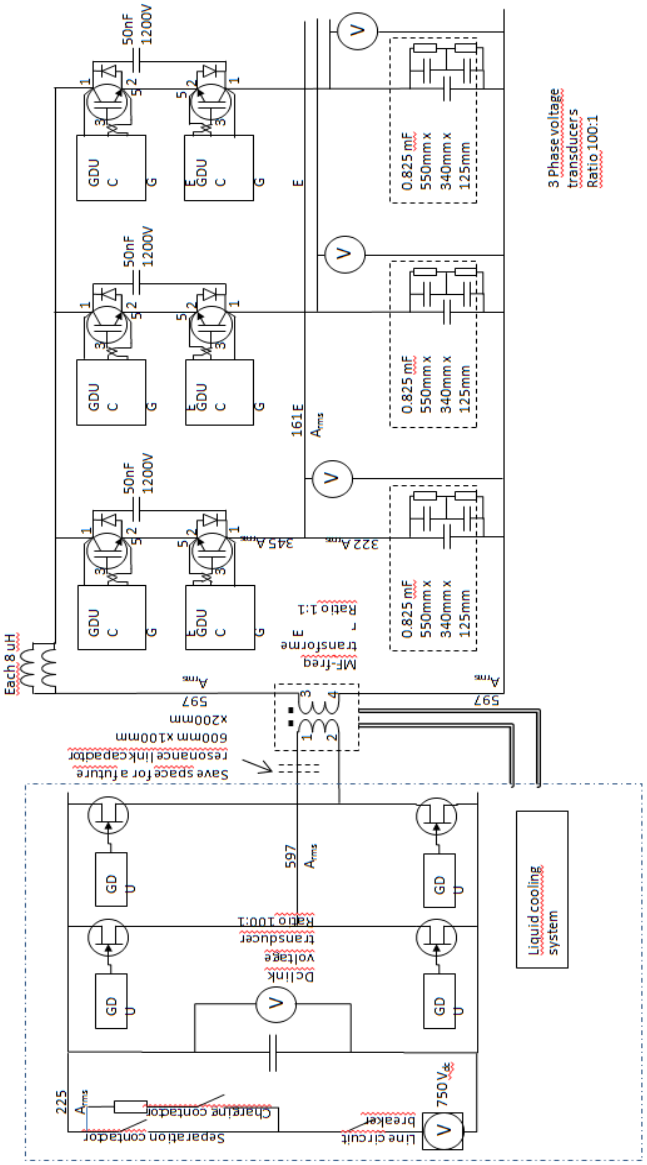


Figure 4.6 Schematic of Lab setup

The voltage sensor is a conventional voltage transducer with an unshielded current to voltage conversion board. This type of circuit has been proven to work in the first prototype. However, it did not work in this test setup, lots of noise is received by the analog input side of the controller and the output voltage cannot be measured correctly. To solve this problem three differential probes are used to measure the output voltage and the gain is set to 100:1. This should be regarded as a temporary solution, in future work, properly shielded voltage sensor shall be used and the cable of the sensor shall be kept as short as possible.

The main power supply is not shown in Figure 4.6. The main power supply is a variable three phase transformer followed by a rectifier, the power rating of the transformer is around 50 kW. This is the limitation of the maximum power we can run in this test setup.

A 1200 V 50nF snubber capacitor is connected in parallel over each bidirectional switch to protect it from over voltage.

The parameters of the prototype are shown as below:

- Dclink voltage 460-611 V
- Ac voltage U_{rmsLN} 230 V
- Fundamental frequency 50 Hz
- Switching frequency 10 kHz

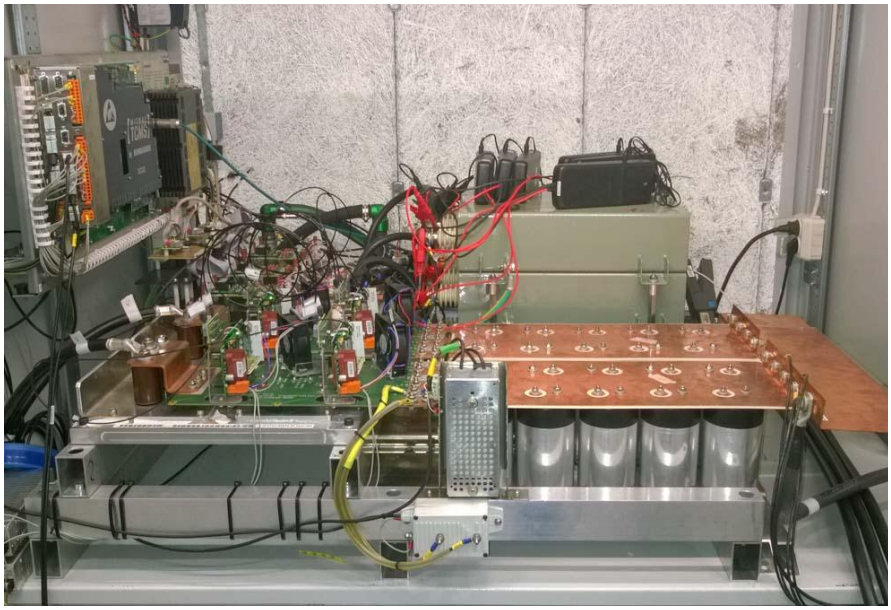


Figure 4.7 Lab setup of the 3-phase auxiliary converter prototype

Figure 4.7 shows the proposed hard switched auxiliary converter, the HF transformer and the inductor are not shown in the figure. They are located in the cooling circuit just below the converter desk.

Experimental measurement

The output power is limited by the DC power supply which has rated power of 50kW. To reduce the risk of semiconductor failure, the DC link voltage is selected maximum 610 V rather than 750 V. The measurement is done by a DEWE/DEWESOFT system. Figure 4.8 and Figure 4.9 show the measured no load output voltage in time and in frequency domain. The voltage in phase U is slightly higher than phase W and V. The reason of the voltage unbalance is that the differential probe used in phase U is not properly calibrated. This differential probe was replaced by a calibrated one in later measurements.

Compare the measured result with the simulation in Figure 2.14 the depth

of the stair case step (ripple voltage) of the measured curve is much smaller than the simulated result for the similar size of output capacitors. The root is that in the lab setup the DC-link voltage has a maximum value of 610 V instead of 750 V; which is used in the simulation. A reduced dc-link voltage causes reduced charge content in the current pulses.

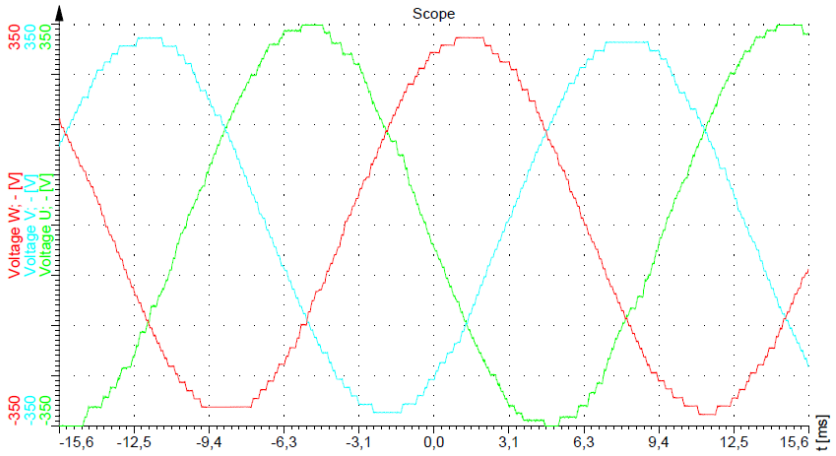


Figure 4.8 Measured no load output voltage waveform

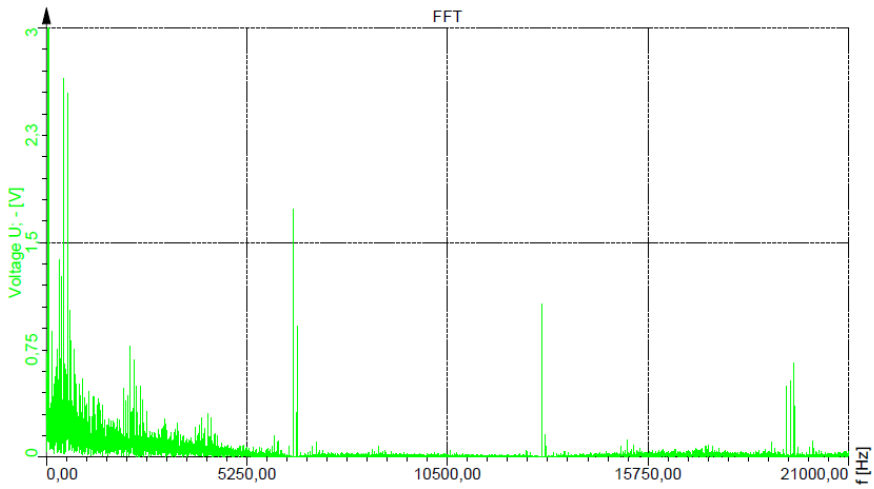


Figure 4.9 Measured no load output voltage harmonics

The power supply is a variable 50 Hz three phase transformer and a rectifier, the voltage varies with different loads. For the measurements shown in Figure 4.8 and 4.9 the DC link voltage is measured to 566 V. At 10 kW load (Figure 4.10 and 4.11) and at 30 kW load (Figure 4.12 and 4.13), the DC link voltage is measured to 540 V and 462 V respectively. At 30 kW load, due to the too low DC link voltage, the output voltage is not a pure sinusoidal. At 50 kW resistive load (Figure 4.14and 4.15), the transformer is adjusted to the DC link voltage 611 V. With this increased DC link voltage, even with an increased output power to 50kW, the quality of output voltage is increased compared with the 30 kW load case.

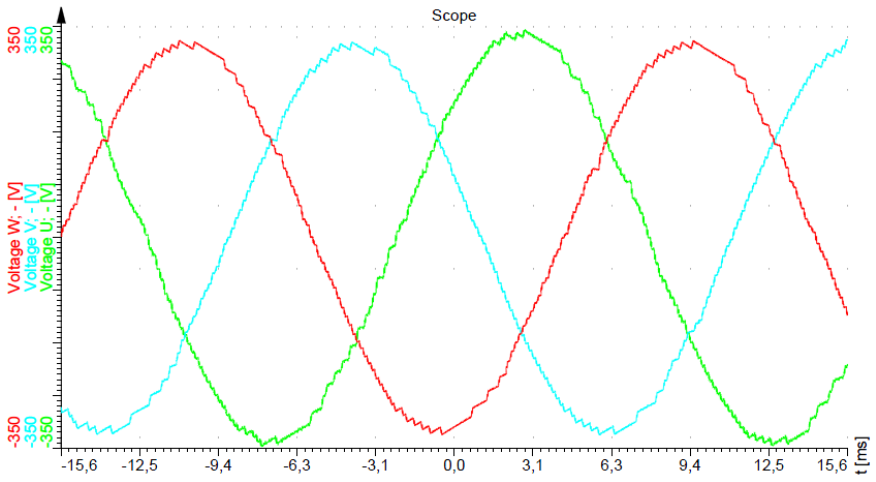


Figure 4.10 measured waveform with 10 kW resistive load

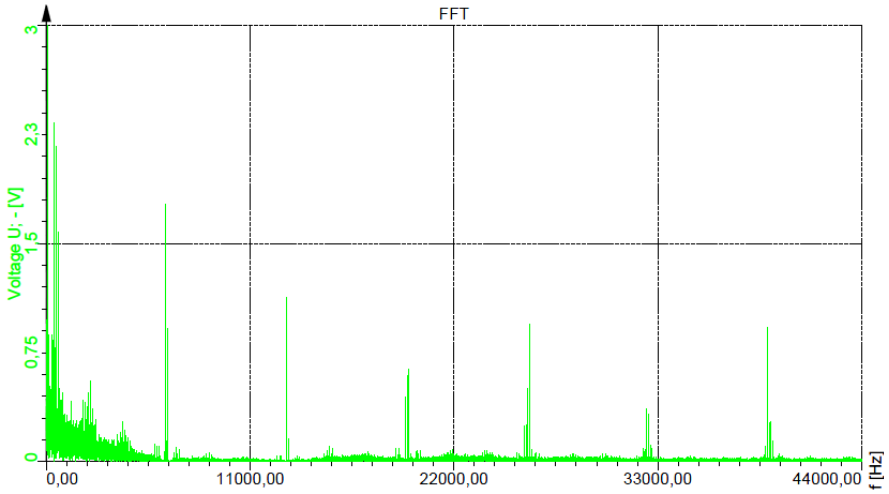


Figure 4.11 Measured output harmonic with 10 kW resistive load

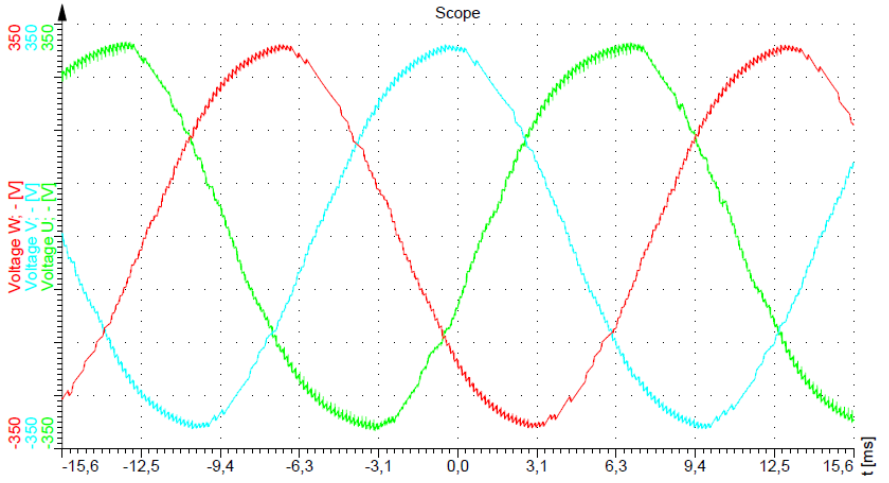


Figure 4.12 Measured waveform with 30 kW resistive load

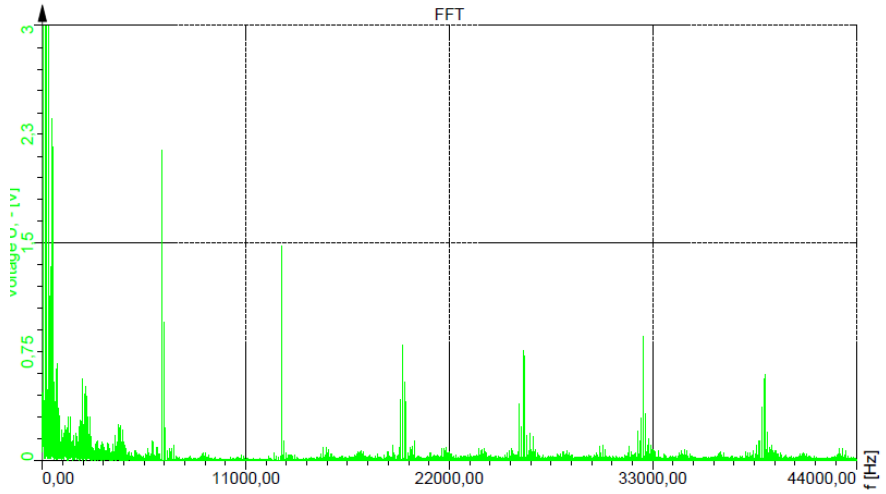


Figure 4.13 Measured output harmonic with 30 kW resistive load

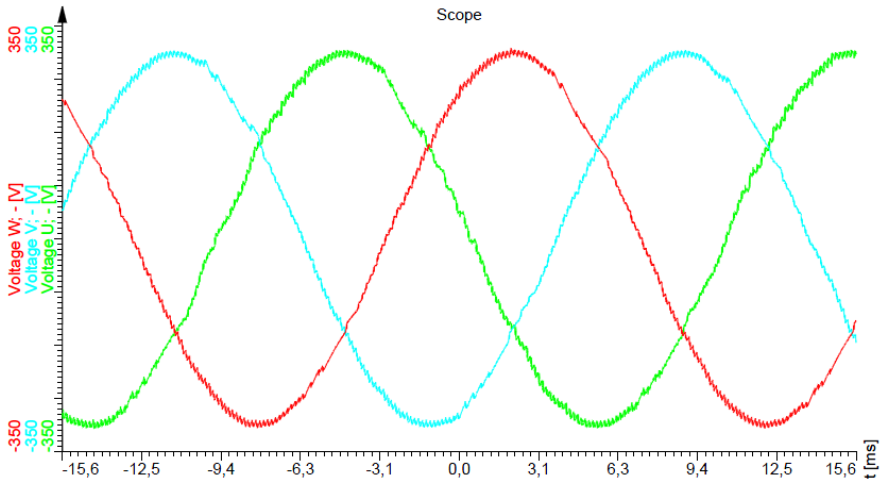


Figure 4.14 Measured waveform with 50 kW resistive load

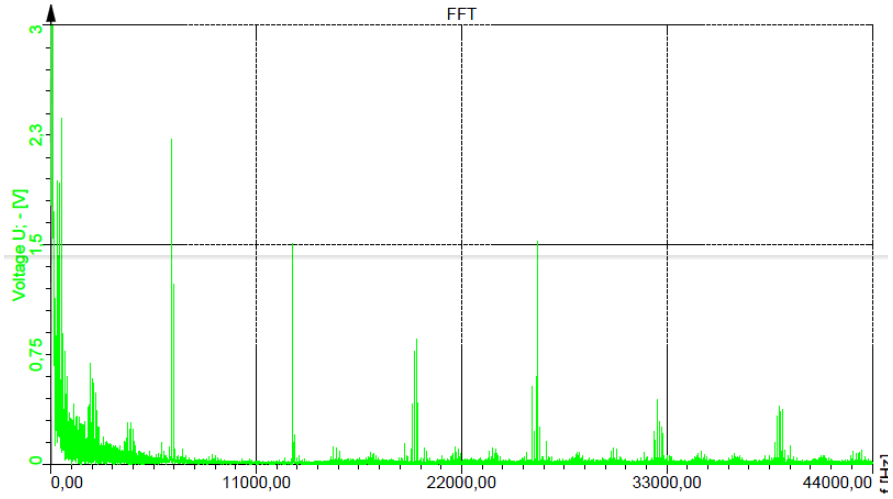


Figure 4.15 Measured output harmonic with 50 kW resistive load

Power losses and output THD (total harmonic distortion) are also interesting parameters. These parameters are measured with Yokogawa WT1600 and WT 3000 power meter. The losses are the difference between the input power and output power. The losses include semiconductor losses, copper losses, transformer losses and output capacitor losses.

There are problems when measuring the input power, especially measuring the input current, which is noisy even when a line filter inductor is connected. Figure 4.16 and Table 4.3 show the results. The blue line shows the measured results from WT3000 and the red dashed line is the results that from WT1600. There is difference between instruments for power losses measurement.

The THD is less than 1% which is a very good value even with the reduced DC link voltage. With an increased DC-link voltage to 750V DC as has been done in the simulation, the THD is expected to be reduced. However this indicates that smaller output capacitors can be implemented to reduce the system cost, weight and volume.

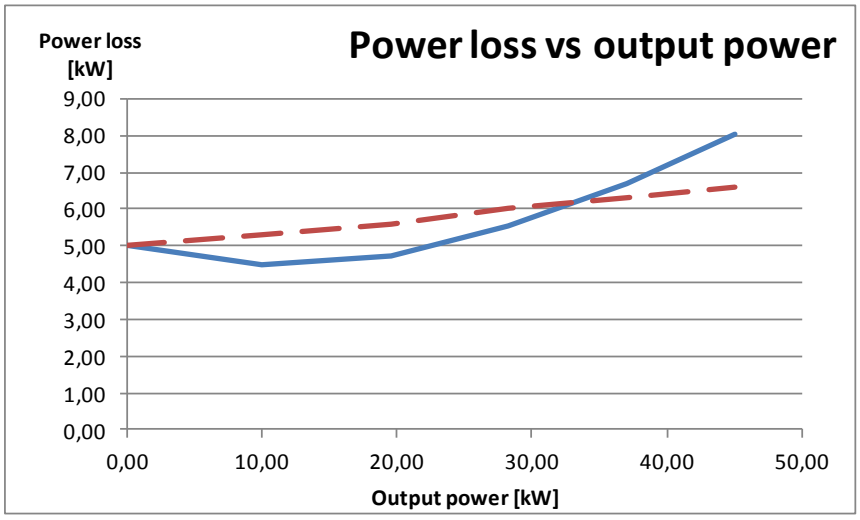


Figure 4.16 Measured losses vs output power

Table 4.3 Measured Power and THD

P_{in}[kW]	P_{out}[kW]	P_{loss}[kW]	THD [%]	U_{dc}[V]
5.006	0	5.01	<1	566.4
14.461	9.97	4.49	<1	540.1
24.247	19.51	4.73	<0.96	505.3
33.796	28.25	5.54	<1	462.5
43.688	37.01	6.68	0.81	606.7
53.043	45.01	8.03	0.91	611.5

Chapter 5
High Efficiency Drive Circuit of SiC BJT Switches

5.1 Introduction of SiC BJT

In the thesis, the author has investigated silicon-carbide transistors in different kinds of converter topologies. Current controlled bipolar junction transistors (BJT) in two level converters, and voltage controlled JFETs in the topology described in this thesis. The voltage controlled devices can use standard gate drive units, while the current controlled BJTs require specialized base drive units [50-55]. The proposed base drive unit is described in this chapter.

Advantages and drawbacks

Low on-state voltage drop, high switching speed, high maximum operating temperature are important issues for power electronic devices. All those three features can be found in Silicon Carbide (SiC) Bipolar Junction Transistor (BJT). Very promising results have been reported recently in the SiC BJT technology [16] [17] [43-46].

Instead of positive temperature coefficient that is inherent in the Si BJT, SiC BJT has negative temperature there by parallel connection of SiC BJT is possible [44]. Second breakdown problem [18] which is one of the main drawbacks of Si BJT is not found in SiC BJT [16]. The switching time of SiC BJT are the same as for unipolar SiC devices like MOSFET and JFET [48-50]

(1) Assuming the supply voltage of the output stage of the driver circuit is 5 V. For a 100 A collector current we need at least 5 A base current. The minimum output power for a three phase inverter could be calculate as: 5V×5A×3=75W

The main disadvantage of SiC BJT is that the BJT is a current controlled device: it needs base current to be turned on. Current gain of SiC BJT is typically around 50 at room temperature (25°C) which is a considerable improvement comparing to Si BJT. However, the current gain decreases to around 25 at 150 degree C. This means, for a 100 A collector current a base current of at least 5 A would be required. This leads to approximately more than 75 W (1) total losses at the driver circuit side for a three phase inverter if a concept of constant base current is used. The SiC BJT base driver circuit will be more expensive than traditional voltage drive devices like IGBTs and MOSFETs due to this significant higher power consumption.

Problem and effort so far

An effort to minimize the base driver power requirement is to use proportional base current, this idea has been applied to Si BJT [19] to [21] in 1980s by including a current transformer. Another effort is to use an IGBT gate drive concept to control the BJT with a voltage signal [22] which could adopt the conventional voltage drive concept and thereby reducing the cost of the driver circuit. However, in this IGBT gate drive concept the conduction losses are increased several times due to the increased collector emitter voltage. A drive concept for reducing the conduction loss in a Darlington Si BJT transistor was introduced in [23], and this concept could be adopted to reduce the increased collector emitter voltage, which is introduced by using the IGBT gate drive concept. In this work the proposed drive concept combines the IGBT gate drive concept and the drive concept introduced in [23] to reduce the power requirement of a SiC BJT driver.

The proposed drive concept

Figure 5.1a shows the IGBT gate drive method. An IGBT *Q1* and a SiC BJT *Q2* are connected like a Darlington transistor. The SiC BJT can be turned on/off by connecting a positive /negative voltage between gate *Q1* and emitter *Q2*. The on-stage voltage drop will be increased according to (5.1)

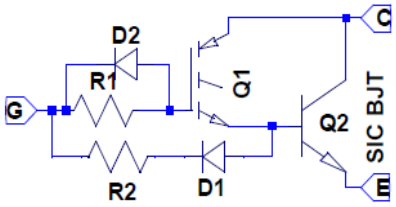


Figure 5.1a IGBT Gate driver concept

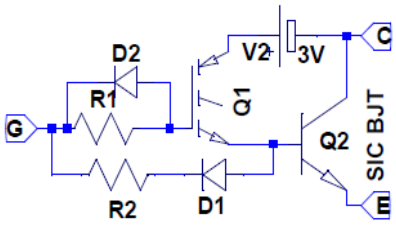


Figure 5.1b Gate driver with voltage compensation

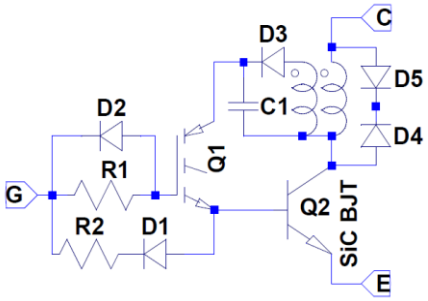


Figure 5.1c Proposed IGBT gate current transformer compensated drive concept

$$V_{ceQ2} = V_{ceQ1} + V_{beQ2} \tag{5.1}$$

Here V_{beQ2} is the on-state base emitter voltage of the SiC BJT, V_{beQ1} is the collector emitter voltage of IGBT $Q1$ with typical values of 2.7V and 1 V respectively. This gives a 3.7 V on-state voltage of the SiC BJT which is not acceptable. This can be compensated for by adding a voltage between the collector $Q1$ and the collector $Q2$ to force the SiC BJT to operate in the deep saturation region (Figure 5.1b) and (5.1) can now be rewritten as (5.2)

$$V_{ceQ2} = V_{beQ1} + V_{ceQ2} - V_2 \tag{5.2}$$

The conduction losses could be decreased by this change of the value of V_2. The compensation voltage in this work is realized with a current transformer as shown in Figure 5.1c. The primary winding is connected to the collector of the SiC BJT and the secondary winding is connected in parallel with C1 via a high voltage SiC diode. The function of C1 is to rectify the current of secondary winding into the compensation voltage. The zener diodes D4 and D5 are connected in opposite direction for resetting the transformer core and clamp the huge voltage caused by the leakage inductance. The base current is fed directly from the load.

5.2 Analysis

For a Silicon BJT the transistor has to operate in the quasi saturation area to switch fast and to reduce the switching losses. The SiC BJT transistor can still switch fast even in the deep saturation area. The current gain of a SiC BJT decreases with increasing temperature. When designing the base drive unit, the maximum junction temperature of the SiC BJT shall be considered, as the base drive circuit shall be able to provide sufficient base current at the maximum junction temperature. In our proposed driver topology the drive current is fed from the load current via a current transformer. The turn ratio of the current transformer defines the ratio between the base current and the load current. The turn ratio shall be smaller than the current gain at maximum operating temperature for sufficient base current.

To turn on the SiC BJT, the base emitter PN junction shall change from reversed bias to forward bias and start to conduct the current. The base emitter parasitic capacitance needs to be charged from negative bias voltage to 3 V. The parasitic capacitance is fairly large, 1.8nF at 0V and 5.6 nF at 3.2V. An over current at the beginning of the turn on interval is needed to charge the base emitter capacitance. This can be achieved by using a capacitor in parallel with the base resistance as shown in Figure 5.2, the capacitor provides the over current at turn on of the transistor.

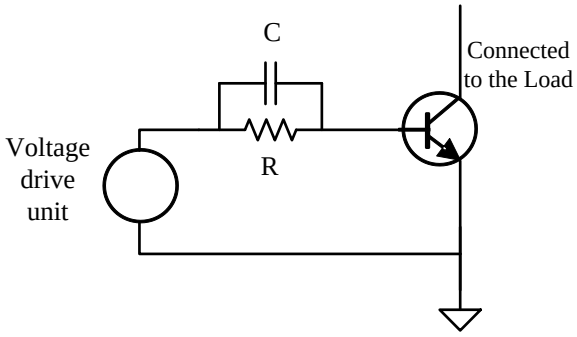


Figure 5.2 Driving concept with parallel capacitor

For the proposed drive topology, the equivalent circuit during turn on is shown in Figure 5.3. When the gate transistor Q1 is turned on, the voltage over the drain and the source of Q1 is starting to decrease, this leads to that the voltage over the collector and the emitter of SiC BJT is decreasing. Since the SiC BJT is not turned on, the only way to discharge the collector and emitter capacitance Cce of the SiC BJT is via the capacitor C1, the transistor Q1 and the base emitter capacitance Cbe.The discharge of the base emitter capacitance provides sufficient over current for the fast turn on of SiC BJT.

Once the base emitter has been forward biased, the transistor starts to conduct current. The transformer secondary current is increasing proportionally to the collector current. This current flows into the base of SiC BJT via D3 and the capacitor C1, a fraction of the current charges C1 to maintain the compensation voltage. The increasing collector current is limited by the leakage inductance of the transformer and the emitter stray inductance.

The turn off of a SiC BJT, using the proposed driving topology, is the same as the turn off of a MOSFET. Once a negative gate voltage is applied, the excess charge carrier is removed via D1 and R1 in a short time and the base emitter capacitance is discharged. After this the collector emitter voltage starts to increase and the collector current starts to decrease.

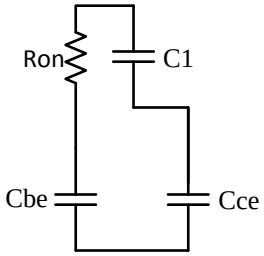


Figure 5.3 Equivalent circuit when during turn on of SiC BJT

5.3 Implementation

In this section, design and selection of the devices are discussed. The current transformer is thoroughly investigated

Diodes

The zener diodes D4 and D5 are connected in opposite direction for resetting the transformer core after turning off the transistor and clamping the surge voltages caused by the leakage inductance. (5.3) gives the break down voltage of the zener diodes. Where V_c, N and η are the compensation voltage, turn ratio of the transformer and maximum duty ratio of the transistor respectively.

$$V_z = \frac{V_c \times \eta}{(1-\eta) \times N} \tag{5.3}$$

The breakdown voltage is selected to 16 V to have more than 98% duty ratio. Diode D3 should be able to withstand the voltage $16 \times N$ V during the core resetting interval, where N is the turn ratio between the secondary and primary windings. In this design a 600 V SiC Schottky diode is selected.

Current transformer

Assuming the capacitance C1 in Figure 5.1c is large enough to keep its voltage stable. Then the secondary voltage V_2 during the turn on interval can also be considered as constant. The magnetizing current could be calculated with (5.4)

$$I_m = \frac{\mathrm{V}_2}{\mathrm{L}_2} t = \frac{\mathrm{V}_2}{A_l N_2^2} t \tag{5.4}$$

Here L_2, N_2 and A_l are the inductance of the secondary winding when the primary winding is open, the number of turns of the secondary winding and A_l the value of the transformer core, respectively. The current of the secondary winding during turn on interval is given by (5.5)

$$I_2 = \frac{I_l}{n} - \frac{\mathrm{V}_2}{A_l N_2^2} t \tag{5.5}$$

Here I_l is the load current, n is the turn ratio of the current transformer. The base current should be the mean value of I_2 during the turn on interval.

$$I_b = \frac{1}{T}\int_0^T I_2 dt = \frac{I_l}{n} - \frac{\mathrm{V}_2}{2A_l N_2^2} T = \frac{I_l}{n} - \frac{\widehat{I_m}}{2} \tag{5.6}$$

Here $\widehat{I_m}$ is the maximum magnetizing current, in order to make the SiC BJT to operate in the saturation region, $I_b \geq I_c/\beta$, where β is the current gain of the transistor. Substitution of $I_b$into $I_b \geq I_c/\beta$ gives:

$$\frac{1}{n} \geq \frac{1}{\beta} + \frac{\widehat{I_m}}{2I_l} \tag{5.7}$$

Conduction losses in this drive concept is written as

$$P_{loss} = (I_l - I_b) \times V_{ceQ2} + I_b \times (V_{ceQ1} + V_{beQ2}) \tag{5.8}$$

(5.8) shows that in order to decrease the conduction losses the base current I_b of Q2 should be kept at a minimum due to the 3 V base emitter diode threshold voltage. Higher turn ratio n will reduce the base current I_b.

The saturation time of the transformer, which defines the minimum switching frequency, is also an important issue that should be investigated. (5.9) [13] gives the saturation time, where N_s is the number of turns of the secondary winding $and\ V_{sec}$is the secondary voltage, respectively. Higher number of turns of the secondary winding gives longer saturation time of

the current transformer, which allows the driver circuit to operate at a lower switching frequency.

$$t_s = \frac{N_s(B_s - B_r)A_e}{V_{sec}} \tag{5.9}$$

According to the discussion above, higher number of turns of the secondary winding is required. The requirement of the turn ratio of the current transformer is given by (5.7). What we can change in (6) is the maximum magnetizing current $\widehat{I_m}$. There are two ways to decrease the $\widehat{I_m}$, either increase the switching frequency to limit the magnetizing time, or select a core with a high A_l value.

A nanocrystalline core from VAC [27] with high A_l value is chosen. The details of the core is presented in Table **5.**1

Table **5.**1 Parameters of transformer core

Dimension	$25 \times 16 \times 10$ mm
A_{Fe}	$0.36cm^2$
I_{Fe}	$6.44cm$
m_{Fe}	$17.0g$
$A_{l\,(10kHz)}$	$\{50\mu, 95\mu\}$

The winding technique of the transformer is always an important issue. It is important that the leakage inductance is kept at a minimum. In this work, the idea is to wind the primary and secondary conductors in parallel paths, which is a well-known method to obtain low leakage inductance. In this case, the turn ratio is selected to 22:1, according to (5.7). Therefore, a split winding technique is adopted. The split winding technique for a coaxial transformer is discussed in [25]. The parallel primary and secondary winding is discussed in [24]. Figure 5.4 shows a prototype of the proposed transformer. The white metal on top is the one turn primary winding, and the copper winding under the white metal is the 22 turn secondary winding. The primary winding contains 11 parallel conductors, and the secondary has 22 series connected conductors. Each primary winding conductors covers 2 secondary conductors.

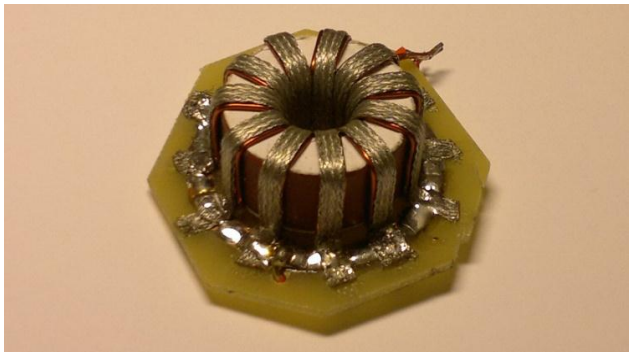


Figure 5.4 Prototype of current transformer

5.4 Experimental results

The proposed driver circuit is driven by an IGBT driver 2SD316EI-12(V1 in Figure 5.5 (a)) from Concept Drive [26] with 10 kHz switching frequency. Figure **5.**5 (b) shows the experimental setup. The load includes a 27mH load inductance bank, a 1.7 ohm power resistance bank and freewheeling diodes. Three 6 A 1200 V SiC BJTs (from TranSiC AB Sweden) are connected in parallel together with 0.05 ohm current sensing resistance. The idea is to switch the driver above a certain switching frequency, measure the on-state voltage drop and the current sharing property of the parallel connected SiC BJTs.

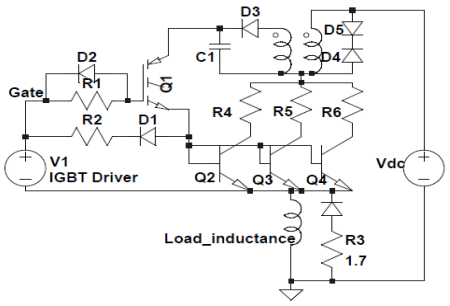


Figure 5.5 a Schematic of experimental setup

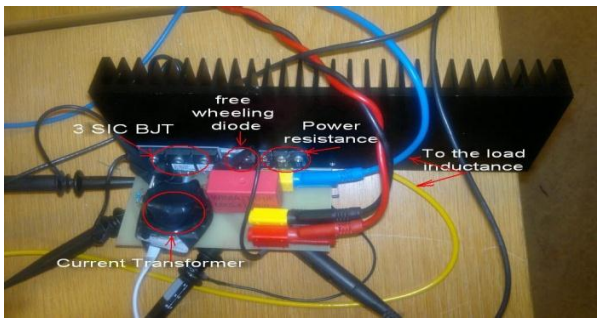


Figure 5.5b Experimental setup

As shown in Figure **5**.6, at the 10 kHz switching frequency, a compensation voltage of 3.7 V will be built up within 3 ms after the transistor starts switching, the measurement verifies the simulation: with an 8.66A load current and 20% switching duty ratio, the compensation voltage is measured to 3.6 V with a multimeter.

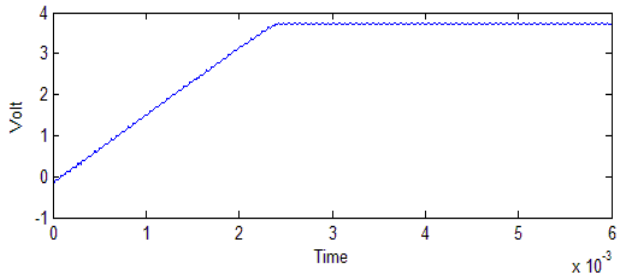


Figure 5.6 Simulated compensation voltage

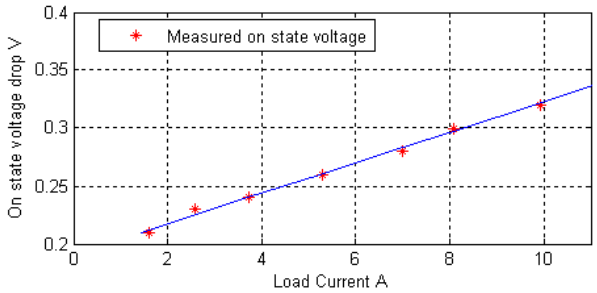


Figure 5.7 Measured on-state voltage drop

With the help of the compensation voltage, the SiC BJT should operate in the saturation region. Figure 5.7 shows the on-state voltage drop when the

proposed drive concept is used. Please note that the X axis indicates the sum of the 3 collector currents. It is clear that the on-state voltage, when using the proposed drive concept, is quite low and the transistor operates in the deep saturation region.

The current sharing property of the parallel connected transistors is also investigated in this work. Figure **5.**8 shows the voltage over the 0.05 ohm current sensing resistance of each transistor. It is clear that there is no observed difference between the collector currents of transistor 1 and of transistor 3 respectively, and the mean current of transistor 2 agrees with the collector current of transistor 1 and 3. Current ringing in transistor 2 is observed, and is further investigated by changing the position of the three transistors. The result shows that the current ringing is only position related, which means that the SiC BJT shares the current equally with the proposed drive concept.

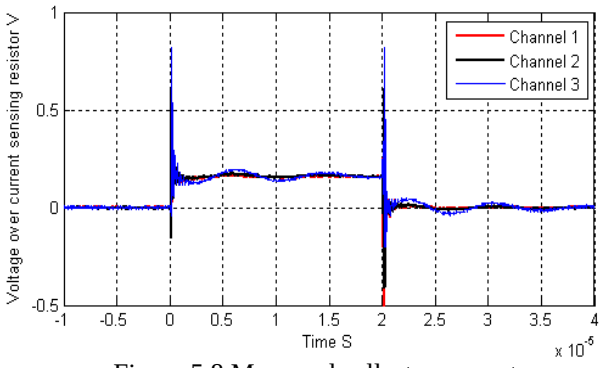


Figure 5.8 Measured collector current

5.5 Summary

A new driving concept for SiC BJT is analyzed, implemented and evaluated. The new driving concept can control the SiC BJT with a voltage signal and keeps the SiC BJT still working in the saturation area during the turn on phase.

SiC JFETs are simple to drive with a voltage controlled driver, while the SiC BJT requires a current controlled driver. The base drive concept

described in the chapter needs bulky current transformer and auxiliary circuit around it which makes the system complex. As voltage controlled driver easily can be found on the market “of the shelf”, the SiC JFET was chosen to be the switch in this project

Chapter 6
Concluding Remarks and Future Work

The aim of this work is to investigate the possibility to generate a low frequency AC voltage by using intermediate high frequency current pulses directly. By doing so the cost of the auxiliary converter system may be reduced because fewer components are needed compared to the number in a conventional auxiliary converter. To be able to verify this, theoretical analysis and calculation is carried out to determine the topology of the converter and to dimension the major component of the converter. The result of the theoretical analysis and the calculation is validated by simulation and measurements in the converter prototype.

6.1 Summary of findings

Simulation of the proposed auxiliary converter topology in combination with the prototype design and measurement is the main focus in this work. Some conclusions regarding the new converter topology are drawn.

First, it is important to understand the mechanism of generating and controlling the current pulses. Two methods are developed in this work,-the inductive link and the resonant link.

The basic idea of the inductive link method is to control the current through an inductor by changing the applied inductor voltage. Equations of how to calculate the duty ratio of each semiconductor switch are developed in this work. The equations of dimensioning the passive component are also given in this thesis. Based on the theoretical analysis and simulation, converter prototypes are built to validate the theoretical analysis.

There is no energy stored in the inductive link circuit between two adjacent current pulses. Thereby the second current pulse is independent of the previous current pulse which gives the freedom to choose the polarity and the duration of the second current pulse. On the other hand, due to the lacking of energy storage device other than the inductor itself, power semiconductor switches need to be turned off at peak current which may introduce excess switching losses. With the aim of reducing the switching losses, the resonant link method is also investigated in this work. By adding a capacitor in series with the inductor, a series resonant circuit is formed. The resonant link method is based on controlling the current in the series resonance circuit with the aim to reduce the switching losses. Compared to the conventional series resonant converter this proposed resonant link topology has difficulty to keep the resonant energy stable, and a new energy balance method is developed in this work to solve the problem. This method is verified by simulation in LTspice. Anyhow as discussed in chapter 3 the resonant link version cannot avoid hard switching of the transistor but, compared to the inductive link, the number of switching are reduced. On the other hand, due to the resonance capacitor, the energy of the series resonant circuit will be stored in the capacitor between two adjacent current pulses, and the resonance capacitor voltage defines the polarity of the next current pulse. Thereby the resonant link version requires balanced loads.

6.2 Future work

This work focuses on developing a new auxiliary converter topology for railway applications. Both the inductive link and the resonant link version of the auxiliary converter is discussed and analyzed. For the proposed auxiliary converters, either with the inductive link or with the resonant link topology, the most bulky components are the output capacitor bank and the 20 kHz pulse frequency transformer, as proposed in this thesis. However, by using Silicon Carbide devices the switching frequency could be higher, which will reduce the size of both the transformer and the output capacitor bank dramatically. However, with an increased pulse frequency the di/dt of each current pulse should be taken into account from an EMC/EMI point of view. Another issue with the increased pulse frequency is that the inductor L1 will be reduced. E.g. the total inductance of the prototype inductor L1, described in section 4.2, see Figure 2.1, is 9.3 µH. With an increased pulse frequency of 60 kHz, the inductance is reduced to 3.1 µH and this value is smaller than the leakage inductance of the transformer, in chapter 4, This

indicates that in order to achieve the same power as proposed in section 4.2, either the switching frequency shall be reduced or the transformer shall be replaced by an transformer with smaller leakage inductance. Ideally the inductor L1 can be the transformer leakage inductance, and this should be the target for future research.

In the prototype described in section 4.2, the transformer is reused from another project and it is over dimensioned for our prototype. The control algorithm has not taken the magnetizing current of the transformer into account. The magnetizing current is neither monitored nor controlled in any way in the prototype. The transformer core may saturate due to too high magnetizing current. Investigation of the transformer core magnetizing current is an interesting issue for the dimensioning of the transformer.

The output capacitors are filter capacitors. The peak current is quite high in the proposed auxiliary converter, and the lifetime estimation of the output capacitor is a really interesting subject and should be investigated thoroughly in future research.

Due to limited time only a prototype with the inductive link version is designed and tested in the lab. The resonant link version is only analyzed and simulated. Design and test of a resonant link auxiliary converter prototype could be considered as a future task.

References

[1] Wikipedia, [Online] [Cited: March 20, 2014] http://en.wikipedia.org/wiki/TGV

[2] Weber J., Berger A. and Falk A.: Galvanic separated high frequency power converter for auxiliary railway supply, 10th Eur. Power Electron. Conf., Toulouse, France, Sep. 2003.

[3] Vinnikov D., Laugis J. and Jalakas T.: Development of auxiliary power supplies for the 3.0 kV DC rolling stock, in Proc. IEEE Int. Symp. Ind. Electron, Vigo, Spain, Jun. 2007, pp. 359–364.

[4] Deblecker O., Moretti A. and Vallée F.: Comparative Study of Soft-Switched Isolated DC-DC Converters for Auxiliary Railway Supply, IEEE TRANSACTIONS ON POWER ELECTRONICS, VOL. 23, NO. 5, SEPTEMBER 2008, pp. 2218–2229.

[5] S. Dieckerhoff and U. Schaefer, "Transformerless drive system formain line rail vehicle propulsion," presented at the 9th Euro. Power Electron. Conf., Gratz, Austria, 2001

[6] S. Dieckerhoff, S. Bernet, and D. Krug, "Power loss-oriented evaluation of high voltage IGBTs and multilevel converters in transformerless traction applications," IEEE Trans. Power Electron. , vol. 20, no. 6, pp. 1328–1329, Nov. 2005.

[7] Nagai M., Mochizuki M., Nabae A.: High-frequency link DC/AC converter with suppressed voltage clamp circuits-naturally commutated phase angle control with self turn-off devices, IEEE Trans. Ind. Applicat., vol. 32, p. 293, Mar/Apr 1996.

[8] M.K. Kazimierczuk and D. Czarkowski," Resonant Power Converters, 2nd Edition",Wiley, New York, USA, 2011

[9] Hall, S., Loayza-Vargas Y. (2013), "An evaluation of two direct current control methods implemented with LabVIEW on a FPGA". *International Conference on Electrical Machines and Systems*

(ICEMS2013), Busan, Korea, October 26-29, 2013.N. Mohan, T.M. Undeland and W.P. Robbins,"Power Electronics; Converters, Applications, and Design", 2nd ed., Wiley, New York, USA, 1995.

[10] http://www.linear.com/designtools/software/

[11] Josef Lutz, Heinrich Schlangenotto, Uwe Scheuermann, Rik De Doncker, Semiconductor Power Devices: Physics, Characteristics, Reliability, Springer 2011.

[12] Rabkowski J., Peftitsis D., Nee H.: Silicon Carbide Power Transistors: A New Era in Power Electronics Is Initiated, IEEE Industrial Electronics Magazine, ISSN: 1932-4529, Vol. 6, No. 2, pp. 17-26.

[13] Barry W Williams, POWER ELECTRONICS Devices, Drivers, Applications, and Passive Components, ISBN 978-0-9553384-0-3, 2006. http://homepages.eee.strath.ac.uk/~bwwilliams/book.htm

[14] N.Mohan, T.M. Undeland, and D. P. Robbins, "Power Electronics: converters, applications, and design," John Wiley & Sons, 1995, ISBN 0-471-14208-5

[15] Per Ranstad, "Design and Control Aspects on Components and Systems in High-Voltage Converter for Industrial Applications" Doctoral Thesis in Power Electronics Stockholm, Sweden 2010, ISBN 978-91-7415-757-4.

[16] Yan Gao, Alex Q. Huang, Sumi Krishnaswami, Jim Richmond, andAnant K. Agarwal, Comparison of Static and Switching Characteristics of 1200 V 4H-SiC BJT and 1200 V Si-IGBT. IEEE Transations On Industry Applications, Vol.44, No. 3, May/June 2008, Pages: 887-893.

[17] Madhu Chinthavali, Puqi Ning, Yutian Cui, Leon M. Tolbert, Investigation on the Parallel Operation of Discrete SiC BJTs and JFETs, Twenty-Sixth Annual IEEE Applied Power Electronics Conference and Exposition,Year: 2011, Pages: 1076-1083.

[18] B.W. Williams: Power Electronics: Devices, Drivers, Applications, and Passive Components.

[19] Avant, R.L.， Shortt, D.J., West, G.E. , Palma, R.E., INTELEC '84 - International Telecommunications Energy Conference Year: 1984 Pages: 352-358 .

[20] Varga L.D., Losic N.A., Design of a high-performance floating power BJT driver with proportional base drive, Industry Applications Society Annual Meeting, 1989, Conference Record of the 1989 IEEE Pages: 1186-1189.

[21] Prest, R.B.,Van Wyk, J.D.,Pulsed transformer base drives for high-efficiency high-current low-voltage switches, IEEE Transactions on Power Electronics Year: 1988 Vol.3 No.2 Pages: 137-146.

[22] Huijie Yu, A gate driver based soft-switching SiC Bipolar Junction Transistor, Power Electronics Specialist Conference, 2003. PESC '03. 2003 IEEE 34th Annual Pages: 968-973.

[23] Isao Takahashi, Jun-ichi Itoh and Guijia Su, How to get 99% inverter efficiency, IAS 1994, Pages: 971-976.

[24] P. Karlsson, Quasi Resonant DC Link Converters – Analysis and Design for a Battery Charger Application, Licentiate's Thesis, Department of Industrial Electrical Engineering and Automation. Lund Institute of Technology, Lund, Sweden, Nov. 1999.

[25] S. Chen, B.J.C. Filho and T.A. Lipo, Design and Implementation of a Passively Clamped Quasi-Resonant Inverter, IEEE-IAS Annual Conf. Rec., 1995, Vol. 3, Pages: 2387-2392.

[26] www.igbt-driver.com.

[27] www.vacuumschmelze.com.

[28] I. Yamato, N. Tokunaga, "Power loss reduction techniquefor three phase high-frequency link DC-AC converter," in Proceeding of IEEE Power Electronics Specialist Conference, pp. 663–668, Jun. 1993.

[29] P.M. Espelage and B.K. Bose, "High-Frequency link powerconversion," IEEE Trans. Indus. Appl., vol. IA-13, no., pp.387-394, 1977.

[30] T. Fukao and M. Matsui, "Basic characteristics of cycloconverter for linking commercial and high frequency distribution lines," IEEE Trans. Indus. Appl., vol. IA-23, no.5, pp. 927-936, 1987

[31] R. Huang, and S.K.Mazumder, "A soft-switching scheme for an isolated DC/DC converter with pulsating DC output for a three-phase high-frequency-link PWM converter", IEEE Trans. Power. Electron., Vol 24, No. 10, pp.2276-2288, Oct. 2009.

[32] R.Garcia-Gil, J. M. Espi, E. J. Dede, and E. E. Sanchis Kilders, "A bidirectional and isolated three-phase rectifier with soft-switching operation," IEEE Trans. Power Electron., vol. 52, no. 3, pp. 765-773, Jun. 2005.

[33] Harada. K, Sakamoto. H, Shoyama. M, Phase-Controlled DC-AC converter with high-frequency switching", Power Electronics, IEEE Transactions on, Vol. 3, Issue 4, Oct.1988, pp. 406-411

[34] M. Matsui, N. Nagai, M. Mochizuki and A. Nabae, High-Frequency Link dc/ac converter with suppressed voltage clamp circuits-naturally commutated phase angle control with self-turn off devices," IEEE Trans. Ind. Appl., vol. 32,no. 2, pp. 293-300, Mar./Apr. 1996

[35] S. Deng, H. Mao, J. Mazumdar, I. Batarseh and K. Islam, "A new control scheme for high-frequency link inverter design,"

[36] Fukao, Tadashi; Matsui, Mikihiko. Basic Characteristics of Cycloconverter for Linking Commercial and High-Frequency Distribution Lines *IEEE Transactions on Industry Applications* , 1987, Vol. IA-23 Issue 5, p927-936, 10p. Publisher: IEEE.

[37] H. Matsuo; K. Iida; K. Harada, High power soft switching PWM AC auxiliary power supply system of the electric railway rolling stock and its deadbeat control, Power Electronics Specialists Conference, 1995. PESC '95 Record., 26th Annual IEEE Year: 1995, Volume: 1Pages: 258 - 263 vol.1

[38] Wu, Dan; Guo, Zhiqiang; Sha, Deshang; Qin, Zian; Liao, Xiaozhong. Parallel-connected three-phase inverters for railway auxiliary power supply without sensing output currents 2012 Twenty-Seventh *Annual IEEE Applied* ***Power*** *Electronics Conference & Exposition (APEC)* , 1/ 1/2012, p136-140, 5p. Publisher: IEEE.

[39] Alkayal, Fisal; Saada, Johnny Bou. Compact three phase inverter in Silicon Carbide technology for auxiliary converter used in railway

applications *2013 15th European Conference on Power Electronics & Applications (EPE)* , 2013, p1-10, 10p. Publisher: IEEE.

[40] Baars, Nico H.; Everts, Jordi; Huisman, Henk; Duarte, Jorge L.; Lomonova, Elena A. A 80-kW Isolated DC–DC Converter for Railway Applications, *IEEE Transactions on Power Electronics.* Dec2015, Vol. 30 Issue 12, p6639-6647. 9p. DOI: 10.1109/TPEL.2015.2396006

[41] Quesada, Isabel; Lazaro, Antonio; Martinez, Carlos; Barrado, Andrés; Sanz, Marina; Fernandez, Cristina; Vazquez, Ramón; Gonzalez, Ignacio. Modulation Technique for Low Frequency Harmonic Cancellation in Auxiliary Railway Power Supplies IEEE Transactions on Industrial Electronics. Sep2011, Vol. 58 Issue 9, p3976-3987. 12p. DOI: 10.1109/TIE.2010.2102320.

[42] Gannshin, A. A.; Meleshin, V. I.; Sachkov, S. A.; Zhiklenkov, D. V. Railway auxiliary power converter operating with 3 kV DC supply line on the basis of 6.5 kV IGBT modules. *2014 16th International Power Electronics & Motion Control Conference & Exposition* , 2014, p654-660, 7p. Publisher: IEEE.

[43] A.Agarwal, Q. Zhang, A. Burk,R.Callanan, and S. Mazumder, "Prospects of bipolar power devices in silicon carbide," in Proc. 34th IEEE Annu. Conf. Ind. Electron., Nov. 10–13, 2008, pp. 2879–2884

[44] M. Chinthavali, P. Ning, Y. Cui, and L. M. Tolbert, "Investigation on the parallel operation of discrete SiC BJTs and JFETs," in Proc. 26th IEEE Annu. Appl. Power Electron. Conf. Expo., Mar. 2011, pp. 1076–1083

[45] M. Domeij, A. Konstantinov, A. Lindgren, C. Zaring, K. Gumaelius, and M. Reimark, "Large area 1200 V SiC BJTs with $\beta > 100$ and ρ ON <3 mΩ cm2 ," Mater. Sci. Forum, vol. 717 - 720, pp. 1123 - 1126, May 2012.

[46] A. Lindgren and M.Domeij, "Degradation free fast switching 1200V50A silicon carbide BJT's," in Proc. IEEE 26th Annu. Appl. Power Electron. Conf. Expo., Mar. 6–11, 2011, pp. 1064–1070.

[47] A. Lindgren and M. Domeij, "Fast switching 1200 V 50 A silicon carbide BJT's in boost converters," in Proc. 14th Eur. Conf. Power Electron. Appl., 2011, pp. 1–8.

[48] J. Rabkowski, D. Peftitsis, H.-P. Nee, andM. Zdanowski, "A simple high performance low-loss current-source driver for SiC bipolar transistors," in Proc. 7th Int. Power Electron. Motion Control Conf., Jun. 2–5, 2012,vol. 1, pp. 222–228.

[49] T. Funaki, M. Sasagawa, and T. Nakamura, "Multi-chip SiC DMOSFET half-bridge power module for high temperature operation," in Proc. 27th IEEE Annu. Appl. Power Electron. Conf. Expo., Feb. 2012, pp. 2525–2529.

[50] Henry; Hofmann, Wilfried. Efficiency increase of SiC-BJT inverter by driver loss reduction with one-step commutation *2014 IEEE 26th International Symposium on Power Semiconductor Devices & IC's (ISPSD)* , 2014, p233-236, 4p. Publisher: IEEE

[51] By: Rabkowski, J.; Tolstoy, G.; Peftitsis, D.; Nee, H. Low-Loss High-Performance Base-Drive Unit for SiC BJTs *IEEE Transactions on Power Electronics*. May2012, Vol. 27 Issue 5, p2633-2643. 11p. DOI: 10.1109/TPEL.2011.2171722. , Database: Business Source Complete

[52] Sarnago, Hector; Lucia, Oscar; Mediano, Arturo; Burdio, Jose M. Improved Operation of SiC–BJT-Based Series Resonant Inverter With Optimized Base Drive*IEEE Transactions on Power Electronics*. Oct2014, Vol. 29 Issue 10, p5097-5101. 5p. DOI: 10.1109/TPEL.2014.2312216

[53] Tolstoy, Georg; Peftitsis, Dimosthenis; Rabkowski, Jacek; Nee, Hans-Peter; Palmer, P. R.;, A discretized proportional base driver for Silicon Carbide Bipolar Junction Transistors Skolan för elektro- och systemteknik (EES), Elektrisk energiomvandling. In: *2013 IEEE ECCE Asia Downunder - 5th IEEE Annual International Energy Conversion Congress and Exhibition, IEEE ECCE Asia 2013*. 01/01/2013 :728-735; IEEE, 2013

[54] Rabkowski, Jacek; Mariusz, Zdanowski; Peftitsis, Dimosthenis; Nee, Hans-Peter; KTH, A Simple High-Performance Low-Loss Current-Source Driver for SiC Bipolar Transistors In: *7th International Power Electronics and Motion Control Conference*

(IPEMC), 2012. 01/01/2012 :222-228; IEEE conference proceedings, 2012

[55] Tournier, D.; Bevilacqua, P.; Brosselard, P.; Planson, D.; Allard, B. SiC BJT driver applied to a 2 kW inverter: Performances and limitations. *2010 6th International Conference on Integrated Power Electronics Systems (CIPS)* , 2010, p1-6, 6p. Publisher: IEEE.

Appendix A Populärvetenskaplig beskrivning av Luyu Wangs doktorsavhandling som skall försvaras vid Lunds Tekniska Högskola

Avhandlingens title:
A new Auxiliary Converter topology with SiC components for Railway Applications

Bakgrund

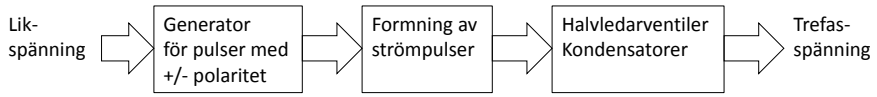
Elektriska fordon tåg, bilar, bussar, lastbilar och vissa typer av båtar försörjs med elektrisk energi från antingen en kontaktledning eller från ombordplacerad utrustning, såsom batteri eller dieselmotordriven generator. Det elektriska systemet försörjer primärt fordonets elektriska framdrivningssystem, motorkonverter och elektrisk motor. Utöver framdrivning av fordonet finns andra elektriska funktioner, fläktar, kompressorer och belysning, som också ska försörjas. För detta ändamål används en s.k. *hjälpkraftkonverter*, som vanligtvis ger en konstant trefasspänning 3x400 V med frekvensen 50 Hz. Från denna spänning erhålls också enfasig 230 V för matning av elektriska uttag vid passagerarplatser.

Hjälpkraftkonverter

Vid konstruktion av en hjälpkraftkonverter är, utöver funktionen, mindre storlek, lägre vikt, högre verkningsgrad och lägre kostnad viktiga egenskaper. Detta arbete avser en ny hjälpkraftkonvertertopologi, som är av multileveltyp, dvs utspänningen är sinusformad utan att ett tungt filter används. Den stora fördelen är således den lägre vikten.

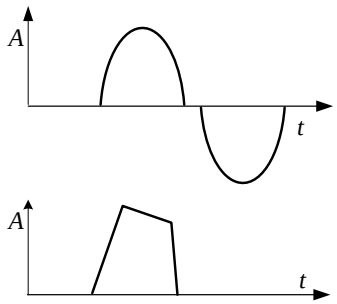
Teknisk beskrivning

Denna konvertertopologi bygger på att alstra strömpulser med mellanfrekvens (något 10-tal kilohertz) och sedan omvandla dessa pulser till den önskade växelspänningen 3x400 V. I topologin sker omvandlingen utan mellanliggande likspänningsmellanled. Istället formas strömpulser i en växelströmslänk mellan den högre frekvensen och den önskade frekvensen 50 Hz, se topologin i Figur A1.



Figur A1 Föreslagen hjälpkraftkonvertertopologi

Som resultat av den inledande teoretiska analysen delas den ursprungliga topologin upp i två topologier, den ena med en induktiv växelströmsmellanlänk medan den andra har en serieresonanslänk. Den senare topologin överenstämmer med den ursprungliga idén men med ett annorlunda modulationssätt. Avhandlingen presenterar modulationssätt samt designregler med ekvationer för båda topologierna. Se strömpulsform i Figure 2.

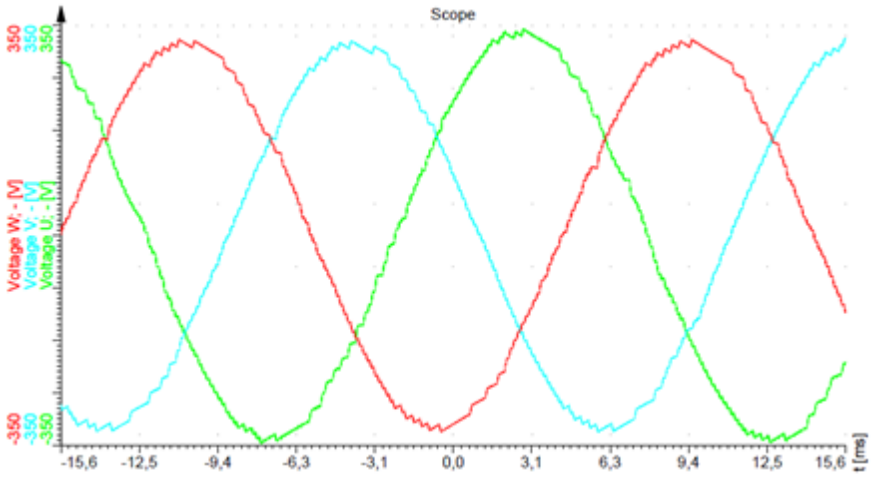


Figur A2 Övre grafen visar strömpulser med serieresonanslänk, nedre grafen strömpuls med induktiv länk (här visas bara en positive puls).

Realisering

För att verifiera teorin är två konvertrar byggda. Den första är en enfasig lågeffektkonverter i vilken styrsystemet utvecklas och testas. Med denna konverter bekräftas också att idén fungerar. Den andra är en trefasig

fulleffektkonverter. Denna är byggd för att testa topologin med den induktiva växelströmslänken och är byggd i Bombardier Transportations laboratorium. Högeffektkonvertern är försedd med kiselkarbidhalvledare där man behöver minska de s.k. switchförlusterna. Se trefasutspänningen i Figure A3.



Figur A3 Erhållen trefasutspänning

Finansiering

Projektet är finansierat av Vinnova och av Bombardier Transportation AB.