Quasi Resonant DC Link Converters

Analysis and Design for a Battery Charger Application

Per Karlsson

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Cover picture
Measurement of the resonant link voltage for the quasi resonant DC link battery charger implemented. See further page 159.

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Abstract

Environmental aspects have during the last years made electric vehicles an interesting competitor to the present internal combustion engine driven vehicles. For a broad introduction of pure electric vehicles, a battery charging infrastructure is deemed necessary. However, to build and maintain such an infrastructure is costly. Active power line conditioning capabilities could be included in the battery charger, making the infrastructure advantageous from the distribution network point of view.

Another option is that the battery charger could be able to support the grid with peak power during periods of stability problems or emergency situations. This means that energy is borrowed from the batteries of vehicles connected to a charger. The price for energy supplied by the batteries is likely to be several times higher than the normal electric energy price, due to the wear costs of the batteries. Therefore, the battery charger losses also represents a high cost. It is often stated that resonant converters have a high efficiency compared to hard switched. Since carrier based pulse width modulation is employed, quasi resonant DC link converters are of interest.

Four of the most promising quasi resonant DC link topologies reported in the literature are compared. A fair comparison is obtained by designing them to meet certain common design criteria, in this case the duration of the zero voltage interval and the maximum output voltage time derivative. The derivation of the design expressions are given, and also the simulation results, by means of efficiency.

A 10 kW battery charger, equipped with one of the quasi resonant DC links investigated is implemented. A hard switched battery charger with the same rating is also tested to compare the measured efficiency with the simulated. Both the simulations and measurements shows that the efficiency decrease for quasi resonant battery chargers compared to the hard switched case. Furthermore, low frequency harmonics appear in the battery charger input and output currents. However, full control of the output voltage derivatives is obtained.

Acknowledgements

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Per Karlsson

Contents

1

Introduction

This chapter introduces electric vehicles and battery chargers for electric vehicles. Then, an introduction to the investigated concept is provided. Finally an overview of the thesis is given.

1.1 Background

Environmental aspects have made electric vehicles (EVs) an interesting challenger of the present Internal Combustion Engine (ICE) driven vehicles. Present electrical drives offers a reliable and environmentally sustainable solution to the pollution problems caused by the ICE driven vehicles. Almost all of the commercial automobile companies do indeed have a product range that also covers EVs. Anyway, today there is only a limited use of EVs for personal traffic. In Sweden, most of the EVs are used for community purposes such as postal delivery. However, also in these cases the EVs constitutes only a minor part of the vehicle fleet of these companies.

The main problem with EVs is that the batteries limit the maximum driving range, since present electro-chemical batteries do have a by far lower energy to weight ratio than gasolin.

Present EVs are equipped with an on-board battery charger. The on-board charger normally has a rather low power rating, since it is primarily intended for night-time battery charging at the owners residence. Usually, Swedish households are equipped with 16 A fuses, which limits the charging power to approximately 10 kW.

Today, this problem can be solved by the use of electro-hybrid systems, were an ICE is mechanically connected to an electrical generator charging the vehicle batteries. Some of these electrical hybrid vehicles (EHVs) also uses a part of the energy generated by the ICE for traction of the vehicle [38]. The idea is to charge the batteries when driving outside city area. The charging strategy can be optimised in such a way that the ICE is controlled to give minimum emissions or to minimise the fuel

consumption or other criteria [21]. However it is obvious that the pollution problem is only decreased, not eliminated by such a solution.

1.2 Fast charging

As previously mentioned, present EVs are equipped with on-board battery chargers, but in order to be able to compete with the ICE driven vehicles by means of daily driving range, a fast charging infrastructure is needed. There are however problems with the building of a fast charger infrastructure as well. First, the cost of chargers is high and second, designs based on diode or thyristor technology could result in current harmonics and voltage distortion [49].

Instead of diode or thyristor technology, fully controllable semiconductor devices, i.e. power transistors, should be used. Transistor equipped voltage source converters (VSCs) are often used for reliably operating speed control of electrical drives. The transistors are controlled by pulse width modulation (PWM) which gives a well defined output current spectrum [44].

If PWM controlled VSCs are used for battery chargers, the problem of grid frequency related distortion can be circumvented. However, the cost of the chargers and controllers increases since they become more complicated. Anyway, a broad introduction of electric vehicles opens a new market for the power semiconductor industry which probably results in a lower price for these devices.

In [36] it is stated that fast charging should be avoided in urban areas due to the fact that the deregulation of the power distribution market has resulted in retirement of several energy plants nearby cities, since it is cheaper to buy power than to run these plants. The electrical power bought on the market is generated at large hydro or nuclear power plants, which results in a low price. The problem is that stability problems might arise since such plants usually are located far away from urban area. Fast charging further increases this problem since the loading of the transmission lines becomes heavier, at all times during the day, thus resulting in higher peak power demands.

1.3 Charger infrastructure

One way to cope with the problem of the initial high cost of the charging infrastructure, is to make it advantageous both for the power delivering company and for the EV owners. It was previously mentioned that a

battery charger using a diode or thyristor based grid interface usually consumes non-sinusoidal current and thus injects harmonics into the grid. If a battery charger infrastructure is built solely on such chargers there would typically be problems like thermal overloading of transformers and shunt capacitors [39]. Furthermore, malfunction of equipment sensitive to disturbances is going to be a problem [39], [50]. If, on the other hand, battery chargers with a power transistor grid interface are used, they can be controlled to inject or consume currents of arbitrary waveform.

This means that the power grid interface can be used to consume harmonics in order to cancel harmonics injected by other loads. Also, reactive power can be generated or consumed by such a power grid interface. Single phase loads can be compensated for, which means that the current can be controlled in a manner were the higher voltage levels will experience the lower as consuming a balanced, harmonic free three phase current with power factor equal to one. These features forms what usually is called an active power line conditioner or active filter [4], [37].

There is one further possibility of such a system, which might be slightly provocative; the battery charger can be used to deliver power from the batteries back to the power grid. This is not likely to be used for the high power charging stations (gas station counterpart) except at emergency situations like during power system stability problems. This is due to the fact that, at the charging station the EV should be charged as fast as possible, without any delays, or there might be an queue situation.

For low power battery chargers at parking lots or office buildings etc., this active power capability can be interesting. At such places there will be occasions when the vehicle is connected to the battery charger for longer time than it takes to charge its batteries. For these occasions, an agreement between the EV owner and the payment system of the battery charger can be set. For instance, the agreement can say that the batteries might be discharged during the day but at a certain time they should be charged to a certain level and the charging energy price should be reduced to a certain level. Discharging the batteries shortens their lifetime which can be costly for the EV owner. This can be solved by a leasing agreement where the power delivering company owns the batteries, and the EV owner leases the batteries.

The agreement procedure indicated above results in no further complexity, since a payment system is needed anyway [39]. The payment system is based on communication between the battery management system (BMS) of the EV, the battery charger and a supervisory unit

which is needed both for billing and for operation of the battery charger as an active power line conditioner.

1.4 Battery charger topology

A wide variety of different converter topologies used for battery chargers do indeed exist. However, in order to meet the capabilities stated in the previous section, the range of circuits is reduced. Since this is a, from power electronic point of view, low to medium power application a voltage source converter is considered. The reason for this is that most transistor valves for this power range are designed for voltage source converters. Also, the simplicity of the voltage source converter compared to the current source converter (CSC) is an advantage.

In Figure 1.1 a voltage source battery charger is shown. Here, the charger is connected to the power grid via a LCL-filter. The line side stage of the battery charger is a three phase voltage source converter, acting as a controlled rectifier. The capacitor C_{dc} is referred to as the DC link capacitor, providing the voltage source feature. On the battery side, a half bridge converter is used to control the charging current fed to the vehicle batteries, via another LCL-filter.

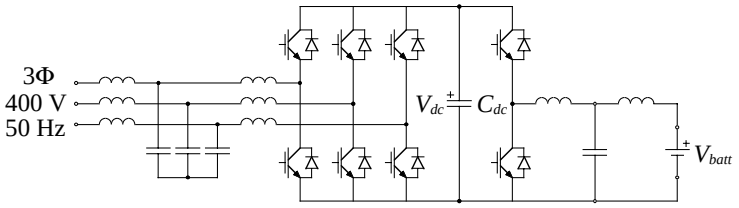


Figure 1.1 Voltage source battery charger. Note that the line and battery side filters are composed from LCL-combinations, forming third order filters.

The advantages of LCL-filters compared to the normally used L-filters are thoroughly discussed in [4]. In Appendix D.3 design of a LCL-filter inductor for a 75 kW battery charger according to Figure 1.1, implemented in [3], is discussed.

1.5 Resonant converters

A consequence of the previously mentioned active power delivery capability is that the efficiency of the battery charger becomes very important, since the energy price for energy delivered from the batteries to the power grid becomes considerably higher than the normal energy price, due to the wear cost of the batteries. It is often stated in the

literature [5], [13], [14], [32], that an increased efficiency can be achieved by using a resonant converter which provides reduced switching losses at the expense of an increased number of passive and in some cases also active devices. Furthermore, it is often pointed out that the device stress for the active devices are reduced for resonant converters [16], [28], [32].

There are several different types of resonant converters but the basic idea is that that the switch state should be changed only at low voltage across or at low current through the semiconductor devices, thus resulting in reduced switching losses. The rising and falling edges of these quantities can also be controlled to reduce interference problems.

For resonant power converters with low semiconductor device count, the resonant circuit is often comprised partly by the load [28], [30], [32], [35], [45], [59]. Here, these are referred to as load resonant converters. For bridge applications on the other hand, often one resonant circuit, inserted in between the passive energy storage device and the semiconductor bridge, is used to serve the entire bridge. This type of resonant converters are referred to as resonant DC link converters [13], [14], [22], [32], [43], [46], [47].

For the basic resonant converters the possible switching instants, i.e. when low device voltage or current is obtained, cannot be controlled. This means that carrier based PWM cannot be used for this type of converters. Only a sub-class of the resonant converters can be trigged on demand, referred to as quasi resonant converters [1], [2], [7], [9], [11], [15], [19], [41], [55], [56]. For a quasi resonant converter, the oscillation is interrupted in between two consecutive switching instants and is only started when a change of converter switch state is commanded.

For a battery charger with active power line conditioning capabilities, carrier based PWM is preferred due to its well known output current spectrum [44]. This means that if resonant power converter technology is to be used, quasi resonant DC link converters are the most interesting.

1.6 Outline of the thesis

In Chapter 2, basic properties of soft switching are discussed, starting from capacitive snubbers. The design expressions for quasi resonant DC link converter passive component selection are developed in Chapter 3. The design expressions are derived through thorough mathematical analysis of four different quasi resonant DC links. In Chapter 4, power electronic semiconductor devices in soft switching applications are

reviewed. Also, the simulation passive component models used in Chapter 5 are discussed. In Chapter 5, battery chargers equipped with the quasi resonant DC links investigated, are simulated. The quasi resonant converters simulated, are designed to have equal properties, at least in some aspects. The simulations are intended to verify the design expressions and also for calculation of the efficiency of the different battery chargers. In Chapter 6, one of the simulated battery chargers is implemented and tested. Chapter 7 concludes the thesis.

Note that this thesis is one of two, evolved from the battery charger project. The accompanying thesis [4], treats control and functional aspects of the battery charger, while this thesis focuses on hardware related aspects.

2

Resonant converters

The present resonant converter topologies do indeed exist in a wide variety of forms. However, they all originate from attempts to avoid simultaneously high voltage across and high current through the semiconductor devices when the device traverses from conducting to blocking state or vice versa. Another advantage of resonant converters often addressed in the literature, is the ability to control the time derivative of the voltage and/or the current. On the other hand, resonant converters introduces new problems. This chapter gives an introduction to the evolution of resonant converters, from load resonant converters to quasi resonant DC link converters. Though not resonant, this presentation starts with a short introduction of a certain kind of snubber, the RCD charge-discharge snubber, which exhibits some of the features of resonant converters.

2.1 The RCD charge-discharge snubber

In this section the RCD charge-discharge snubber is investigated. This is mainly done in order to introduce the term soft switching. The investigation starts with a presentation of the hard switched step down converter. Then, a capacitive snubber is introduced. This is followed by the introduction of the full RCD charge-discharge snubber applied both for the step down converter and a transistor half bridge.

Hard switching

One of the most basic transistor bridge configurations for power electronic applications is the step down converter. It consists of a voltage source (DC link capacitor), a power transistor (IGBT in this case) and a freewheeling diode, see Figure 2.1. Since this is a voltage source converter, the load is a current source, i.e. inductive. When the state of the switch is changed from on to off (turn-off) or from off to on (turn-on), the transition will take a finite time in the non-ideal case. Furthermore, for non-ideal circuits there are parasitic components, for

example stray inductance that can cause overvoltage across the semiconductor devices at turn-off.

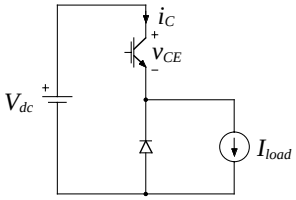


Figure 2.1 Basic step down converter used in the analysis.

Figure 2.2 shows typical collector current and collector-emitter voltage for a power transistor (IGBT in this case), when used in the step down converter above. Note that the collector current and collector-emitter voltage is expressed in p.u., where the normalisation values are selected as the rated maximum continuos collector current, I_C, and maximum collector-emitter voltage that can be sustained across the device, V_{CES}. In the simulation of the step down converter the DC link voltage V_{dc} and load current I_{load} are selected as

$$\begin{cases} I_{load} = 0.8 I_C \\ V_{dc} = 0.6 V_{CES} \end{cases} \tag{2.1}$$

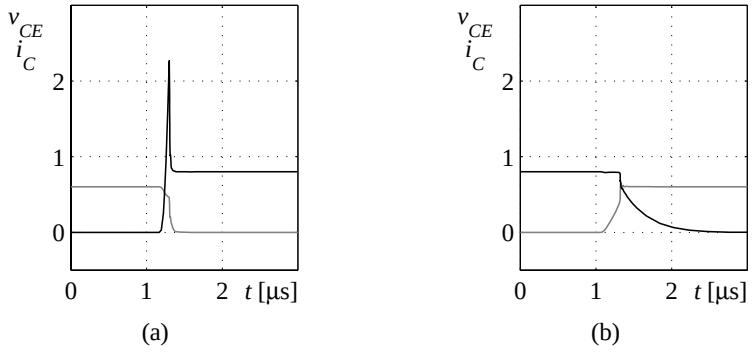


Figure 2.2 Time-signals showing normalised transistor current (black) and voltage (grey) at (a) turn-on and (b) turn-off of the power transistor in the step down converter.

In Figure 2.2, the power transistor is exposed to a current spike at turn-on which is due to reverse recovery of the freewheeling diode. Furthermore, it is clearly seen that the IGBT is exposed to simultaneously high current and voltage at the switching instants. This leads to high switching losses, especially at turn-off since the IGBT exhibits a collector

current tail here. The physics of reverse recovery of a power diode and the IGBT current tail are discussed in Chapter 4.

A common way to visualise the stress levels imposed on a power electronic semiconductor device is to plot the switching trajectories, i.e. current versus voltage, on top of the safe operating area (SOA) of the device. The power semiconductor manufacturers specify the SOA on absolute maximum values that must not be exceeded. However, in some cases there are two SOAs, the second valid only for very short pulses (transients). Figure 2.3 shows the switching trajectories corresponding to the time signals in Figure 2.2 on top of the SOA for the particular IGBT used in the simulation of the step down converter above.

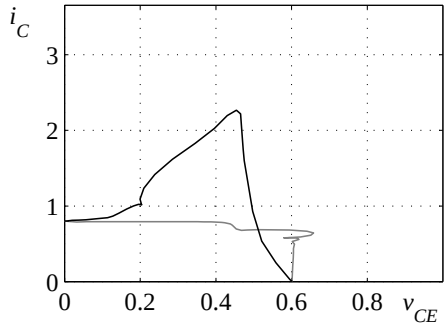


Figure 2.3 Switching trajectories (turn-on black and turn-off grey) of an IGBT in a step down converter application. The total area corresponds to the safe operating area valid for short pulses.

The switching trajectories in Figure 2.3 shows that there are no problems with overvoltage or overcurrent extending outside the SOA. The duration of the time intervals where the power transistor is exposed to high current and voltage simultaneously, causing high losses, is however not seen. This can only be seen in Figure 2.2. Both these plots are valuable since either of them are delimiting to what extent, by means of transferred power, the power converter can be used.

In some cases, the circuit stray inductance can be high causing a high overvoltage at turn-off, which means that there must be a large margin between the DC link voltage used and the rated voltage. In other cases the switching losses can be high causing a low value of rated converter current in order to keep the junction temperature of the power transistor at an acceptable level.

To partly overcome this problem and be able to use the semiconductor devices in a more efficient way, snubber circuits are introduced [44], [62],

[63]. There are several different snubber circuits used for different purposes, for example to reduce the overvoltage caused by stray inductance, at turn-off. There are also snubber circuits where the aim is to move the switching loci further into the SOA, which means lower losses, at least if the duration of the switching intervals are not prolonged. One such snubber is the RCD (resistor, capacitor, diode) charge-discharge snubber.

The capacitive snubber

From now on the RCD charge-discharge-snubber is referred to only as RCD snubber, even though there are several types of RCD snubbers for different purposes. At turn-off, this snubber behaves as a pure capacitor. Therefore, in order to simplify the preliminary analysis, the snubber is considered as consisting only of a single capacitor denoted C_s in Figure 2.4.

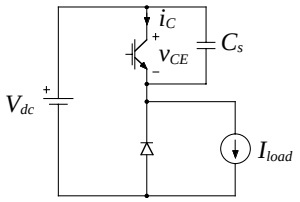


Figure 2.4 The step down converter with a purely capacitive turn-off snubber.

By introducing a capacitor across the power transistor output terminals, the voltage derivative with respect to time can be controlled, see for example [44]. This is possible since at turn-off, a part of the transistor current finds an alternative path through the capacitor, which means that the transistor collector current falls and the collector-emitter voltage rises simultaneously, see Figure 2.5. This is not possible in the previous case, i.e. without a snubber, since here the only alternative way for the load current is through the freewheeling diode.

The freewheeling diode only carries substantial current when forward biased, which means that the transistor collector-emitter voltage must be approximately equal to the DC link voltage, V_{dc}, before the collector current can begin to decline at turn-off for the case without a snubber.

It is sometimes stated that this type of snubber circuit provides turn-off under zero voltage switching (ZVS) conditions, or soft switched conditions [52]. This refers to the fact that when the turn-off sequence is initiated, the collector-emitter voltage is approximately zero. However, at

the end of the current fall interval the collector-emitter voltage is high, ideally equal to the DC link voltage V_{dc}, according to [44].

Converters not using snubbers providing soft transitions neither at turn-on or turn-off, are often termed hard switched [32], [52]. Another characterisation of soft switching is also used in this context, zero current switching (ZCS), which refers to that either or both the turn-on and turn-off transitions take place at virtually zero current [35], [44].

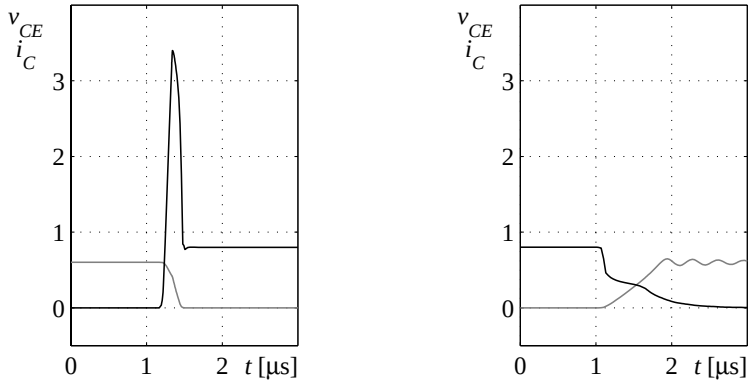


Figure 2.5 Time-signals showing transistor current (black) and voltage (grey) at (a) turn-on and (b) turn-off of the power transistor in the step down converter with a capacitive snubber across the power transistor. Note the high collector current peak at turn-on, and that the collector current and collector-emitter voltage changes simultaneously at turn-off.

From Figure 2.5 it is seen that the snubber capacitor is affecting the turn-off waveforms in such a way that the turn-off losses do decrease. Also, the collector-emitter voltage derivative is controlled which can be an important aspect by means of electromagnetic compatibility (EMC) [51]. On the other hand, it is also seen that the turn-on waveforms becomes less favourable.

For the hard switched step down converter there was a short collector current spike due to reverse recovery of the freewheeling diode at turn-on of the power transistor. For the case with a capacitive snubber the current spike is even higher, thus adding stress to the transistor at turn-on.

Prior to turn-on, the snubber capacitor is fully charged, i.e. the capacitor voltage equals V_{dc}. The voltage across the freewheeling diode remains close to zero as long as its junction is forward biased, which implies that

the capacitor voltage, and thereby the collector-emitter voltage, cannot decrease before the pn-junction of the freewheeling diode becomes reverse biased. The freewheeling diode becomes reverse biased exactly when the reverse recovery current reaches its peak value.

Reverse recovery is due to stored minority charge carriers close to the pn-junction of the diode, causing the junction to be forward biased even though the diode current is negative. The negative current sweeps out the minority carriers and eventually the junction becomes reverse biased. As mentioned earlier, power electronic diodes and IGBTs are investigated further in Chapter 4.

The discussion above implies that the capacitor discharge starts when the reverse recovery current reaches its peak. Even if the diode recovers fast, the transistor has to carry an excessive current for quite some time since the only discharge path for the capacitor is through the power transistor.

The RCD snubber

In order to cope with the problem of the capacitive snubber, a resistor is added. The intention with the resistor is to limit the capacitor discharge current at transistor turn-on. A diode is placed in parallel with the resistor since at turn-off, the capacitor gives the desired behaviour and the resistor would only cause increased losses. This completes the RCD snubber, see Figure 2.6.

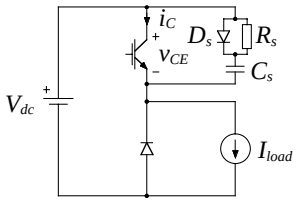


Figure 2.6 The step down converter with the full RCD charge-discharge snubber placed across the output terminals of the device.

The resistor value is chosen in such a way that the capacitor peak discharge current do not exceed the peak reverse recovery current of the freewheeling diode [44]. Figure 2.7 shows the time signals of the transistor collector current and collector-emitter voltage. It is clearly seen that the turn-off sequence is similar to the one for the purely capacitive snubber, but the stress levels at turn-on is only slightly higher than it was for the hard switched step down converter.

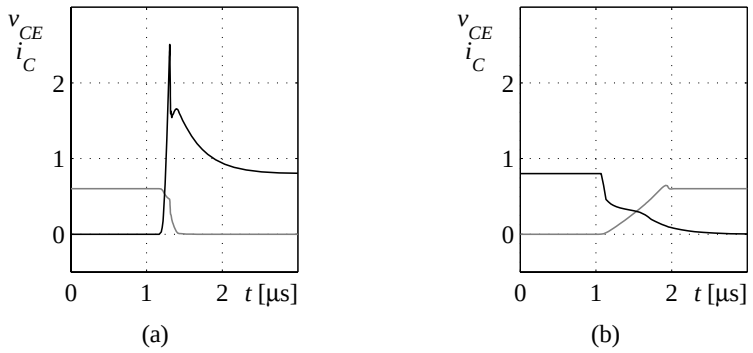


Figure 2.7 Time-signals showing transistor current (black) and voltage (grey) at (a) turn-on and (b) turn-off of the power transistor in the step down converter with a full RCD charge-discharge snubber across the power transistor.

The RCD charge-discharge snubber in bridge applications

The battery charger proposed consists of four half bridges with two IGBTs and two freewheeling diodes each, see Figure 1.1. To investigate the switching waveforms for a battery charger implemented with RCD snubbers, one across each IGBT, an entire half bridge has to be considered. In Figure 2.8 a half bridge with a RCD snubber across each transistor is shown.

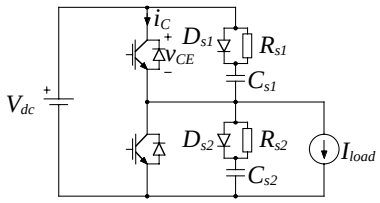


Figure 2.8 A half bridge with one RCD snubber connected across each transistor.

The upper RCD snubber is intended to provide soft turn-off for the upper IGBT. The lower RCD snubber is intended to provide soft turn-off for the lower IGBT. The simulated collector current and collector-emitter voltage are shown in Figure 2.9. Note the very high current peak at transistor turn-on.

The occurrence of this current peak is due to the capacitive current path seen from the IGBT output terminals, [44]. At turn-on of the upper IGBT, the collector-emitter voltage should decrease for the upper IGBT and increase for the lower. This means that the upper snubber capacitor in

Figure 2.8, denoted C_{s1}, should be discharged and the lower, denoted C_{s2}, should be charged.

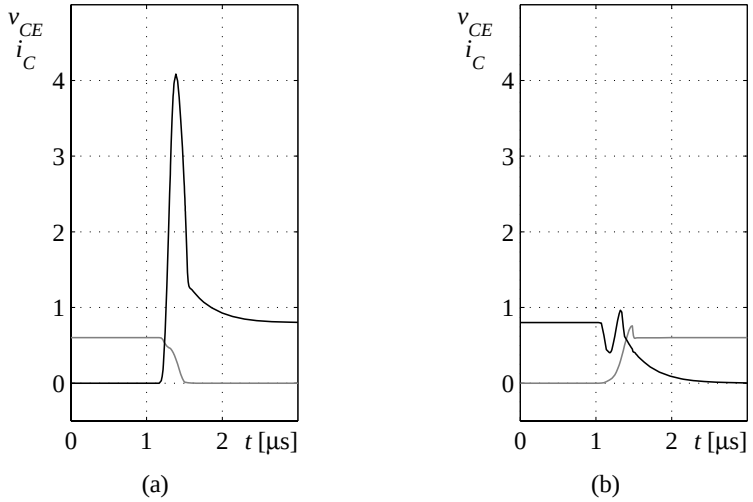


Figure 2.9 Time-signals showing transistor collector current (black) and collector-emitter voltage (grey) at (a) turn-on and (b) turn-off of the upper IGBT in the converter consisting of a bridge leg. One RCD snubber is used across each IGBT. Note the high collector current peak at turn-on. Also note the poor behaviour at turn-off.

The discharge current of C_{s1} is limited by the snubber resistor R_{s1} as previous but the charging current of C_{s2} is not limited by any other component. Furthermore, the only path possible for the charging current, is through the upper IGBT. In this way, the charging current of the lower snubber capacitor gives a large contribution to the collector current of the upper IGBT, at turn-on. The same problem appears for the lower transistor.

Another problem seen in Figure 2.9 is that the turn-off is not soft, i.e. the collector current fall and the collector-emitter voltage rise do not occur simultaneously. Instead, the collector current falls somewhat, then increases and eventually the current falls again. This is referred to as a current tail bump, which is discussed in Chapter 4.

The switching loci for the converter consisting of a bridge leg with RCD snubbers across the transistors is shown in Figure 2.10. Note that the switching trajectory is outside the SOA valid for very short pulses, which is very dangerous, since this can lead to device failure.

Small variations of the snubber circuit can be used to partly solve this problem. First, the snubber diodes in parallel with the resistors can be removed. In this way the capacitive path is broken but soft turn-off is also lost. However, EMC related problems can still be reduced [44].

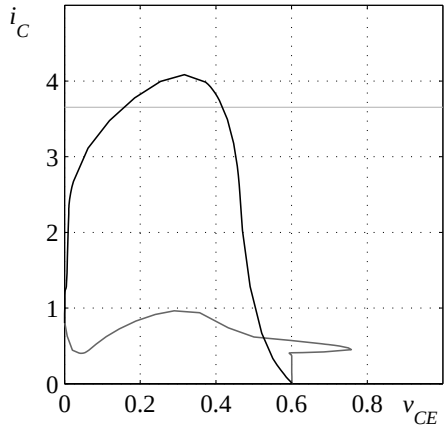


Figure 2.10 Switching loci (turn-on black and turn-off dark grey) of the bridge leg with RCD snubbers. Note that the turn-on collector current is beyond the current limit of the dynamic SOA (light grey), valid for short pulses.

Another way to solve this problem is by introducing inductors in series with the snubbers, thus reducing the current derivative with respect to time [63]. This works, but gives a bulky snubber. This is not desirable, especially not since eight such snubbers are needed for the battery charger considered.

2.2 Load resonant converters

The next step is to investigate load resonant converters. The name load resonant converter refers to the fact that for this type of converters, the load is part of the resonant circuit. There are basically two different types, the series and the parallel resonant converters. In this section both these, also referred to as class D converters, are discussed. According to [28] the class D resonant converters were invented by P.J. Baxandall in 1959.

The idea of resonant converters is to provide soft switching in order to be able to increase the switching frequency. An increased switching frequency means that the passive filter requirements and/or the output current ripple are decreased. Also, switching frequencies beyond the

audible limit of the human ear can be used, thus reducing the disturbing noise of the converter.

The series resonant converter

The series resonant converter consist of one or two half bridges forming a half or full bridge converter. Between the output terminals, a series resonant circuit is connected. This series resonant circuit consists of an inductor, a capacitor and a resistor, with one or more of these elements actually being part of the load. Usually, at least the resistor is part of the load. However, for this basic circuit only AC-power can be delivered to the load, due to the resonant behaviour of the circuit. If a DC-load is used, the resistor can be replaced by a rectifier connected to the DC load.

If the load is directly connected to the resonant circuit, i.e. without a rectifier in between, it is referred to as a series resonant DC to AC converter. If the load is connected to the converter via a rectifier, it is referred to as a series resonant DC to DC converter. The basic series resonant DC to DC full-bridge converter is shown in Figure 2.11.

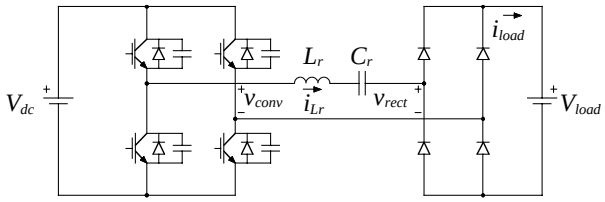


Figure 2.11 Series resonant DC-DC full-bridge converter. In this case the load consist of a constant voltage source, i.e. an ideal battery.

Besides the basic components previously discussed, the converter in Figure 2.11 is also equipped with loss-less snubbers, i.e. capacitive snubbers, which are discussed later. The rectifier is connected in series with the resonant circuit which acts as a current source for the rectifier. Since the rectifier is current fed, the rectifier output should appear as a voltage source.

Load resonant circuits are often [28], [44] characterised upon the fundamental of the excitation frequency fed by the converter. The behaviour of the circuit is varying depending on whether the converter output frequency is below, at or above the resonance frequency of the LC circuit [28], [44]. The resonance frequency is given by

$$\omega_r = 2\pi f_r = \frac{1}{\sqrt{L_r C_r}} \tag{2.2}$$

Figure 2.12 shows the waveforms of the series resonant converter operating at switching frequency above the resonance frequency.

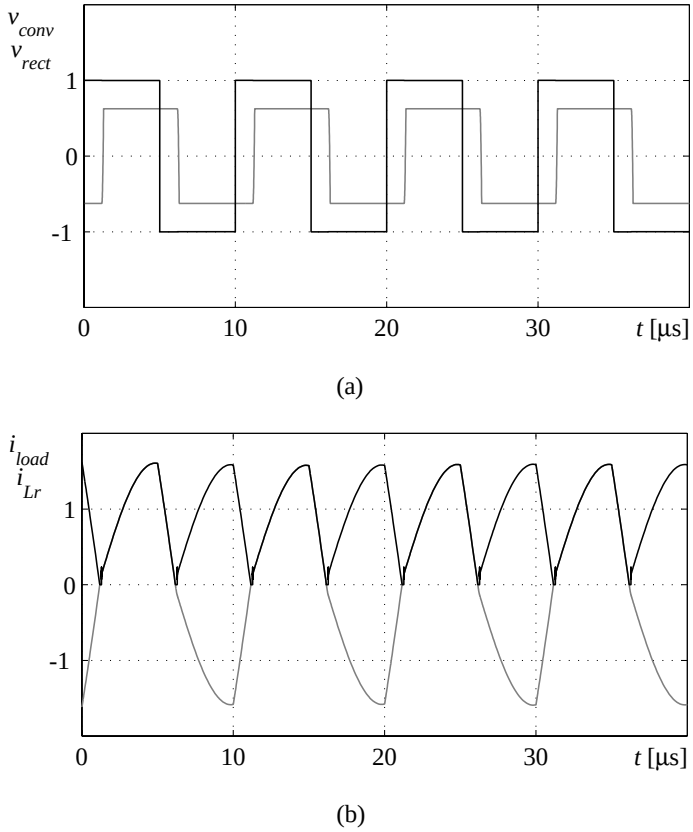


Figure 2.12 Normalised voltages (a), converter output voltage (black) and rectifier input voltage (grey). Normalised currents (b), load current (black) and resonant current (grey). Note that the resonant current is lagging the fundamental of the converter output voltage.

The quantities in Figure 2.12 are normalised to a p.u. system with base values selected according to

$$\begin{cases} I_{base} = I_{load,\,avg} \\ V_{base} = V_{dc} \end{cases} \tag{2.3}$$

The shape of the waveforms, especially the resonant current in the case of a series resonant converter, are strongly dependent on the loaded quality factor, Q_L, defined as

$$Q_L = \frac{Z_r}{R_{eq}} \tag{2.4}$$

where

$$Z_r = \sqrt{\frac{L_r}{C_r}} \tag{2.5}$$

In [28] it is stated that the resonant current i_{Lr} is almost sinusoidal if Q_L is larger than 2.5. For a non-linear load, an equivalent loaded quality factor have to be calculated.

For the converter in Figure 2.11, with waveforms as in Figure 2.12, an equivalent load resistance is calculated based on the amplitude of the fundamental of the rectifier input voltage, which is proportional to the battery voltage. It is also assumed that the resonant current is sinusoidal.

In this example, a Q_L of 1.5 and a resonance frequency of 66.7 kHz are desired. These two parameters together with the equivalent series resistance gives the component values of L_r and C_r. The reason for selecting a low Q_L is that this gives a low resonant current and a low resonant capacitor voltage v_{Cr} [28], [35].

For the series resonant converter, a switching frequency lower than the resonance frequency means that the resonant circuit behaves like a capacitive load. Switching frequency higher than the resonant frequency means that the resonant circuit appears as an inductive load for the converter. Thus, at switching frequencies below resonance, the resonant current i_{Lr} leads the fundamental of the converter output voltage. Consequently, i_{Lr} lags the fundamental of the converter voltage when the resonant circuit is excited above the resonance frequency.

For continuos load current this means that below resonance frequency the converter switches are turned on in a hard switched manner and turned off under ZVS and ZCS conditions. Above resonance the converter switches are turned on under ZVS and ZCS conditions and turned off under hard switched conditions. Loss-less turn-off above resonance is provided by the individual snubber capacitors in parallel with each converter switch, as shown in Figure 2.11.

Previously when ZVS turn-off snubbers were discussed, it was found that the use of capacitive snubbers mounted across each transistor in a half bridge, resulted in high collector current peaks at turn-on. However, in the case of a series resonant converter this problem is not observed due to

the fact that the transistors turn-on at ZVS and ZCS conditions since the diode in parallel with the transistor is carrying the resonant current, prior to turn-on. The resonant current commutates to the transistors when its sign changes. This implies that transistor turn-on do not change the charge state of the snubber capacitors, and consequently no snubber capacitor charging current is carried by the transistors.

Although this circuit was invented already in 1959, the series resonant converter is still a research object [28], [45]. Also variants of this circuit together with the circuit discussed in the next section, the parallel resonant converter, is gaining a lot of interest [28], [30], [44].

In [35], [45] the series resonant converter is used in a somewhat different way than previously described. Here, the series resonant circuit is operated well below resonant frequency and with discontinuous resonant current. Although the circuit presented in [35] do not look exactly as a series resonant in Figure 2.11, it is still a series resonant DC to DC converter.

The idea of operating the series resonant converter below resonance and with discontinuous current is that turn-on and turn-off is performed under (virtually) ZCS conditions. The reason for this is that the resonant current is only piecewise sinusoidal, with intervals approximately equal to zero in between. In [35] it is stated that these intervals are not equal to zero, since a transformer is connected between the resonant circuit and the rectifier, which gives rise to a small magnetising current during the discontinuous current intervals. Anyway, the converter switches are operated at low current.

The parallel resonant converter

The parallel load resonant converter is similar to the previously investigated series resonant converter. However, in the case of a parallel resonant converter, the output rectifier is connected in parallel with the resonant capacitor, see Figure 2.13. Since the resonant capacitor represents a voltage source to the rectifier, the output filter of the rectifier must be a current source, i.e. inductive. The rectifier represents a non-linear load, also in this case. Usually, a transformer is connected between the resonant circuit and the rectifier in order to adapt the load voltage to the DC link voltage used. A transformer can also be used to provide a galvanically isolated output voltage, which is desired in some applications.

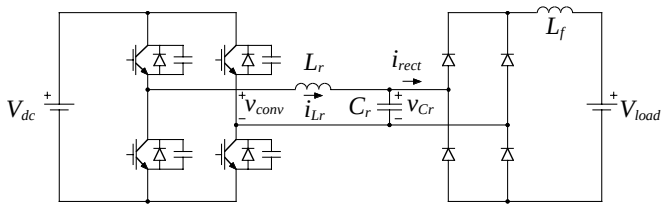
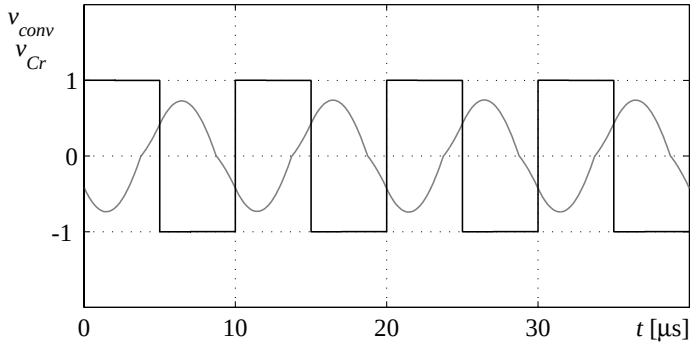
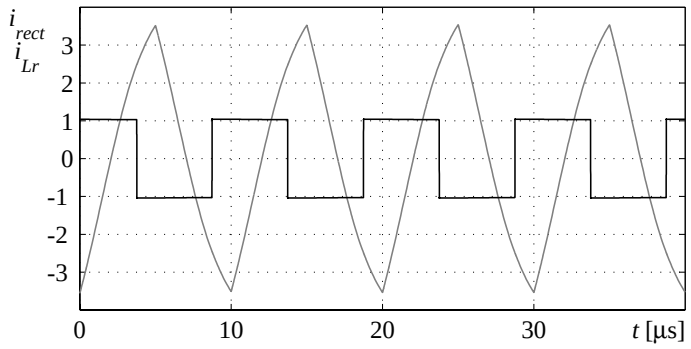


Figure 2.13 The parallel resonant converter with a constant voltage load. Note the capacitive snubbers connected across the converter switches providing loss-less turn-off. Often a transformer is connected between the resonant circuit and the rectifier.

The resonant waveforms of the parallel resonant converter in Figure 2.13, operating at switching frequency above resonance are shown in Figure 2.14. Here, the waveforms are normalised according to (2.3).



(a)



(b)

Figure 2.14 Normalised voltages (a), converter output voltage (black) and resonant capacitor voltage (grey). Normalised currents (b), load current (black) and resonant inductor current (grey).

Unlike the case with the series resonant converter, the resonant inductor current is not determined by the rectifier output current for the parallel resonant converter. On the other hand, the rectifier output voltage is dependent on the resonant capacitor voltage for the parallel resonant converter.

For the parallel resonant converter, continuos current operation above resonance results in turn-on at ZCS conditions since the resonant current commutates from the freewheeling diodes to the power transistors naturally. In this case, natural commutation means that the commutation takes place at the zero crossing of the resonant inductor current.

Transistor turn-off however, is not performed under neither ZCS or ZVS conditions, unless loss-less turn-off snubbers are used. As before, the capacitive snubbers provide turn-off at low voltage. Similar to the case for the series resonant converter, there is no current peak occurring with such snubbers at turn-on of the converter switches for the parallel resonant converter.

The main problem of both the series and the parallel resonant converters, is that the resonant currents and voltages can be several times higher than the average load current and DC link voltage respectively, depending on the load. If large load variations are likely, the components of the resonant converter must be designed for the worst case stress.

Several variations and combinations of the series and parallel resonant converters do exist [28], [44]. There are also completely different resonant converters like the class E resonant converters [28], [44] and the zero voltage transition (ZVT) converters [24]. However, there are so many resonant converter topologies that a complete review would be very extensive. Furthermore, the research on resonant converters is widespread which also makes a complete survey difficult.

2.3 The resonant DC link converter

A huge step in resonant converter technology was taken in 1986 when the resonant DC link converter was invented [13], [14]. For the resonant DC link converter, one resonant circuit is used to provide soft switching for the entire converter. As the name resonant DC link hints, it is the DC link which is forced to oscillate. This means that the resonance circuit is located on the DC link side and not on the load side of the converter. This is very useful, especially for three (or more) phase converters since otherwise, one resonant circuit for each half bridge would be required.

The basic three phase resonant DC link converter is shown in Figure 2.15. If a three phase back-to-back converter [6] is to be implemented with a resonant DC link, this is done by connecting the six half bridges in parallel [13]. In [13] another solution for the resonant back-to-back converter is also presented where a current fed H-bridge is used. This circuit requires four extra switches and is not considered here.

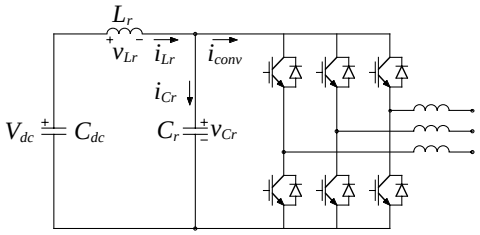


Figure 2.15 The basic three phase resonant DC link converter.

In order to investigate the resonant DC link converter, a simplification of the converter in Figure 2.15 is done. Instead of the three phase converter, a piecewise constant current source is connected across the DC link representing the current fed to the converter. However, one switch must be kept across the DC link since a path for the circulating resonant current has to be provided. The simplified resonant DC link converter is shown in Figure 2.16.

The idea of the resonant DC link converter is that the switch state of the converter only should be changed at or close to zero link voltage. This implies that the current drawn by the current source in Figure 2.16, should change only at low DC link voltage. The resonant circuit is formed by the resonant inductor L_r and the resonant capacitor C_r. Since the DC link capacitor C_{dc} has a much higher capacitance than C_r, it does not affect the resonance behaviour. In other words, the DC link capacitor can be regarded as a constant voltage source.

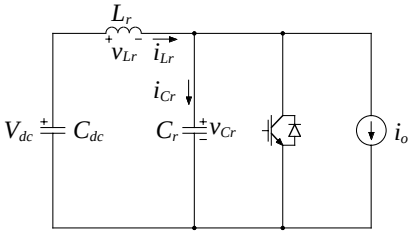


Figure 2.16 Simplified resonant DC link converter.

Assume that a resonant cycle starts at a capacitor voltage equal to twice the DC link voltage V_{dc}. Due to the resonant properties of this circuit the capacitor voltage decreases towards zero. When the voltage across C_r passes the level of the DC link voltage the inductor current is close to its minimum value.

When the capacitor voltage reaches zero, it will be clamped to this level due to the fact that the load current freewheels through the freewheeling diodes, at least if the resonant inductor current is lower than the load current which is the case if no switching is performed.

As soon as the inductor current reaches the level of the load current, the capacitor voltage starts to ramp up. When the voltage across C_r passes the level of the DC link voltage the inductor current is at its maximum value. For the case where the output current is not changed, the capacitor voltage reaches the starting point of the analysis which equals twice the DC link voltage. The resonant DC link converter is mathematically analysed in Appendix C.2.

The normalised resonant waveforms for the case of changing output current are shown in Figure 2.17. From Figure 2.17 some interesting observations are made. First, when the output current i_o is decreased due to a change of the converter switch state, the resonant DC link voltage resonates to a peak value higher than twice the DC link voltage V_{dc}. Second, when the output current is increased, the zero voltage interval is prolonged and the resonant capacitor voltage increases with a moderate derivative, to a peak value close to twice the DC link voltage V_{dc}.

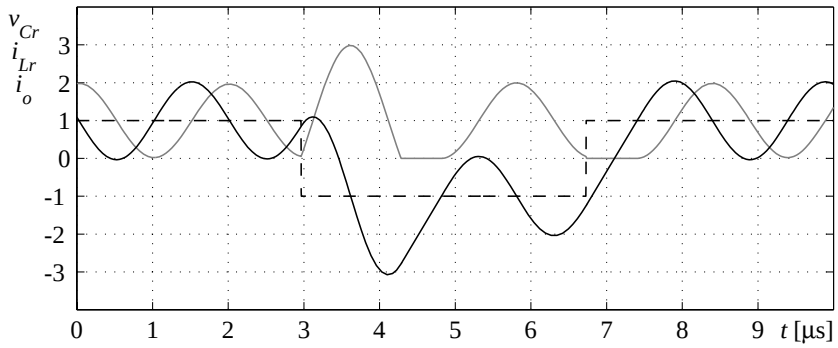


Figure 2.17 Normalised inductor current (black) and resonant link voltage (grey) for a resonant DC link converter. The current fed to the converter is also shown (dashed). Note the resonant link voltage peak resulting from a decrease of the converter current.

In the first case, there is excess energy stored in the resonant inductor due to the previously high current through L_r, corresponding to the load current. This energy must decrease to meet the new output current, which implies that the energy must be transferred to the resonant capacitor C_r. This excess energy thus results in a high voltage across the capacitor. By increasing the capacitance and decreasing the inductance, the peak capacitor voltage is decreased. However, the same action increases the magnitude of the resonant current through L_r.

Also the derivative of the voltage ramp up interval can be controlled by selection of the inductance and capacitance of the resonant circuit. This is important in motor drive applications since it has been found that high voltage derivatives shortens the lifetime of the winding insulation of motors [46], [47], [53].

In the second case, a too small amount of energy is stored in the inductor, which results in a prolonged zero voltage interval. The length of the zero voltage interval is determined by the time needed for the inductor current to reach the same level as the converter current. When the inductor current reaches the level of the converter current, the resonant capacitor is being charged, since the inductor current continues to rise. Since the capacitor charging current is low and controlled by the inductor in this case, the voltage is increasing with a moderate derivative. The capacitor voltage only reaches about twice the DC link voltage, which is due to the fact the voltage rise interval starts at zero voltage with zero charging current.

If the resonance frequency of the DC link is much higher than the switching frequency the oscillation might be damped which means that after some resonance cycles, zero voltage will not be reached. This damping is due to losses of the passive components. One way to cope with this problem is to maintain the zero voltage interval somewhat longer by short circuiting the resonant capacitor with the converter switches. This forces storage of more energy in the resonant inductor which in turn results in higher capacitor peak voltage.

Another problem of this circuit is that carrier wave PWM can not be used since the possible switching instants are determined by the resonant circuit. Instead other modulation strategies must be applied [13]. One such modulation strategy is reviewed in Appendix A. However, these modulation strategies require that the resonance frequency is much higher than the switching frequency, in order to get a result comparable to carrier based PWM by means of output current spectrum [46], [47].

Several other resonant link circuits are presented in the literature. Both AC and DC link circuits are developed and also ZVS and ZCS resonant circuits are available. Anyway, the rest of this report only deals with resonant DC link circuits intended for providing ZVS condition at transistor switching.

Clamp circuits

There are mainly two problems associated with the resonant DC link converters. One problem is that PWM cannot be used, which as previously mentioned can be solved by increasing the resonant link frequency. The other problem is the capacitor voltage overshoot following a change of switch state that decreases the current fed from the DC link to the converter. This can be solved by allowing the change of switch state at a slightly higher voltage than zero [46], [47], see Appendix C.2. By using this voltage peak control (VPC), a capacitor peak voltage only slightly higher than twice the DC link voltage is obtained, even at converter switchings resulting in a decrease of the resonant link output current.

The other way is to use a clamp circuit, which assures that the maximum capacitor voltage is limited to a certain level by an external circuit. Two methods of clamping are proposed in the literature, active and passive clamping. Active clamping [14], [22], utilises a capacitor and an auxiliary switch to provide clamp action, see Figure 2.18. Here, the resonant DC link voltage is limited to a level determined by the voltage across the clamp capacitor C_c. When v_{Cr} reaches $K \cdot V_{dc}$, the anti-parallel diode of S_{aux} starts to conduct. Thus, the resonant link voltage is clamped to this value. The parameter K is called clamping factor.

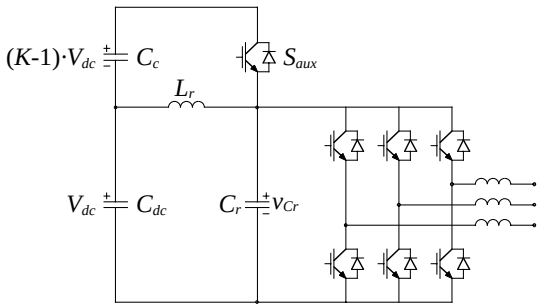


Figure 2.18 Active clamp circuit for the resonant DC link converter.

Note that during clamp action, the capacitor C_c is charged, implying that the clamping voltage will increase if no precautions are made. To solve

this problem the controllable part of S_{aux} has to be operated during the off-clamping intervals of the resonant cycle. If this is done appropriately the clamping voltage can be controlled to be almost constant. The idea is to turn on the transistor of S_{aux} while the diode is conducting, which means that this occurs at zero voltage. Then, S_{aux} is kept on in order to discharge the clamp capacitor in such a way that the voltage across C_c returns to the value determined by the clamp factor. According to [14], a suitable value for the clamp factor is between 1.2 and 1.4.

In the case of passive clamping [14], a transformer is used to achieve the desired limitation of the resonant link voltage, see Figure 2.19. In this case the idea is that the clamp diode D_2 should be reverse biased for resonant link voltages less than the clamp level. When the resonant link voltage reaches the clamp level, D_2 should be a the edge of forward biasing. This is obtained by a proper selection of the clamping transformer turns ratio, since at this point the secondary voltage equals V_{dc} and the primary voltage equals $(K\text{-}1)\cdot V_{dc}$. Thus, the clamp transformer winding turns ratio should be selected according to

$$\frac{N_1}{N_2} = \frac{1}{K-1} \tag{2.6}$$

where N_1 and N_2 are the number of winding turns for the clamp transformer primary and secondary, respectively. The clamping factor can however not be chosen arbitrarily, since it has to be granted that the resonant link voltage fulfils the oscillation all the way down to zero voltage. This implies that the clamping factor can not be less than two [14], for the passively clamped resonant DC link.

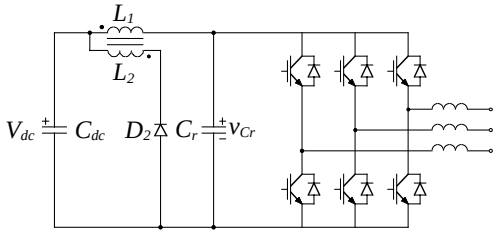


Figure 2.19 A passively clamped resonant DC link converter.

One major problem with this circuit is that D_2 has to sustain a high reverse voltage during the resonant DC link zero voltage interval. This voltage equals

$$V_{RM} = \left(1 + \frac{N_2}{N_1}\right) V_{dc} \tag{2.7}$$

Thus, for a clamping voltage equal to two, the diode has to be able to withstand a reverse voltage equal to three times V_{dc}. There are also other problems associated with passive clamping, which are discussed in later chapters.

Passive clamping is closely related to regenerative snubbers. In fact, the passive clamping network is identical to a regenerative snubber found in [63].

2.4 Quasi resonant DC link converters

In this section quasi resonant DC link converters are introduced. The words quasi resonant refers to the fact that these circuits are not continuously oscillating, but can be triggered by active components to perform a resonant cycle.

Here, the circuits are presented in a basic manner, which in this case means that no mathematical derivation is performed and no waveforms are shown. Instead this is shown in the next chapter.

Of course, there are several quasi resonant DC link converters not discussed here. For example, circuits where more than two auxiliary switches are needed [19], [20], are not considered. The circuit presented in [11], [31] is not discussed here since it is similar to the one presented in [40], [41], which is discussed here. The circuit investigated in [12], [56], [57], [58] is not discussed here due to its high passive component count.

The passively clamped two switch quasi resonant DC link converter

The first circuit investigated is a passively clamped two switch quasi resonant converter presented in [7], see Figure 2.20. Further work have been carried out, focusing on implementation [8] and modulation issues [17]. The circuit has also been further developed resulting in a new circuit [9], which is discussed later on. The passive clamping circuitry is recognised from the previous section. However, the inductor L_2 and the transistors S_1 and S_2 together with the diodes D_1 and D_2 are added. Actually, the trig on demand ability is formed by these components.

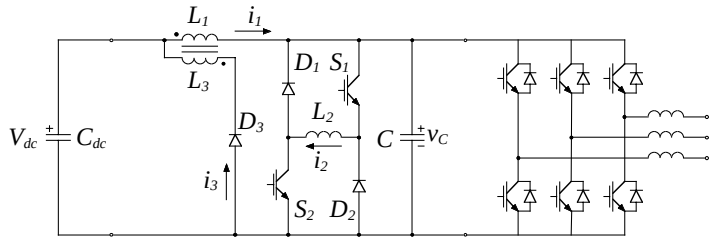


Figure 2.20 The passively clamped two switch quasi resonant DC link three phase converter.

When a change in converter switch state is commanded by the modulator, S_1 and S_2 are simultaneously turned on. Since these transistors are connected in series with L_2, across the resonant link capacitor C, a discharge path for C results. Note that S_1 and S_2 are turned on in a ZCS manner, since the current i_2 is zero initially. As the link voltage ramps down, the energy stored in C is transferred to L_2, causing an increase of the current through this inductor.

When C is discharged to zero voltage, i_2 saturates but i_1 continues its increase since the full DC link voltage is applied across L_1. As long as the transistors S_1 and S_2 are kept on, zero voltage is maintained and i_1 is increasing at a constant rate. As soon as zero link voltage is obtained, the commanded switching state is set (ZVS). The duration of the zero voltage interval is selected to fulfil safe operation, i.e. to avoid shoot through of the main circuit transistors. However, a very long duration of the zero voltage interval results in a high current through L_1, which not only results in high losses but also implies that a large amount of energy is stored in the resonant circuit. The latter problem is discussed in later sections.

When the transistors S_1 and S_2 are turned off, the current i_2 commutates from these transistors to the diodes D_1 and D_2. This commutation occurs under ZVS conditions. The energy stored in the inductor L_2 is transferred to the capacitor C, which implies that the resonant link voltage begins to ramp up. When the capacitor voltage reaches the clamp level, determined by the turns ratio of L_1/L_3, it becomes clamped and the resonant excess energy is transferred to the secondary winding of the clamping transformer, i.e. L_3.

During the clamping interval, the current i_3 decreases at a constant rate determined by the clamp transformer secondary side self inductance, L_3, and the DC link voltage. When i_3 has declined to zero, the clamping

interval ends. Thus, the duration of the clamping interval is determined by the amount of resonant excess energy at the start of the interval.

For this quasi resonant converter, a suitable choice of clamping factor is between 1.1 and 1.3, according to [7]. This is considerably lower than the value necessary for the passively clamped resonant DC link converter described in the previous section. For the quasi resonant counterpart, the ability to reach zero voltage is guaranteed despite the low clamping factor, since the transistors S_1 and S_2 actually short circuits the resonant link capacitor C, when conducting.

The passively clamped one switch quasi resonant DC link converter

The quasi resonant circuit discussed in the previous section have been further developed, to obtain a quasi resonant converter with low auxiliary device count. For the circuit previously described this is done by incorporating the resonant inductor L_2 on the very same core as the clamping transformer L_1/L_3. An obvious advantage in doing this is that only one core is needed. However, there is another advantage due to the fact that only one resonant link transistor is needed, if mutual coupling between L_2 and the clamping transformer is obtained. The passively clamped one switch quasi resonant DC link is presented in [9] and a circuit diagram for this circuit used for a three phase converter is shown in Figure 2.21.

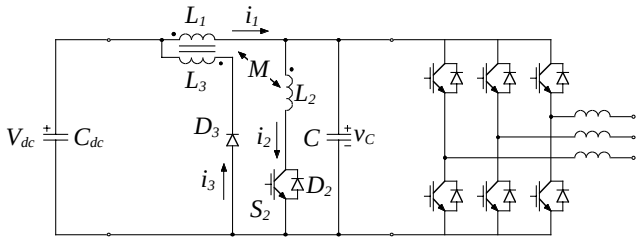


Figure 2.21 The passively clamped one switch quasi resonant DC link three phase converter.

According to [9], a suitable magnetic coupling factor between inductor L_2 and the clamping transformer L_1/L_3, is between 0.75 and 0.95.

Essentially, this circuit operates similar to the previously described but there are some differences regarding mainly the zero voltage interval. First, due to magnetic coupling between L_2 and L_1/L_3 the current i_2 is not constant during the zero voltage interval. Second, zero voltage is not

maintained by the transistor S_2 but instead by the main circuit freewheeling diodes as for the resonant DC link converter. Thus, for this circuit the duration of the zero voltage interval is determined by the change of current fed from the DC link to the three phase bridge at the switching instant.

It was previously mentioned that i_2 is not constant during the zero voltage interval. According to [9], a proper choice of the passive component values even results in a change of direction of i_2 during the zero voltage interval. For such component values, i_2 commutates from the transistor S_2 to the diode D_2 naturally (ZCS).

The parallel quasi resonant DC link converter

The parallel quasi resonant DC link circuit shown in Figure 2.22 is presented in [41]. As seen in Figure 2.22, this circuit has no actual clamping circuitry but instead a transistor, S_s, and its anti-parallel diode, D_s, are connected between the resonant circuit and the DC link. In Figure 2.22, the resonant capacitor is split among all the main circuit switches, forming individual turn-off snubbers. This is due to the fact that the resonant link is only operated for turn-on of the converter transistors, that actually will carry current. Turn-on of all these transistors occurs at the same instant. For turn-off of the transistors carrying current, i.e. current commutation to a freewheeling diode, soft turn-off are provided by the snubber capacitors. The modulation strategy adopted for this resonant circuit is presented in [40], [41].

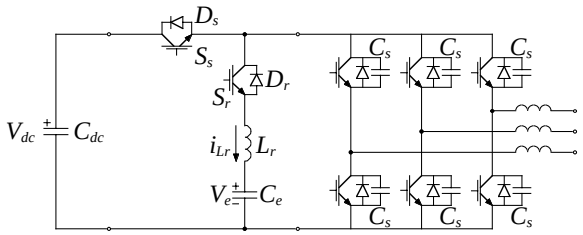


Figure 2.22 The parallel quasi resonant DC link three phase converter. Note the individual snubber capacitors forming the resonant DC link capacitor.

One way of understanding the modulation strategy given in [40], [41], is that it corresponds to saw-tooth carrier modulation, see Appendix A, with individual carriers. Whether the steep flank of each carrier is positive or negative is determined by the direction of the output current for the particular half bridge. In this way, a modulation strategy is obtained, where the transistors that will carry current are turned on simultaneously.

Each transistor is individually turned off and the output current commutates to the corresponding freewheeling diode. Soft turn-off is provided by the corresponding snubber capacitor.

The reason for turning on the transistors that is going to conduct current is probably that the other transistors should be kept off during the entire carrier period in order to avoid the current spike problems associated with snubber capacitor charging, discussed previously in this chapter. If common saw-tooth carrier modulation is used, either transistor of each half bridge has to be triggered (except during the commutation), if the direction of the corresponding output current is not considered.

At turn-on, the equivalent resonant capacitor is given by [41]

$$C_r = 3C_s \tag{2.8}$$

Actually, for the simulation in Chapter 5, the resonant circuit shown in Figure 2.23 is used instead, in order to give a fair comparison among the circuits investigated. This is due to the fact that the other circuits investigated uses triangular carrier modulation PWM, which therefore should be used also for the battery charger using this quasi resonant DC link. This means that a resonant cycle is started when a change of switch state is commanded, independent of switching state pattern and output current.

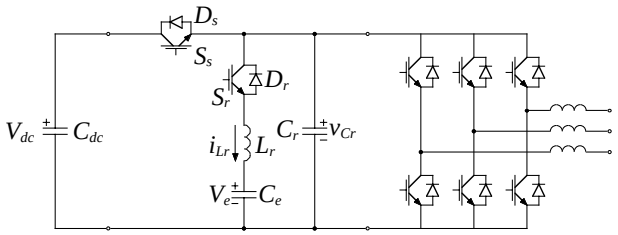


Figure 2.23 The parallel quasi resonant DC link converter when the individual snubber capacitors have been replaced with an equivalent resonant link capacitor.

According to [41], the capacitor C_e should be controlled to keep a voltage close to

$$V_e = 0.6V_{dc} \tag{2.9}$$

To ensure that the resonant link voltage returns to V_{dc} after a resonant cycle, V_e must be higher than half the DC link voltage V_{dc}, which is shown in the next chapter.

The resonant cycle starts with turn-on of the resonant transistor S_r. Since the resonant current, i_{Lr}, equals zero prior to turn-on of S_r, this operation takes place at ZCS conditions.

As soon as the resonant current reaches a pre-calculated value referred to as the trip current level, I_{r1}, the transistor S_s is turned-off (ZVS), causing discharge of the resonant link equivalent capacitor. The trip current is selected in such a way that the capacitor is completely discharged. Thus, zero voltage is reached. When zero voltage is obtained, the resonant current i_{Lr} commutates to the converter freewheeling diodes, which in effect means that the resonant link voltage is clamped to zero by the freewheeling diodes.

Also, when zero resonant link voltage is established the main circuit transistors are simultaneously turned on. This is done to provide a path for the resonant current i_{Lr}, since eventually its direction will change.

The resonant current continues to decrease until the second trip current level I_{r2} is reached. At this level the new switch state is set, resulting in the fact that the path for the resonant current through the transistors is broken. Instead, the resonant current begins to charge the equivalent resonant link capacitor, resulting in resonant link voltage ramp up.

The ramp up interval continues until the resonant link voltage reaches the level of the DC link voltage V_{dc}, where D_s becomes forward biased and the excess resonant energy is transferred back to the DC link capacitor. When D_s is conducting, S_s is turned on at both ZCS and ZVS conditions.

As previously mentioned, the circuit discussed above is similar to the one presented in [11], [31]. However in the latter case, the capacitance of the energy storage capacitor C_e is much lower. In fact, it can not be considered as a energy storage capacitor, since the voltage across it returns to zero after each resonant cycle. As a result, the resonant current i_{Lr} must be considerably higher in order to store the energy needed to complete the resonant cycle. This circuit is not considered hereafter.

The actively clamped quasi resonant DC link converter

The last quasi resonant converter to be discussed, is referred to as an actively clamped quasi resonant DC link converter. A three phase converter using this quasi resonant DC link is presented in [55], and also shown in Figure 2.24.

For quasi resonant operation, two transistor-diode couples, S_r/D_r and S_c/D_c, and a clamp capacitor C_c are added to the original resonant DC link circuit. The clamp capacitor is controlled to keep a constant clamp voltage. According to [55], an appropriate clamp factor is 1.2, which means that the voltage across C_c should equal $1.2 \cdot V_{dc}$. Note that the resonant link capacitor C_r is connected between the resonant switches and the negative supply rail.

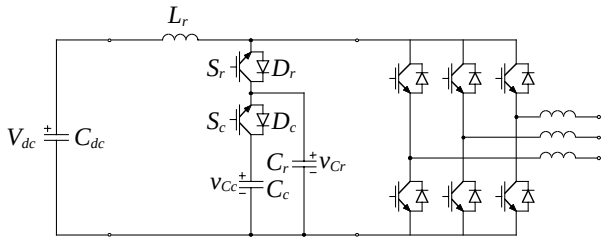


Figure 2.24 The actively clamped quasi resonant DC link three phase converter.

The resonant cycle is started with simultaneous turn-on of S_r and S_c, resulting in a sudden increase of the voltage across the converter half bridges, since the clamping capacitor is connected to the converter bridge via these transistors. Also, since the clamping capacitor voltage is 20% higher than the DC link voltage, a linearly increasing resonant current starts to flow through the inductor L_r.

When the resonant part of the inductor current reaches the pre-calculated trip current level I_{r1}, the transistor S_c is turned off (ZVS), forcing a discharge of the resonant capacitor C_r. Thus, the resonant link voltage ramps down. For this to work, the capacitance of C_r must be considerably lower than the capacitance of C_c. If the trip current is high enough, it is ensured that the resonant capacitor becomes fully discharged and thus zero voltage across the converter bridge is obtained.

As the link voltage reaches zero, the current through L_r commutates from C_r to the freewheeling diodes, clamping the resonant link voltage to zero. At this point, the converter switch state is set according to the modulator command. Eventually, the resonant current changes direction and reaches the level according to the new switch state. When this occurs, the link voltage is no longer clamped by the freewheeling diodes. Consequently, the resonant current commutates to D_r, charging the resonant capacitor C_r. As a result, the resonant link voltage ramps up.

When the resonant link voltage approaches the clamp voltage level, D_c becomes forward biased. Since the capacitance of C_c is much larger than

the one of C_r, the resonant link voltage becomes clamped to a level determined by the voltage across C_c.

At the clamping interval, the excess energy remaining in L_r after the ramp up interval, is fed to the clamping capacitor C_c. This implies that the clamping voltage will increase slightly after each resonant cycle. On the other hand, at the start of each resonant cycle C_c is discharged to some extent.

To compensate for these variations of the clamping voltage, control is needed. To decrease the clamp voltage, the trip current level is slightly increased resulting in a somewhat larger discharge of C_c. According to [55], the clamp voltage is increased by short circuiting the three phase bridge for a short while at the end of the zero voltage interval. In this way, more excess energy is held by L_r at the start of the clamping interval. The three phase bridge is short circuited by turning on both transistors of each half bridge simultaneously.

3

Analysis and design of quasi resonant DC link converters

In this chapter, the resonant circuits introduced in the previous subsection on quasi resonant DC link converters, are thoroughly examined. Design expressions based on analytical solutions to the differential equations corresponding to the different modes of the resonant cycle, are derived. Each of the quasi resonant DC links are treated separately, even though there are some similarities.

Methods to select passive component values to meet specific design criteria are also given. In Chapter 5, where the different topologies are compared, these methods are then used to give an, in some aspects, similar behaviour of the different quasi resonant DC link circuits. The design criteria common to all these topologies are, the maximum duration of the zero voltage interval and the maximum resonant link voltage derivative, i.e. the maximum output voltage derivative.

An appropriate duration of the zero voltage interval is determined by the semiconductor devices used. It must be long enough to ensure safe commutation, without an excessive short circuit current appearing through the semiconductors of the converter.

The maximum output voltage derivative is limited for mainly two reasons. First, a high voltage derivative with respect to time can result in EMC problems causing malfunction of other electronic equipment [51]. Second, the insulation of motor or output choke windings are subject to increased ageing, if exposed for continuously high voltage derivatives [9], [46], [47].

One shortcoming of the design criteria used, is that none of them takes the maximum obtainable switching frequency into consideration. Of course, this is also an important design parameter since resonant converters are often designed to operate at high switching frequencies, where the switching losses otherwise would be too dominating.

3.1 The passively clamped two switch quasi resonant circuit

As mentioned in Chapter 2, the passively clamped two switch quasi resonant DC link, previously shown in Figure 2.20, is well investigated in the literature [7], [8], [17]. Nevertheless, there are still issues to be investigated. For example, selection of passive component values to obtain certain operational criteria, which is covered in this section. First, the differential equations and their solutions are derived. To some extent this is already done in [7], but there are differences compared with the derivations given here. In [8] design and implementation of this quasi resonant DC link for an inverter application, is investigated. In [17] modulation issues for this inverter, using individual snubber capacitors as in [41], are discussed. Nevertheless, the explicit design expressions found here, are not found in any of the papers [7], [8], [17].

The simplified circuit, used in the analysis is shown in Figure 3.1, where the converter is represented by an ideal current source and an equivalent freewheeling diode representing the converter freewheeling diodes. The total resonant current through the converter freewheeling diodes is denoted i_{FD}.

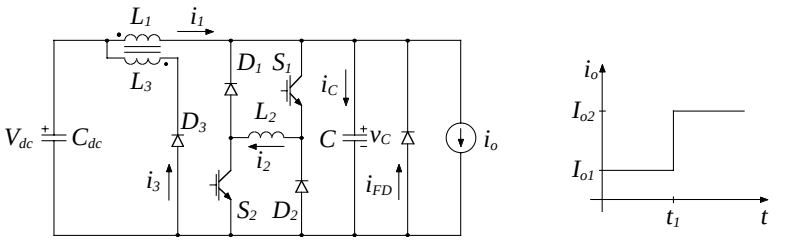


Figure 3.1 The simplified passively clamped two switch quasi resonant DC link converter, where the converter is represented as an ideal current source. To the right, the resonant link output current change is shown.

Both in Figure 3.1 and in the mathematical derivations, L_1 and L_3 denotes the clamping transformer self inductance of the primary and secondary, respectively. In this section, the clamping transformer is considered as ideal, i.e. it is considered having perfect magnetic coupling and as being loss-less.

In Figure 3.2, normalised waveforms of the main quantities of the resonant circuit are shown. The resonant link voltage v_C is normalised with respect to the DC link voltage V_{dc} and the currents are normalised to the maximum resonant link output current i_o increase.

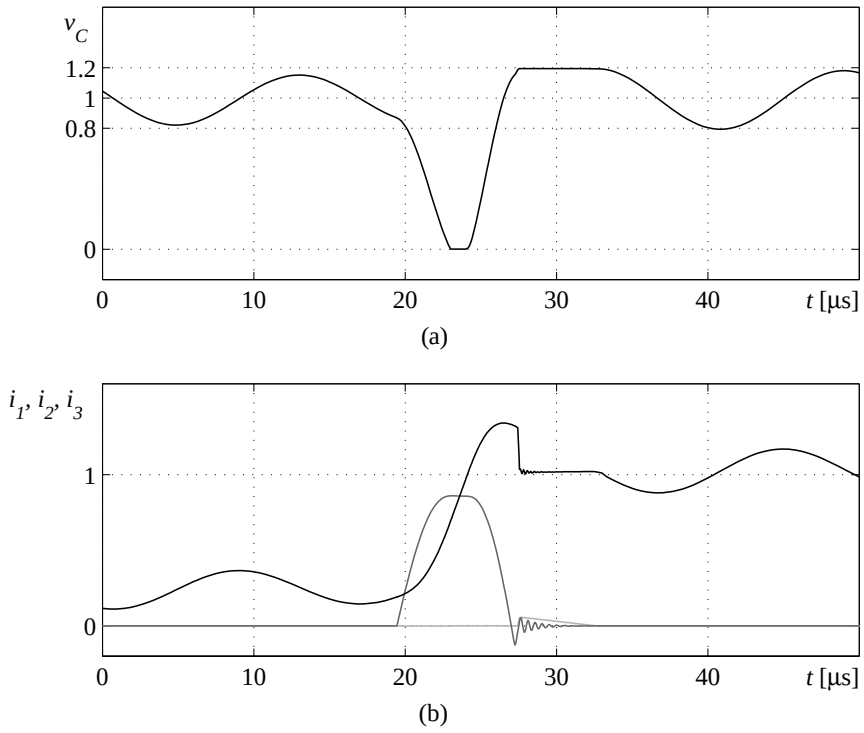


Figure 3.2 Normalised resonant link voltage (a) and inductor currents (b). In (b), the current i_1 is black, i_2 is dark grey and i_3 is light grey. The reason for the amplitude of i_3 being low in this case is that only a small amount of excess energy is stored in L_1 at the end of the resonant link voltage ramp up interval.

Resonant link voltage ramp down interval

This interval, referred to as mode 1, starts with turn-on of the switches S_1 and S_2, following a modulator command requesting a change of the converter switch state. The system of differential equations is thus written

$$\begin{cases} L_1 \dfrac{di_1}{dt} + v_C = V_{dc} \\ L_2 \dfrac{di_2}{dt} - v_C = 0 \\ i_C = C \dfrac{dv_C}{dt} \\ i_1 - i_2 - i_C - I_{o1} = 0 \end{cases} \tag{3.1}$$

The system is rearranged to form a second order ordinary differential equation through the steps shown below.

$$\frac{di_1}{dt} - \frac{di_2}{dt} - C\frac{d^2v_C}{dt^2} = 0 \tag{3.2}$$

$$V_{dc} - L_1\left(\frac{1}{L_2}v_C + C\frac{d^2v_C}{dt^2}\right) - v_C = 0 \tag{3.3}$$

$$\frac{d^2v_C}{dt^2} + \frac{1}{\frac{L_1L_2C}{L_1+L_2}}v_C = \frac{1}{L_1C}V_{dc} \tag{3.4}$$

The solution to the second order differential equation is

$$v_C(t) = A\cos\omega_1(t-t_0) + B\sin\omega_1(t-t_0) + \frac{L_2}{L_1+L_2}V_{dc} \tag{3.5}$$

where

$$\omega_1 = \frac{1}{\sqrt{\frac{L_1L_2C}{L_1+L_2}}} \tag{3.6}$$

By the use of (3.1), it follows that the capacitor current is written

$$i_C(t) = -\omega_1 CA\sin\omega_1(t-t_0) + \omega_1 CB\cos\omega_1(t-t_0) \tag{3.7}$$

During the off resonance interval, i.e. when the circuit is not in the resonant cycle, the resonant link voltage is anyway oscillating. This is due to poor damping in the L_1-C circuit, which means that a resonant cycle can start from a resonant link voltage level not equal to V_{dc}. For a clamping factor K=1.2, v_C is oscillating between 0.8 and 1.2 times V_{dc}, see Figure 3.2, which makes any of the values in between equally possible as starting point. However, by assuming that the resonant cycle starts at rest, the initial conditions for the resonant link capacitor voltage and current are written

$$\begin{cases} v_C(t_0) = A + \dfrac{L_2}{L_1+L_2}V_{dc} = V_{dc} \\ i_C(t_0) = \omega_1 CB = 0 \end{cases} \tag{3.8}$$

This means that the resonant link capacitor voltage and current are written as

$$\begin{cases} v_C(t) = \dfrac{V_{dc}}{L_1 + L_2}\left(L_2 + L_1 \cos \omega_1 (t - t_0)\right) \\ i_C(t) = -\dfrac{V_{dc}}{\omega_1 L_2} \sin \omega_1 (t - t_0) \end{cases} \tag{3.9}$$

The inductor currents are found by integration, see Appendix C, of the differential equations in (3.1), i.e.

$$\begin{aligned} i_1(t) &= i_1(t_0) + \frac{1}{L_1}\int_{t_0}^{t} \left(V_{dc} - v_C(\tau)\right) d\tau = \\ &= I_{o1} + \frac{V_{dc}}{\omega_1 \left(L_1 + L_2\right)} \cdot \left(\omega_1 (t - t_0) - \sin \omega_1 (t - t_0)\right) \end{aligned} \tag{3.10}$$

$$\begin{aligned} i_2(t) &= i_2(t_0) + \frac{1}{L_2}\int_{t_0}^{t} v_C(\tau) d\tau = \\ &= \frac{V_{dc}}{\omega_1 \left(L_1 + L_2\right)} \cdot \left(\omega_1 (t - t_0) + \frac{L_1}{L_2} \sin \omega_1 (t - t_0)\right) \end{aligned} \tag{3.11}$$

The resonant link voltage ramp down interval is finished when the resonant link capacitor voltage v_C equals zero. The corresponding time instant is referred to as t_1, hence

$$v_C(t_1) = 0 \tag{3.12}$$

Substitution into (3.9) and rearranging gives

$$\cos \omega_1 (t_1 - t_0) = -\frac{L_2}{L_1} \tag{3.13}$$

The corresponding sine term is found with aid of the trigonometric identity, see Appendix C. It should be clear that the sine term is positive, since this corresponds to the shortest time, i.e. smallest argument of the sine term. Thus

$$\sin \omega_1 (t_1 - t_0) = \sqrt{1 - \left(\frac{L_2}{L_1}\right)^2} \tag{3.14}$$

According to this, the resonant inductor currents at the end of mode 1, are written

$$\begin{cases} i_1(t_1) = I_{o1} + \dfrac{V_{dc}}{\omega_1(L_1+L_2)} \cdot \left(\arccos\left(-\dfrac{L_2}{L_1}\right) - \sqrt{1-\left(\dfrac{L_2}{L_1}\right)^2} \right) \\ i_2(t_1) = \dfrac{V_{dc}}{\omega_1(L_1+L_2)} \cdot \left(\arccos\left(-\dfrac{L_2}{L_1}\right) + \dfrac{L_1}{L_2}\sqrt{1-\left(\dfrac{L_2}{L_1}\right)^2} \right) \end{cases} \quad (3.15)$$

It is important to calculate the final values of the voltage ramp down interval since they serve as initial conditions for the next mode of operation, the zero voltage interval.

Zero voltage interval

As soon as the quasi resonant DC link enters the zero voltage interval, mode 2, the new converter switch state according to the modulator command is set, causing i_o to change level, see Figure 3.1. The current equation for mode 2 is written

$$i_1 - i_2 + i_{FD} - I_{o2} = 0 \quad (3.16)$$

Since the freewheeling diodes of the converter has a low forward voltage drop (ideally zero), it is assumed that

$$v_C(t) = 0 \quad (3.17)$$

which is a reasonable assumption as long as the equivalent freewheeling diode current, i_{FD}, is positive. Anyway, also for the case when i_{FD} equals zero this is in principle true, which is due to the fact that the capacitor current will remain low since L_1 is large. This implies only a small capacitor voltage increase, at least for a short duration of the zero voltage interval. This also means that the following differential equations are valid for the entire interval.

$$\begin{cases} L_1 \dfrac{di_1}{dt} = V_{dc} \\ L_2 \dfrac{di_2}{dt} = 0 \end{cases} \quad (3.18)$$

The solution to the upper of these differential equations are found directly by integration. The lower differential equation states that the current i_2 is constant throughout the entire zero voltage interval, see Figure 3.2.

$$i_1(t) = i_1(t_1) + \frac{1}{L_1}\int_{t_1}^{t} V_{dc}\,d\tau = i_1(t_1) + \frac{V_{dc}}{L_1}(t - t_1) \tag{3.19}$$

At the end of the zero voltage interval, $t=t_2$, the current through L_1 is given by

$$i_1(t_2) = I_{o1} + \\ + \frac{V_{dc}}{\omega_1(L_1 + L_2)} \cdot \left(\arccos\left(-\frac{L_2}{L_1}\right) - \sqrt{1 - \left(\frac{L_2}{L_1}\right)^2} \right) + \frac{V_{dc}}{L_1}(t_2 - t_1) \tag{3.20}$$

This ends the discussion about the zero voltage interval, for this circuit.

Resonant link voltage ramp up interval

The resonant link voltage ramp up interval, mode 3, is the most complicated, by means of solving differential equations. This is due to the fact that none of the constants of the solution to the differential equations are equal to zero, as *B* is for mode 1.

Nevertheless, mode 3 is the most important since here it is determined whether the capacitor voltage ramps up in a controlled manner or not, i.e. without a voltage dip in the intermediate sections of the interval. Also, the maximum resonant link voltage derivative, which is an important design parameter, appears in this mode.

Mode 3 starts when S_1 and S_2 are turned off by application of proper gate signals. Since S_1 and S_2 are turned off, the resonant inductor current i_2 is forced to commutate to the diodes D_1 and D_2. The voltage v_C ramps up with a high derivative, since both i_1 and i_2 contributes to the capacitor current i_C, which is not the case when the resonant part of the freewheeling diode current i_{FD} becomes zero in the zero voltage interval.

The system of differential equations is similar to the one of mode 1, except that the current i_2 has changed direction, thus

$$\begin{cases} L_1 \dfrac{di_1}{dt} + v_C = V_{dc} \\ L_2 \dfrac{di_2}{dt} + v_C = 0 \\ i_C = C \dfrac{dv_C}{dt} \\ i_1 + i_2 - i_C - I_{o2} = 0 \end{cases} \tag{3.21}$$

Also in mode 3, substitution gives a second order differential equation

$$\frac{d^2 v_C}{dt^2} + \frac{1}{\dfrac{L_1 L_2 C}{L_1 + L_2}} v_C = \frac{1}{L_1 C} V_{dc} \tag{3.22}$$

Note that the differential equation is the same as the one found for mode 1. Therefore, the solution is written

$$v_C(t) = A\cos\omega_1(t - t_2) + B\sin\omega_1(t - t_2) + \frac{L_2}{L_1 + L_2} V_{dc} \tag{3.23}$$

which gives the corresponding capacitor current according to (3.21), i.e.

$$i_C(t) = -\omega_1 CA\sin\omega_1(t - t_2) + \omega_1 CB\cos\omega_1(t - t_2) \tag{3.24}$$

The constants A and B are found by identifying the initial capacitor voltage and current, for the mode. The initial capacitor voltage is written

$$v_C(t_2) = A + \frac{L_2}{L_1 + L_2} V_{dc} = 0 \tag{3.25}$$

and the initial capacitor current

$$\begin{aligned} & i_C(t_2^+) = \omega_1 CB = i_1(t_2) + i_2(t_2) - I_{o2} = \\ & = \frac{V_{dc}}{\omega_1(L_1 + L_2)} \cdot \left(2\arccos\left(-\frac{L_2}{L_1} \right) + \left(\frac{L_1}{L_2} - 1 \right) \cdot \sqrt{1 - \left(\frac{L_2}{L_1} \right)^2} \right) + \\ & + \frac{V_{dc}}{L_1}(t_2 - t_1) - (I_{o2} - I_{o1}) \end{aligned} \tag{3.26}$$

This gives an expression for the constant *B* valid for the resonant link voltage ramp up interval, which is used later on when the design criteria are developed. The resonant inductor currents are found by integration

$$\begin{aligned} i_1(t) &= i_1(t_2) + \frac{1}{L_1}\int_{t_2}^{t}\left(V_{dc} - v_C(\tau)\right)d\tau = \\ &= i_1(t_2) + \frac{V_{dc}}{\omega_1\left(L_1 + L_2\right)}\omega_1(t - t_2) - \\ &- \frac{1}{\omega_1 L_1}\left(A\sin\omega_1(t - t_2) + B\left(1 - \cos\omega_1(t - t_2)\right)\right) \end{aligned} \tag{3.27}$$

$$\begin{aligned} i_2(t) &= i_2(t_2) - \frac{1}{L_2}\int_{t_2}^{t} v_C(\tau)d\tau = \\ &= i_2(t_2) - \frac{V_{dc}}{\omega_1\left(L_1 + L_2\right)}\omega_1(t - t_2) - \\ &- \frac{1}{\omega_1 L_2}\left(A\sin\omega_1(t - t_2) + B\left(1 - \cos\omega_1(t - t_2)\right)\right) \end{aligned} \tag{3.28}$$

This means that the link voltage ramp up interval is characterised. Anyway, the complicated expressions derived, can hardly be used for design purposes. For the discussion on final values valid for this mode, it is assumed that clamping occurs before the resonant inductor current i_2 has declined to zero. This is not always the case but when component values according to the later derived design expressions are used, the opposite occurs only for a large resonant link output current increase. For such a large increase, clamping will not occur anyway, with the component values selected.

For the case when clamping do appear, the final resonant capacitor voltage is

$$v_C(t) = KV_{dc} \tag{3.29}$$

where *K* is the clamping factor, which is given by

$$K = 1 + \frac{N_1}{N_3} = 1 + \sqrt{\frac{L_1}{L_3}} \tag{3.30}$$

where N_1 and N_3 denotes the clamping transformer number of winding turns for the primary and secondary, respectively.

The previous two expressions are derived, based on the fact that clamping occurs when the voltage across the transformer secondary (index *3*) equals the DC link voltage V_{dc}. The constants *A* and *B* valid for mode 3 together with resonant the DC link clamping voltage given above, are substituted into the design rule given in Appendix C.1, resulting in

$$i_C(t_3^-) = \omega_1 C \sqrt{KV_{dc}^2\left(2\frac{L_2}{L_1+L_2} - K\right) + B^2} \tag{3.31}$$

As discussed in the section on the clamping interval, this final value is enough for characterising the interval, by means of initial conditions.

Clamping interval

When clamping occurs, the excess energy stored in the clamping transformer primary (index *1*) is transferred to the secondary (index *3*). Thus, the primary current is given by

$$i_1 = -i_2 + I_{o2} \tag{3.32}$$

The previous expression together with the current constraint of (3.21), directly gives the initial value of the secondary current

$$i_3(t_3^+) = \frac{N_1}{N_3}\left(i_1(t_3^-) - i_1(t_3^+)\right) = \frac{N_1}{N_3} i_C(t_3^-) \tag{3.33}$$

The voltages across the resonant DC link components are constant during the clamping interval, resulting in

$$\begin{cases} L_2\dfrac{di_2}{dt} + v_C = L_2\dfrac{di_2}{dt} + KV_{dc} = 0 \\ L_3\dfrac{di_3}{dt} + V_{dc} = 0 \end{cases} \tag{3.34}$$

The resonant inductor current i_2 is derived by integration

$$i_2(t) = i_2(t_3) - \frac{1}{L_2}\int_{t_3}^{t} KV_{dc}\,d\tau = i_2(t_3) - \frac{KV_{dc}}{L_2}(t - t_3) \tag{3.35}$$

The clamping current i_3 is also found by integration

$$i_3(t) = i_3(t_3^+) - \frac{1}{L_3}\int_{t_3}^{t} V_{dc}\,d\tau = i_3(t_3^+) - \frac{V_{dc}}{L_3}(t - t_3) \tag{3.36}$$

The clamping interval is finished when i_3 has declined to zero. The corresponding time instant is denoted as t_4, i.e.

$$i_3(t_4) = 0 \tag{3.37}$$

which gives the duration of the clamping interval

$$t_{clamp} = t_4 - t_3 = \frac{L_3}{V_{dc}} i_3(t_3^+) \tag{3.38}$$

After a completed clamping interval, a new resonant cycle can be initiated immediately. However, if the clamping interval is not completed, the energy stored in the secondary of the transformer (index *3*) is transferred to the primary, resulting in a high magnitude of the resonant inductor current i_2. This is not allowed, since the current stress on the transistors S_1 and S_2 is increased in such a case.

Off resonance interval

After a completed clamping interval, the off resonance interval commences. The name is somewhat misleading for this circuit, since even though i_2 equals zero, L_1 and C still forms a resonant circuit. This implies that the oscillation of the resonant link voltage will continue. The amplitude of the oscillating voltage is determined by the clamping factor, as described in this section. The system is in this case described by

$$\begin{cases} L_1 \dfrac{di_1}{dt} + v_C = V_{dc} \\ i_C = C\dfrac{dv_C}{dt} \\ i_1 - i_C - I_{o2} = 0 \end{cases} \tag{3.39}$$

By rearranging the system of differential equations, a second order differential equation is obtained

$$\frac{d^2 v_C}{dt^2} + \frac{1}{L_1 C} v_C = \frac{1}{L_1 C} V_{dc} \tag{3.40}$$

The solution is written

$$v_C(t) = A\cos\omega_2(t-t_4) + B\sin\omega_2(t-t_4) + V_{dc} \tag{3.41}$$

where A and B are constants and

$$\omega_2 = \frac{1}{\sqrt{L_1 C}} \tag{3.42}$$

The capacitor current is found by substituting (3.41) into (3.39), which gives

$$i_C(t) = -\omega_2 CA\sin\omega_2(t-t_4) + \omega_2 CB\cos\omega_2(t-t_4) \tag{3.43}$$

Since clamping in most cases occurs prior to the off resonance interval, the initial conditions are

$$\begin{cases} v_C(t_4) = A + V_{dc} = KV_{dc} \\ i_C(t_4) = \omega_2 CB = 0 \end{cases} \tag{3.44}$$

The initial capacitor current is equal to zero according to (3.39), since at the end of the clamping interval i_1 equals I_{o2}. The capacitor voltage and current for the off resonance interval are thus written

$$\begin{cases} v_C(t) = V_{dc}\left(1 + (K-1)\cos\omega_2(t-t_4)\right) \\ i_C(t) = -\sqrt{\dfrac{C}{L_1}}(K-1)V_{dc}\sin\omega_2(t-t_4) \end{cases} \tag{3.45}$$

Here it is clearly seen that for the off resonance interval, the resonant DC link voltage will oscillate between

$$(2-K)V_{dc} \le v_C(t) \le KV_{dc} \tag{3.46}$$

if damping is neglected. The clamping factor used throughout the entire text equals 1.2, which means that the resonant link capacitor voltage will vary between 0.8 and 1.2 times V_{dc}, see Figure 3.2. Note that for the next resonant cycle, any initial voltage in between is equally probable, which was also stated in the derivation made for the resonant link voltage ramp down interval.

Design expressions

The design criteria are based on three different constraints, since there are three component values to be selected, L_1, L_2 and C. The first two

design constraints are the duration of the zero voltage interval and the maximum resonant DC link voltage derivative obtained. These two are used for all the quasi-resonant circuits investigated. The third constraint used for this circuit, aims for limitation of the current i_2.

To start with, L_1 is calculated in such a way that the resonant cycle is completed in an acceptable manner. For the maximum increase of the output current, i_o, the capacitor current should not be negative when i_1 has increased to I_{o2} at the end of the resonant link voltage ramp up interval. If the resonant capacitor current is negative at this point, the capacitor voltage is decreasing instead of increasing. The limiting case is thus given by

$$\begin{cases} i_1(t_3) = I_{o2} \\ i_C(t_3) = 0 \end{cases} \tag{3.47}$$

Together with the expression for the currents of equation system (3.21), it is also found that

$$i_2(t_3) = 0 \tag{3.48}$$

for this case. Since the capacitor current should equal zero at the end of the ramp up interval for the limiting case, (3.24) gives

$$A \sin \omega_1(t_3 - t_2) = B \cos \omega_1(t_3 - t_2) \tag{3.49}$$

Rearranging this equation gives

$$B = A \tan \omega_1(t_3 - t_2) \tag{3.50}$$

Substitution into (3.28) and using the final value for i_2 according to (3.48) gives

$$i_2(t_2) - \frac{V_{dc}}{\omega_1(L_1 + L_2)} \cdot \left(\omega_1(t_3 - t_2) - \tan \omega_1(t_3 - t_2)\right) = 0 \tag{3.51}$$

Assume

$$\begin{cases} \sin \omega_1(t_3 - t_2) = \sqrt{1 - \alpha^2} \\ \cos \omega_1(t_3 - t_2) = -\alpha \end{cases} \tag{3.52}$$

which gives

$$\tan \omega_1 (t_3 - t_2) = -\frac{\sqrt{1-\alpha^2}}{\alpha} \tag{3.53}$$

Substitution into expression (3.51) above gives

$$i_2(t_2) = \frac{V_{dc}}{\omega_1 (L_1 + L_2)} \cdot \left(\arccos(-\alpha) + \frac{\sqrt{1-\alpha^2}}{\alpha} \right) \tag{3.54}$$

The corresponding current found in the investigation of the zero voltage interval, i.e. equation (3.15), states that

$$\begin{aligned} & i_2(t_2) = i_2(t_1) = \\ & = \frac{V_{dc}}{\omega_1 (L_1 + L_2)} \cdot \left(\arccos\left(-\frac{L_2}{L_1} \right) + \frac{L_1}{L_2} \sqrt{1 - \left(\frac{L_2}{L_1} \right)^2} \right) \end{aligned} \tag{3.55}$$

By comparing the previous two expressions for i_2, it is found that

$$\alpha = \frac{L_2}{L_1} \tag{3.56}$$

which means that in this case, the resonant link voltage ramp down and ramp up intervals have the same duration. To get a more compact description, (3.56) is substituted into all the expressions hereafter. As previously mentioned, it is not the output current level but the change of the output current level that determines the worst case. Also, the current i_1 increases most for a zero voltage interval of maximum duration. Inserting this into equation (3.27) and using the limiting value for i_1 in (3.47) above, gives

$$\begin{aligned} & i_1(t_3) = I_{o1} + \frac{V_{dc}}{\omega_1 L_1 (1+\alpha)} \cdot \left(2 \arccos(-\alpha) - 2\sqrt{1-\alpha^2} \right) + \\ & + \frac{V_{dc}}{L_1} (t_2 - t_1)_{max} = I_{o2} \end{aligned} \tag{3.57}$$

Rearranging the previous expression gives the upper limit for the inductance L_1 according to

$$L_1 = \frac{V_{dc}}{\omega_1 \left(I_{o2} - I_{o1}\right)_{max}} \cdot \frac{2}{1+\alpha} \cdot \left(\arccos(-\alpha) - \sqrt{1-\alpha^2}\right) + \\ + \frac{V_{dc}(t_2 - t_1)_{max}}{\left(I_{o2} - I_{o1}\right)_{max}} \tag{3.58}$$

This value of L_1 is calculated upon the maximum duration of the zero voltage interval. The next constraint to be fulfilled is to limit the maximum resonant link voltage derivative, i.e. the maximum output voltage derivative. By assuming the maximum negative output current change for a resonant cycle to equal the maximum positive, by means of magnitude, i.e.

$$\left(I_{o2} - I_{o1}\right)_{min} = -\left(I_{o2} - I_{o1}\right)_{max} \tag{3.59}$$

the maximum value of the constant B for mode 3 is found by inserting (3.58) into equation (3.26) and rearranging. Hence

$$B_{max} = 4V_{dc} \frac{\alpha}{(1+\alpha)^2} \cdot \arccos(-\alpha) - V_{dc} \frac{3-\alpha}{(1+\alpha)^2} \cdot \sqrt{1-\alpha^2} + \\ + V_{dc} \frac{\alpha}{1+\alpha} \left(\omega_1 (t_2 - t_1)_{max} + \omega_1 (t_2 - t_1)\right) \tag{3.60}$$

If the duration of the zero voltage interval is held constant, i.e.

$$\omega_1 (t_2 - t_1) = \omega_1 (t_2 - t_1)_{max} \tag{3.61}$$

it is found that

$$B_{max} = 4V_{dc} \frac{\alpha}{(1+\alpha)^2} \cdot \arccos(-\alpha) - V_{dc} \frac{3-\alpha}{(1+\alpha)^2} \cdot \sqrt{1-\alpha^2} + \\ + 2V_{dc} \frac{\alpha}{1+\alpha} \omega_1 (t_2 - t_1)_{max} \tag{3.62}$$

The maximum resonant link voltage derivative is calculated from expression (3.23). With the value for the constant A from (3.25), substituted into this derivative it is found that

$$\left.\frac{dv_C}{dt}\right|_{max} = \omega_1 \sqrt{\left(\frac{\alpha}{1+\alpha} V_{dc}\right)^2 + B_{max}^2} \tag{3.63}$$

The last design constraint is used to limit the current i_2 in order to keep the current rating of the resonant link semiconductors, S_1/S_2 and D_1/D_2, at

an acceptable level. According to expression (3.15), the peak value of i_2 is given by

$$i_2(t_1) = \frac{V_{dc}}{\omega_1 L_1 (1+\alpha)} \cdot \left(\arccos(-\alpha) + \frac{\sqrt{1-\alpha^2}}{\alpha} \right) \qquad (3.64)$$

The design expressions (3.58), (3.63) and (3.64) together determines L_1, ω_1 and α, which in effect means that L_1, L_2 and C are determined. However, to find the proper values, the calculation of these three expressions have to be iterated.

3.2 The passively clamped one switch quasi resonant circuit

The passively clamped one switch quasi resonant circuit described here is a further development of the two switch counterpart described in the previous section. A simplified converter using the passively clamped one switch quasi resonant DC link is shown in Figure 3.3. Since the circuit has only one additional switch, the resonant inductor current i_2 can not be forced to commutate from S_2 to D_2 to initiate the resonant DC link voltage ramp up interval. Instead, mutual magnetic coupling between L_1/L_3 and L_2 is employed in order to obtain inherent reversal of i_2. To obtain mutual magnetic coupling, L_1/L_3 and L_2 are wound upon the same iron core. In Figure 3.3 the mutual coupling is shown by the M located between L_1/L_3 and L_2.

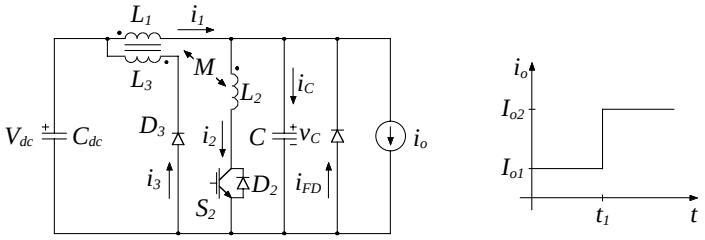


Figure 3.3 The passively clamped one switch quasi resonant DC link with a simplified converter equivalent consisting of a current source and an equivalent freewheeling diode. To the right, a resonant link output current change is shown.

Due to the magnetic coupling between the primary (index *1*) and the secondary (index *2*) windings, the voltages across the corresponding windings are written

$$\begin{cases} v_1 = \dfrac{d}{dt}\left(L_1 i_1 + M i_2\right) = L_1 \dfrac{di_1}{dt} + M \dfrac{di_2}{dt} \\ v_2 = \dfrac{d}{dt}\left(M i_1 + L_2 i_2\right) = M \dfrac{di_1}{dt} + L_2 \dfrac{di_2}{dt} \end{cases} \tag{3.65}$$

The mutual inductance is given by

$$M = k\sqrt{L_1 L_2} \tag{3.66}$$

where k is the magnetic coupling factor, for the primary and secondary windings. Note that the tertiary winding also should be included in the expressions for the winding voltages. There are mainly two reasons for not doing this here. First, the magnetic coupling factor is assumed to be equal to one for the primary and tertiary windings, i.e. the clamp transformer is regarded as being ideal. Second, the secondary and tertiary windings do not carry current simultaneously for this circuit.

The passively clamped one switch quasi resonant circuit is presented in [9], together with the differential equations and their solutions for each mode. However, selection of appropriate passive component values is not discussed in [9].

In this section, the differential equations and their solutions are given for each mode of operation. Furthermore, design expressions developed to meet certain constraints are presented. In Figure 3.4 normalised waveforms of the quantities of main interest for this circuit are shown. The resonant link voltage v_C is normalised with respect to the DC link voltage V_{dc}. The resonant link currents in Figure 3.4 are normalised with respect to the maximum increase of the resonant link output current i_o, which the resonant link is designed to meet.

Several interesting observations are made from Figure 3.4. The high magnitude of the resonant inductor current i_2 is clearly seen. The magnitude of this current is actually several times higher than the output current, implying that the resonant link semiconductors must have a current rating several times higher than the converter semiconductors. Also note that the resonant link voltage ramp up interval is divided into two parts, with large differences in the derivative which the voltage increases with. Also, between these two parts, the resonant link voltage is actually decreasing for a short while. The origin of this decrease is discussed in Chapter 5.

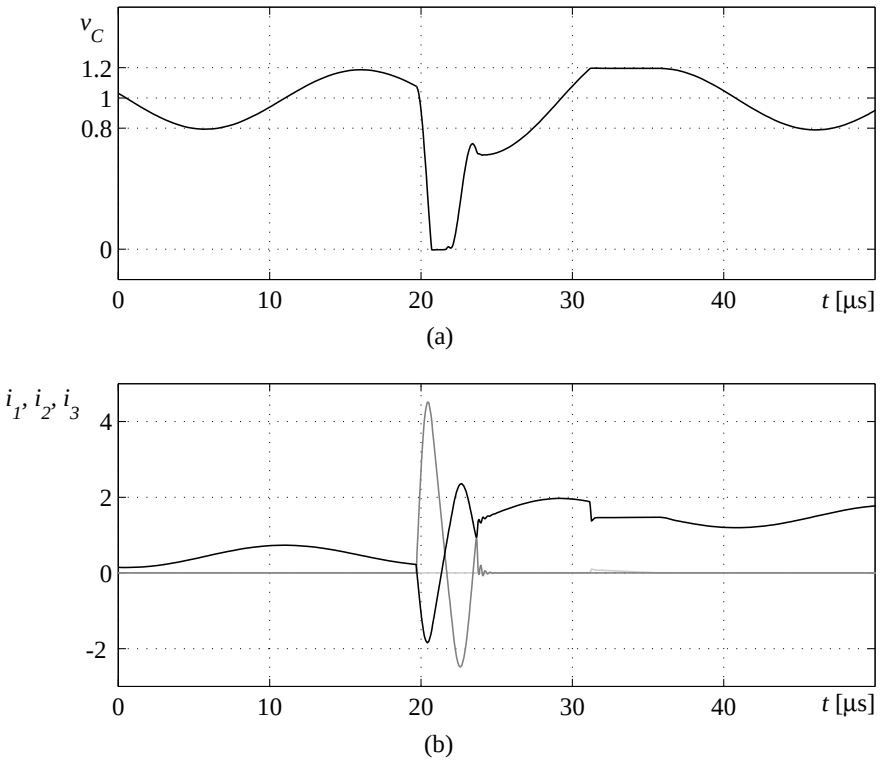


Figure 3.4 Normalised resonant link voltage (a) and inductor currents (b). In (b), the current i_1 is black, i_2 is dark grey and i_3 is light grey.

For the resonant cycle shown in Figure 3.4 it should be noted that the short duration of the clamping interval at the end of the cycle, is because only a small of amount of excess energy has to be returned to the DC link capacitor, since the resonant link output current increase is relatively high. This also results in a low clamp transformer current i_3 during the clamping interval. The duration of the clamping interval depends on the magnitude of the resonant link output current change, for the particular resonant cycle, which is discussed later on in this section.

Resonant link voltage ramp down interval

The resonant link voltage ramp down interval, is initiated with turn-on of the resonant transistor S_2, following a modulator command. The resulting system of differential equations valid for mode 1, which this interval is termed, is given below.

$$\begin{cases} L_1 \dfrac{di_1}{dt} + M \dfrac{di_2}{dt} + v_C = V_{dc} \\ M \dfrac{di_1}{dt} + L_2 \dfrac{di_2}{dt} - v_C = 0 \\ i_C = C \dfrac{dv_C}{dt} \\ i_1 - i_2 - i_C - I_{o1} = 0 \end{cases} \tag{3.67}$$

By rearranging the system of differential equations above, two differential equations are obtained

$$\frac{di_1}{dt} + \frac{L_2 + M}{L_1 L_2 - M^2} v_C = \frac{L_2}{L_1 L_2 - M^2} V_{dc} \tag{3.68}$$

$$\left(L_1 + M\right)\frac{di_1}{dt} - MC\frac{d^2 v_C}{dt^2} + v_C = V_{dc} \tag{3.69}$$

which are substituted to form a second order differential equation

$$\frac{d^2 v_C}{dt^2} + \frac{1}{\dfrac{\left(L_1 L_2 - M^2\right)C}{L_1 + L_2 + 2M}} v_C = \frac{L_2 + M}{\left(L_1 L_2 - M^2\right)C} V_{dc} \tag{3.70}$$

The solution to the second order differential equation is

$$v_C(t) = A\cos\omega_1(t - t_0) + B\sin\omega_1(t - t_0) + \frac{L_2 + M}{L_1 + L_2 + 2M} V_{dc} \tag{3.71}$$

where the characteristic angular frequency, ω_1, is given by

$$\omega_1 = \frac{1}{\sqrt{\dfrac{L_1 L_2 - M^2}{L_1 + L_2 + 2M} C}} \tag{3.72}$$

According to (3.67), the resonant link capacitor current is expressed as

$$i_C(t) = -\omega_1 CA\sin\omega_1(t - t_0) + \omega_1 CB\cos\omega_1(t - t_0) \tag{3.73}$$

The constants A and B are given by the initial conditions of the resonant link capacitor voltage and current, respectively, according to

$$\begin{cases} v_C(t_0) = A + \dfrac{L_2 + M}{L_1 + L_2 + 2M} V_{dc} = V_{dc} \\ i_C(t_0) = \omega_1 CB = 0 \end{cases} \tag{3.74}$$

Note that it is assumed that the resonant link starts at rest. Later on it is shown that this is not necessarily true, similar to the case for the two switch counterpart discussed in the previous section. With the initial conditions stated above, the capacitor voltage and current are given by

$$\begin{cases} v_C(t) = \dfrac{V_{dc}}{L_1 + L_2 + 2M}\left(\left(L_2 + M\right) + \left(L_1 + M\right)\cos\omega_1(t - t_0)\right) \\ i_C(t) = -\dfrac{V_{dc}\left(L_1 + M\right)}{\omega_1\left(L_1 L_2 - M^2\right)}\sin\omega_1(t - t_0) \end{cases} \tag{3.75}$$

Integrating (3.68) gives

$$\begin{aligned} i_1(t) &= i_1(t_0) + \frac{1}{L_1 L_2 - M^2}\int_{t_0}^{t}\left(L_2 V_{dc} - \left(L_2 + M\right)v_C(\tau)\right)d\tau = I_{o1} + \\ &+ \frac{V_{dc}}{\omega_1\left(L_1 + L_2 + 2M\right)}\cdot\left(\omega_1(t - t_0) - \frac{\left(L_1 + M\right)\left(L_2 + M\right)}{L_1 L_2 - M^2}\sin\omega_1(t - t_0)\right) \end{aligned} \tag{3.76}$$

The algebraic current equation of (3.67) gives

$$\begin{aligned} i_2(t) &= i_1(t) - i_C(t) - I_{o1} = \\ &= \frac{V_{dc}}{\omega_1\left(L_1 + L_2 + 2M\right)}\cdot\left(\omega_1(t - t_0) + \frac{\left(L_1 + M\right)^2}{L_1 L_2 - M^2}\sin\omega_1(t - t_0)\right) \end{aligned} \tag{3.77}$$

The resonant link voltage ramp down interval is finished when

$$v_C(t_1) = 0 \tag{3.78}$$

which together with (3.75) gives

$$\cos\omega_1(t_1 - t_0) = -\frac{L_2 + M}{L_1 + M} \tag{3.79}$$

According to the trigonometric identity it is found that

$$\sin \omega_1 (t_1 - t_0) = \sqrt{1 - \left(\frac{L_2 + M}{L_1 + M} \right)^2} \tag{3.80}$$

It should be clear that the last quantity is positive, since it should correspond to the shortest time. Substituting into (3.75) gives

$$i_C(t_1) = -\frac{V_{dc}}{\omega_1} \cdot \frac{L_1 + M}{L_1 L_2 - M^2} \cdot \sqrt{1 - \left(\frac{L_2 + M}{L_1 + M} \right)^2} \tag{3.81}$$

Similarly, substituting into (3.76) and (3.77) gives the inductor currents at the end of the resonant link voltage ramp down interval.

$$\begin{aligned} i_1(t_1) = I_{o1} + \frac{V_{dc}}{\omega_1 (L_1 + L_2 + 2M)} \cdot \arccos\left(-\frac{L_2 + M}{L_1 + M} \right) - \\ - \frac{V_{dc}}{\omega_1 (L_1 + L_2 + 2M)} \cdot \frac{(L_2 + M)^2}{L_1 L_2 - M^2} \cdot \sqrt{\left(\frac{L_1 + M}{L_2 + M} \right)^2 - 1} \end{aligned} \tag{3.82}$$

$$\begin{aligned} i_2(t_1) = \frac{V_{dc}}{\omega_1 (L_1 + L_2 + 2M)} \cdot \arccos\left(-\frac{L_2 + M}{L_1 + M} \right) + \\ + \frac{V_{dc}}{\omega_1 (L_1 + L_2 + 2M)} \cdot \frac{(L_1 + M)^2}{L_1 L_2 - M^2} \cdot \sqrt{1 - \left(\frac{L_2 + M}{L_1 + M} \right)^2} \end{aligned} \tag{3.83}$$

The final values of the resonant link voltage ramp down interval, by means of inductor currents, are used as initial conditions for the zero voltage interval.

Zero voltage interval

As soon as the zero voltage interval (mode 2) is entered, the new switch state according to the modulator command should be set. However, this do not affect the resonant link since the capacitor voltage is clamped to zero by the freewheeling diodes of the converter. In effect, this means that the resonant current flows through the freewheeling diodes which is the reason why an equivalent freewheeling diode must be included in the simplified converter equivalent. This implies that for the zero voltage interval, the system of differential equations is given by

$$\begin{cases} V_{dc} - v_1 = V_{dc} - L_1 \dfrac{di_1}{dt} - M \dfrac{di_2}{dt} = 0 \\ v_2 = M \dfrac{di_1}{dt} + L_2 \dfrac{di_2}{dt} = 0 \\ i_1 - i_2 + i_{FD} - I_{o2} = 0 \end{cases} \tag{3.84}$$

The first two equations are rearranged to

$$\begin{cases} \dfrac{di_1}{dt} = \dfrac{L_2}{L_1 L_2 - M^2} V_{dc} \\ \dfrac{di_2}{dt} = -\dfrac{M}{L_1 L_2 - M^2} V_{dc} \end{cases} \tag{3.85}$$

Hence, the inductor currents of mode 2 are found by integration

$$\begin{aligned} i_1(t) &= i_1(t_1) + \frac{L_2}{L_1 L_2 - M^2} \cdot \int_{t_1}^{t} V_{dc} d\tau = \\ &= i_1(t_1) + V_{dc} \frac{L_2}{L_1 L_2 - M^2} (t - t_1) \end{aligned} \tag{3.86}$$

$$\begin{aligned} i_2(t) &= i_2(t_1) - \frac{M}{L_1 L_2 - M^2} \cdot \int_{t_1}^{t} V_{dc} d\tau = \\ &= i_2(t_1) - V_{dc} \frac{M}{L_1 L_2 - M^2} (t - t_1) \end{aligned} \tag{3.87}$$

The current equation of the equation system (3.84), together with the resonant inductor currents (3.86) and (3.87) with the final values (3.82) and (3.83) of the resonant link voltage ramp down interval substituted, gives the current through the equivalent freewheeling diode

$$\begin{aligned} i_{FD}(t) &= I_{o2} - i_1(t) + i_2(t) = \\ &= \frac{V_{dc}}{\omega_1} \cdot \frac{\sqrt{(L_1 + L_2 + 2M) \cdot (L_1 - L_2)}}{L_1 L_2 - M^2} + \\ &+ (I_{o2} - I_{o1}) - V_{dc} \frac{L_2 + M}{L_1 L_2 - M^2} (t - t_1) \end{aligned} \tag{3.88}$$

In opposite to the two switch counterpart, the zero voltage interval cannot be prolonged by keeping the resonant link transistor on. Instead, the zero voltage interval is finished when i_{FD} has decreased to zero, which means that the resonant current commutates from the converter freewheeling diodes to the resonant link capacitor C. The time instant when this occurs is denoted t_2. Hence

$$i_{FD}(t_2) = 0 \tag{3.89}$$

Actually, this is equivalent to

$$i_1(t_2) - i_2(t_2) = I_{o2} \tag{3.90}$$

Any of the last two expressions gives the duration of the zero voltage interval

$$(t_2 - t_1) = \frac{1}{\omega_1} \cdot \sqrt{\left(\frac{L_1 + M}{L_2 + M}\right)^2 - 1} + \frac{(I_{o2} - I_{o1})}{V_{dc}} \cdot \frac{L_1 L_2 - M^2}{L_2 + M} \tag{3.91}$$

If (3.82) and (3.91) are substituted into (3.86), the resonant inductor current i_1 at the end of the zero voltage interval is found to be

$$\begin{aligned} i_1(t_2) = I_{o1} &+ \frac{V_{dc}}{\omega_1(L_1 + L_2 + 2M)} \cdot \arccos\left(-\frac{L_2 + M}{L_1 + M}\right) + \\ &+ \frac{V_{dc}}{\omega_1(L_1 + L_2 + 2M)} \cdot \sqrt{\left(\frac{L_1 + M}{L_2 + M}\right)^2 - 1} + \frac{L_2}{L_2 + M}(I_{o2} - I_{o1}) \end{aligned} \tag{3.92}$$

Similar, if (3.83) and (3.91) are substituted into (3.87), the resonant inductor current i_2 at the time instant t_2, is expressed by

$$\begin{aligned} i_2(t_2) = &\frac{V_{dc}}{\omega_1(L_1 + L_2 + 2M)} \cdot \arccos\left(-\frac{L_2 + M}{L_1 + M}\right) + \\ &+ \frac{V_{dc}}{\omega_1(L_1 + L_2 + 2M)} \cdot \sqrt{\left(\frac{L_1 + M}{L_2 + M}\right)^2 - 1} - \frac{M}{L_2 + M}(I_{o2} - I_{o1}) \end{aligned} \tag{3.93}$$

There is one important remark to be made here, which is that the resonant inductor current i_2 should change sign, i.e. become negative, during the zero voltage interval, see Figure 3.4. This is important since it implies that the transistor S_2 turns off naturally, i.e. i_2 commutates from S_2 to D_2 by it self without removal of the gating signal of S_2. According to [9] this

is fulfilled if the magnetic coupling factor k, between L_1 and L_2 is in the interval [0.75<k<0.95].

The resonant link voltage ramp up interval

For this circuit, the resonant link voltage ramp up interval actually consists of two modes. The first part, mode 3, is the part with non-zero resonant current i_2. The second part, mode 4, is when the current i_2 equals zero. As a matter of fact, there is an quite large difference between these two modes due to the change in characteristic angular frequency when traversing from mode 3 to 4, see Figure 3.4. For mode 3, the system of differential equations is written

$$\begin{cases} L_1 \dfrac{di_1}{dt} + M \dfrac{di_2}{dt} + v_C = V_{dc} \\ M \dfrac{di_1}{dt} + L_2 \dfrac{di_2}{dt} - v_C = 0 \\ i_C = C \dfrac{dv_C}{dt} \\ i_1 - i_2 - i_C - I_{o2} = 0 \end{cases} \tag{3.94}$$

Note the similarities with the equation system of mode 1, (3.67). The equation system is rearranged into a second order differential equation through the same steps as for mode 1, which gives

$$\frac{d^2 v_C}{dt^2} + \frac{1}{\dfrac{\left(L_1 L_2 - M^2\right)C}{L_1 + L_2 + 2M}} v_C = \frac{L_2 + M}{\left(L_1 L_2 - M^2\right)C} V_{dc} \tag{3.95}$$

The general solution to the differential equation above is written

$$v_C(t) = A\cos\omega_1(t - t_2) + B\sin\omega_1(t - t_2) + \frac{L_2 + M}{L_1 + L_2 + 2M} V_{dc} \tag{3.96}$$

Which also implies that the capacitor current is given by

$$i_C(t) = -\omega_1 CA\sin\omega_1(t - t_2) + \omega_1 CB\cos\omega_1(t - t_2) \tag{3.97}$$

The constants A and B are determined from the initial conditions

$$\begin{cases} v_C(t_2) = A + \dfrac{L_2 + M}{L_1 + L_2 + 2M} V_{dc} = 0 \\ i_C(t_2) = \omega_1 CB = 0 \end{cases} \tag{3.98}$$

The resonant link capacitor voltage and current are thus expressed as

$$\begin{cases} v_C(t) = \dfrac{L_2 + M}{L_1 + L_2 + 2M} V_{dc}\left(1 - \cos\omega_1(t - t_2)\right) \\ i_C(t) = \dfrac{V_{dc}\left(L_2 + M\right)}{\omega_1\left(L_1 L_2 - M^2\right)} \sin\omega_1(t - t_2) \end{cases} \tag{3.99}$$

Similar to the resonant link voltage ramp down interval, the equation system (3.94) is rearranged to get expressions where the resonant inductor currents are calculated from integration. This gives

$$\begin{aligned} i_1(t) &= i_1(t_2) + \frac{1}{L_1 L_2 - M^2} \int_{t_2}^{t} \left(L_2 V_{dc} - \left(L_2 + M\right) v_C(\tau)\right) d\tau = \\ &= i_1(t_2) + \frac{V_{dc}}{\omega_1\left(L_1 + L_2 + 2M\right)} \omega_1(t - t_2) + \\ &+ \frac{V_{dc}}{\omega_1\left(L_1 + L_2 + 2M\right)} \cdot \frac{\left(L_2 + M\right)^2}{L_1 L_2 - M^2} \sin\omega_1(t - t_2) \end{aligned} \tag{3.100}$$

$$\begin{aligned} i_2(t) &= i_1(t) - i_C(t) - I_{o2} = \\ &= i_2(t_2) + \frac{V_{dc}}{\omega_1\left(L_1 + L_2 + 2M\right)} \omega_1(t - t_2) - \\ &- \frac{V_{dc}}{\omega_1\left(L_1 + L_2 + 2M\right)} \cdot \frac{\left(L_1 + M\right)\left(L_2 + M\right)}{L_1 L_2 - M^2} \sin\omega_1(t - t_2) \end{aligned} \tag{3.101}$$

The first part of the resonant link voltage ramp up interval, i.e. mode 3, ends as previously mentioned when

$$i_2(t_3) = 0 \tag{3.102}$$

Consequently, the duration of mode 3 must be calculated from the non-linear equation

$$\omega_1(t_3-t_2)-\frac{(L_1+M)(L_2+M)}{L_1L_2-M^2}\sin\omega_1(t_3-t_2)=$$
$$=\arccos\left(-\frac{L_2+M}{L_1+M}\right)+\sqrt{\left(\frac{L_1+M}{L_2+M}\right)^2-1}- \qquad (3.103)$$
$$-\frac{\omega_1(L_1+L_2+2M)}{V_{dc}}\cdot\frac{M}{L_2+M}(I_{o2}-I_{o1})$$

Since the expression above is non-linear, the final values of mode 3 for the other state variables can not be expressed with the time dependent terms substituted.

The system of differential equations for mode 4 is similar to the one of the previous mode (3.94), with i_2 and its time derivative set equal to zero.

$$\begin{cases} L_1\dfrac{di_1}{dt}+v_C=V_{dc} \\ i_C=C\dfrac{dv_C}{dt} \\ i_1-i_C-I_{o2}=0 \end{cases} \qquad (3.104)$$

This is rearranged to form a second order differential equation

$$\frac{d^2v_C}{dt^2}+\frac{1}{L_1C}v_C=\frac{1}{L_1C}V_{dc} \qquad (3.105)$$

The general solution to the differential equation is given by

$$v_C(t)=A\cos\omega_2(t-t_3)+B\sin\omega_2(t-t_3)+V_{dc} \qquad (3.106)$$

where the characteristic angular frequency ω_2 equals

$$\omega_2=\frac{1}{\sqrt{L_1C}} \qquad (3.107)$$

The resonant link capacitor current, i_C, is calculated according to (3.104), giving

$$i_C(t)=-\omega_2CA\sin\omega_2(t-t_3)+\omega_2CB\cos\omega_2(t-t_3) \qquad (3.108)$$

The algebraic current equation of (3.94) together with (3.102) and the current equation of (3.104), gives

$$i_C(t_3^-) = i_1(t_3^-) - I_{o2} = i_1(t_3^+) - I_{o2} = i_C(t_3^+) \tag{3.109}$$

stating that the initial capacitor current of mode 4 is equal to the ending capacitor current of mode 3. This means that the constants of the general solution are found from the initial conditions according to

$$\begin{cases} v_C(t_3) = A + V_{dc} = V_{dc}\dfrac{L_2 + M}{L_1 + L_2 + 2M}\left(1 - \cos\omega_1(t_3 - t_2)\right) \\ i_C(t_3) = \omega_2 CB = \dfrac{V_{dc}}{\omega_1} \cdot \dfrac{L_2 + M}{L_1 L_2 - M^2}\sin\omega_1(t_3 - t_2) \end{cases} \tag{3.110}$$

Rearranging gives the constants

$$\begin{cases} A = -\dfrac{V_{dc}}{L_1 + L_2 + 2M}\left(\left(L_1 + M\right) + \left(L_2 + M\right)\cos\omega_1(t_3 - t_2)\right) \\ B = V_{dc}\dfrac{\omega_1}{\omega_2} \cdot \dfrac{L_2 + M}{L_1 + L_2 + 2M}\sin\omega_1(t_3 - t_2) \end{cases} \tag{3.111}$$

The resonant link voltage ramp up interval is finished when the clamping voltage level is reached, i.e. when

$$v_C(t) = KV_{dc} \tag{3.112}$$

The method used to calculate final values, see Appendix C, gives

$$i_C(t_4^-) = \omega_2 C\sqrt{A^2 + B^2 - V_{dc}^2(K-1)^2} \tag{3.113}$$

According to the current equation of (3.104) it is also found that

$$i_1(t_4^-) = i_C(t_4^-) + I_{o2} \tag{3.114}$$

The clamping interval

Since clamping occurs when the diode D_3 becomes forward biased, the clamping factor K is determined by the turns ratio between the primary and tertiary windings

$$K = 1 + \frac{N_1}{N_3} = 1 + \sqrt{\frac{L_1}{L_3}} \tag{3.115}$$

where N_1 and N_3 are the number of winding turns for the primary and tertiary winding, respectively. The excess magnetic energy stored in the primary, is transferred to the tertiary winding, giving

$$i_1 = i_1(t_4^+) = I_{o2} \tag{3.116}$$

$$i_3(t_4^+) = \frac{N_1}{N_3}\left(i_1(t_4^-) - i_1(t_4^+)\right) = \frac{N_1}{N_3} i_C(t_4^-) \tag{3.117}$$

Neglecting the forward voltage drop across D_3 gives

$$L_3 \frac{di_3}{dt} + V_{dc} = 0 \tag{3.118}$$

This first order differential equation is solved by direct integration

$$i_3(t) = i_3(t_4^+) - \frac{1}{L_3}\int_{t_4}^{t} V_{dc} d\tau = i_3(t_4^+) - \frac{V_{dc}}{L_3}(t - t_4) \tag{3.119}$$

The clamping interval ends when i_3 has declined to zero, i.e.

$$i_3(t_5) = 0 \tag{3.120}$$

Hence, the duration of the clamping interval equals

$$t_{clamp} = t_5 - t_4 = \frac{L_3}{V_{dc}} i_3(t_4^+) \tag{3.121}$$

Off Resonance

When the excess resonant energy has been transferred back to the DC link capacitor, i.e. when the clamping interval is finished, the quasi resonant DC link circuit is ready for a new cycle. However, the circuit is not at rest since an oscillation is started in the resonant circuit formed by L_1 and C, see Figure 3.4. The system of differential equations for the off resonance interval is given by

$$\begin{cases} L_1 \dfrac{di_1}{dt} + v_C = V_{dc} \\ i_C = C \dfrac{dv_C}{dt} \\ i_1 - i_C - I_{o2} = 0 \end{cases} \tag{3.122}$$

This is actually the same as the one valid for mode 4 of the resonant link voltage ramp up interval. Consequently, substitution to obtain a second order differential equation gives the same result

$$\frac{d^2 v_C}{dt^2} + \frac{1}{L_1 C} v_C = \frac{1}{L_1 C} V_{dc} \tag{3.123}$$

The general solution to the differential equation above gives the resonant link capacitor voltage

$$v_C(t) = A \cos \omega_2 (t - t_5) + B \sin \omega_2 (t - t_5) + V_{dc} \tag{3.124}$$

The corresponding current is found by derivation

$$i_C(t) = -\omega_2 CA \sin \omega_2 (t - t_5) + \omega_2 CB \cos \omega_2 (t - t_5) \tag{3.125}$$

The initial conditions for the resonant capacitor voltage and current are used to determine the constants *A* and *B* of the general solution

$$\begin{cases} v_C(t_5) = A + V_{dc} = KV_{dc} \\ i_C(t_5) = \omega_2 CB = 0 \end{cases} \tag{3.126}$$

resulting in the following expressions for the capacitor voltage and current

$$\begin{cases} v_C(t) = V_{dc}\left(1 + (K-1)\cos \omega_2 (t - t_5)\right) \\ i_C(t) = -\sqrt{\frac{C}{L_1}}(K-1) V_{dc} \sin \omega_2 (t - t_5) \end{cases} \tag{3.127}$$

As for the two switch counterpart, the resonant link voltage will oscillate between

$$(2 - K)V_{dc} \le v_C(t) \le KV_{dc} \tag{3.128}$$

also for the passively clamped one switch quasi resonant circuit, during the off resonance interval. If the clamping factor *K* equals 1.2, the resonant link voltage is thus oscillating between 0.8 and 1.2 times the DC link voltage, see Figure 3.4.

Design expressions

Also for this circuit design expressions are derived based upon the duration of the zero voltage interval and maximum resonant link voltage derivative. Nevertheless, the most important design objective is to ensure that the resonant circuit is able to complete its cycle at the worst case loading. Therefore, this is treated first.

For mode 3 of the resonant link voltage ramp up interval, it was previously stated that it ends when

$$i_2(t_3) = 0 \tag{3.129}$$

For proper operation it is also desirable that

$$i_C(t_3) \geq 0 \tag{3.130}$$

If the last expression is not fulfilled, the resonant link voltage has already started do decrease. The resonant link capacitor current is given by (3.99) which for this case gives

$$\sin \omega_1 (t_3 - t_2) \geq 0 \tag{3.131}$$

which is equivalent to

$$\omega_1 (t_3 - t_2) \leq \pi \tag{3.132}$$

Also note that (3.129) and (3.130) together are equivalent to

$$i_1(t_3) \geq I_{o2} \tag{3.133}$$

To simplify the expressions, the substitution

$$\alpha = \frac{L_2}{L_1} \tag{3.134}$$

is used which gives the mutual inductance

$$M = k\sqrt{L_1 L_2} = L_1 k \sqrt{\alpha} \tag{3.135}$$

The limiting case substituted into (3.100) gives

$$i_1(t_3) = I_{o2} = I_{o1} + \frac{V_{dc}}{\omega_1 L_1\left(1+\alpha+2k\sqrt{\alpha}\right)} \cdot \arccos\left(-\frac{\alpha+k\sqrt{\alpha}}{1+k\sqrt{\alpha}}\right) + \\ + \frac{V_{dc}}{\omega_1 L_1\left(1+\alpha+2k\sqrt{\alpha}\right)} \cdot \sqrt{\left(\frac{1+k\sqrt{\alpha}}{\alpha+k\sqrt{\alpha}}\right)^2 - 1} + \\ + \frac{\alpha}{\alpha+k\sqrt{\alpha}}\left(I_{o2} - I_{o1}\right) + \frac{V_{dc}}{\omega_1 L_1\left(1+\alpha+2k\sqrt{\alpha}\right)} \cdot \pi \tag{3.136}$$

Rearranging the terms, gives the maximum value of L_1 according to

$$L_1 = \frac{V_{dc}}{\omega_1\left(I_{o2} - I_{o1}\right)_{max}} \cdot \frac{\alpha+k\sqrt{\alpha}}{k\sqrt{\alpha}\left(1+\alpha+2k\sqrt{\alpha}\right)} \cdot \\ \cdot \left(\pi + \arccos\left(-\frac{\alpha+k\sqrt{\alpha}}{1+k\sqrt{\alpha}}\right) + \sqrt{\left(\frac{1+k\sqrt{\alpha}}{\alpha+k\sqrt{\alpha}}\right)^2 - 1}\right) \tag{3.137}$$

For this circuit, the duration of the zero voltage interval depends on the magnitude of the output current, i_o, change during the resonant cycle. For the maximum change, the duration of the zero voltage interval also becomes the longest. According to (3.91) the maximum duration is

$$(t_2 - t_1)_{max} = \frac{1}{\omega_1}\sqrt{\left(\frac{1+k\sqrt{\alpha}}{\alpha+k\sqrt{\alpha}}\right)^2 - 1} + \\ + \frac{\left(I_{o2} - I_{o1}\right)_{max}}{V_{dc}} \cdot \frac{\alpha - k^2\alpha}{\alpha+k\sqrt{\alpha}} \cdot L_1 \tag{3.138}$$

The maximum resonant link voltage derivative for mode 1, is calculated from (3.75), which gives

$$\left.\frac{dv_C}{dt}\right|_{max} = \omega_1 V_{dc}\,\frac{L_1+M}{L_1+L_2+2M} = \omega_1 V_{dc}\,\frac{1+k\sqrt{\alpha}}{1+\alpha+2k\sqrt{\alpha}} \tag{3.139}$$

For mode 3, the maximum resonant link voltage derivative is calculated from (3.99), which gives

$$\left.\frac{dv_C}{dt}\right|_{max} = \omega_1 V_{dc}\,\frac{L_2+M}{L_1+L_2+2M} = \omega_1 V_{dc}\,\frac{\alpha+k\sqrt{\alpha}}{1+\alpha+2k\sqrt{\alpha}} \tag{3.140}$$

Since

$$\alpha < 1 \tag{3.141}$$

according to [9], the maximum voltage derivative is obtained during the resonant link voltage ramp down interval.

In order to select appropriate passive component values for the passively clamped one switch quasi resonant DC link, the equations (3.137), (3.138) and (3.139) are used. This gives appropriate values for L_1, α and ω_1, which are used to calculate the corresponding values of L_1, L_2 and C.

Note that the magnetic coupling factor, k, between the inductors L_1 and L_2 is not used as a design variable. This could be used to minimise the peak value of resonant current i_2. Anyway, it is not that easy to design the resonant inductors L_1 and L_2 on the same magnetic core to obtain a certain coupling factor. It is likely that the three winding transformer is designed to have an as high magnetic coupling factor as possible and then introduce an additional inductor in series with the secondary winding to tune the inductance of L_2.

3.3 The parallel quasi resonant circuit

The parallel quasi resonant DC link converter is described in [41]. In [40], modulation issues are discussed. In both these papers the resonant link capacitor is split among the half bridges of the converter to form individual snubber capacitors. This is needed due to the modulation strategy used, which was discussed in Chapter 2. Here, this modulation strategy is not used. Instead, triangular carrier PWM, see Appendix A, is used to be able to give an as fair as possible comparison.

In Figure 3.5, a simplified version of the converter using this quasi resonant DC link is shown. Here, the individual snubber capacitors are replaced by one single equivalent resonant link capacitor C_r. This is also done in [41], but only to simplify the analysis.

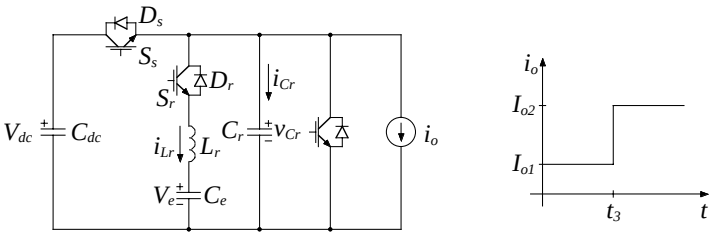


Figure 3.5 The parallel quasi resonant DC link circuit with a simplified converter equivalent, containing one transistor and one diode together with a current source. To the right, an output current change is shown.

The converter equivalent in Figure 3.5 consists of a current source and also a transistor and a freewheeling diode. For the previous two quasi resonant DC links, the converter equivalent have not been equipped with a transistor across the resonant link. The reason why it is needed here, is the fact that the resonant current through the freewheeling diode must be allowed to change sign, i.e. commutate from the converter freewheeling diodes to the transistors. This implies that not only the freewheeling diodes are clamping the link voltage to zero, but also the transistors. When the current through the equivalent transistor equals the resonant link output current i_o, according to the new switch state, this should be set, i.e. one transistor of each converter half bridge is turned off.

By keeping the resonant link short circuited for a longer time, more energy is transferred from the energy storage capacitor C_e to the resonant inductor L_r, causing a decrease of V_e.

To increase the voltage V_e, the resonant link transistors S_s and S_r are kept on simultaneously for a slightly longer time than needed to ensure that the resonant link voltage ramp down interval is completed, at the beginning of the resonant cycle. Thus, more energy is transferred from the DC link capacitor to the energy storage capacitor.

To control the energy storage capacitor voltage V_e, the margins introduced for the trip currents are varied. This is discussed when the expressions for the trip current levels are derived, later on in this section.

However, for the derivation of the differential equations and their solutions, the voltage across the energy storage capacitor C_e is considered as being constant. In order to ensure completion of the resonant cycle, this voltage should be controlled to equal

$$V_e = 0.6V_{dc} \tag{3.142}$$

according to [41]. The reason for this value being suitable is shown later on.

In Figure 3.6 a resonant cycle is shown. The quantities shown in Figure 3.6 are normalised, where the voltage base value is the DC link voltage V_{dc} and the current base value is selected as the maximum resonant link output current increase during one cycle, which the resonant link is designed to meet.

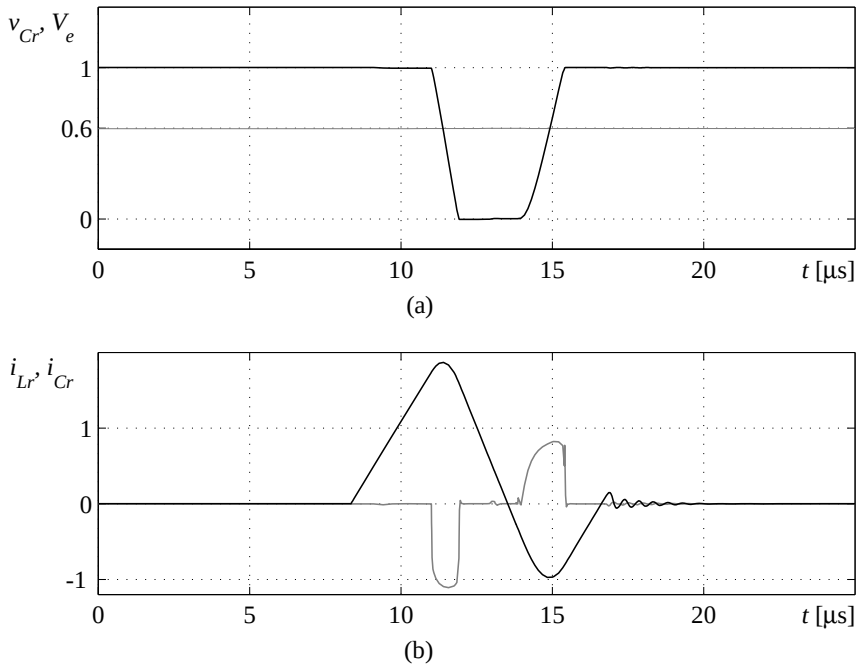


Figure 3.6 Normalised waveforms, (a) resonant link voltage v_C (black) and energy storage capacitor voltage V_e (grey), and (b) resonant inductor current i_{Lr} (black) and resonant capacitor current i_{Cr} (grey).

Energy storage interval

For the parallel quasi resonant DC link, an energy storage interval referred to as mode 1, is needed in order to store resonant energy in the resonant inductor L_r to ensure that the resonant link voltage do decrease down to zero, during the ramp down interval. The energy storage interval starts with turn-on of the resonant link transistor S_r. The resulting differential equation is written

$$V_{dc} - L_r \frac{di_{Lr}}{dt} - V_e = 0 \tag{3.143}$$

This is rearranged to express the inductor current time derivative, i.e.

$$\frac{di_{Lr}}{dt} = \frac{V_{dc} - V_e}{L_r} \tag{3.144}$$

By integrating the last expression, the resonant inductor current is written

$$i_{Lr}(t) = i_{Lr}(t_0) + \frac{V_{dc} - V_e}{L_r}(t - t_0) = \frac{V_{dc} - V_e}{L_r}(t - t_0) \qquad (3.145)$$

The energy storage interval is finished when the inductor current reaches the mode 1 trip current level, denoted I_{r1}. Hence

$$i_{Lr}(t_1) = I_{r1} \qquad (3.146)$$

Thus, the duration of the energy storage interval is equal to

$$(t_1 - t_0) = \frac{L_r I_{r1}}{V_{dc} - V_e} \qquad (3.147)$$

Resonant link voltage ramp down interval

The resonant link voltage ramp down interval (mode 2), is initiated by turning off the resonant link series transistor S_s, forcing a discharge of the resonant link capacitor C_r. The system of differential equations valid for this mode is given below.

$$\begin{cases} v_{Cr} - L_r \dfrac{di_{Lr}}{dt} - V_e = 0 \\ i_{Cr} = C_r \dfrac{dv_{Cr}}{dt} \\ i_{Lr} + i_{Cr} + I_{o1} = 0 \end{cases} \qquad (3.148)$$

The equation system is rewritten to form a second order differential equation

$$\frac{d^2 v_{Cr}}{dt^2} + \frac{1}{L_r C_r} v_{Cr} = \frac{1}{L_r C_r} V_e \qquad (3.149)$$

The general solution to the second order differential equation is written

$$v_{Cr}(t) = A\cos\omega_r(t - t_1) + B\sin\omega_r(t - t_1) + V_e \qquad (3.150)$$

where the characteristic angular frequency ω_r is given by

$$\omega_r = \frac{1}{\sqrt{L_r C_r}} \qquad (3.151)$$

According to the original system of differential equations, (3.148), the resonant link capacitor current is found from the time derivative of the voltage. This gives

$$i_{Cr}(t) = -\omega_r C_r A \sin \omega_r (t - t_1) + \omega_r C_r B \cos \omega_r (t - t_1) \quad (3.152)$$

The initial capacitor voltage and current determines the constants A and B, according to

$$\begin{cases} v_{Cr}(t_1) = A + V_e = V_{dc} \\ i_{Cr}(t_1) = \omega_r C_r B = -I_{r1} - I_{o1} \end{cases} \quad (3.153)$$

The ramp down interval is finished when the resonant link voltage reaches zero. The corresponding time instant is denoted t_2. Thus,

$$v_{Cr}(t_2) = 0 \quad (3.154)$$

A necessary condition for this to occur is

$$i_{Cr}(t_2) \leq 0 \quad (3.155)$$

According to the method for calculating final values given in Appendix C.1, the limiting case is written

$$(0 - V_e)^2 + \left(\frac{0}{\omega_r C_r} \right)^2 = (V_{dc} - V_e)^2 + \left(-\frac{I_{r1} + I_{o1}}{\omega_r C_r} \right)^2 \quad (3.156)$$

The minimum trip current level of mode 1 is thus given by

$$I_{r1} = -I_{o1} + \sqrt{\frac{C_r}{L_r} V_{dc} (2V_e - V_{dc})} \quad (3.157)$$

Introducing a small current margin

$$I_{m1} > 0 \quad (3.158)$$

which is added to the minimum trip current, giving

$$I_{r1} = I_{m1} - I_{o1} + \sqrt{\frac{C_r}{L_r} V_{dc} (2V_e - V_{dc})} \quad (3.159)$$

If the trip current value calculated above is used, the initial resonant capacitor current equals

$$i_{Cr}(t_1)_{max} = \omega_r C_r B_{max} = -I_{m1} - \sqrt{\frac{C_r}{L_r} V_{dc}\left(2V_e - V_{dc}\right)} \quad (3.160)$$

and the capacitor current at the start of the zero voltage interval is given by

$$i_{Cr}(t_2)_{max} = -\sqrt{I_{m1}^2 + 2I_{m1}\sqrt{\frac{C_r}{L_r} V_{dc}\left(2V_e - V_{dc}\right)}} \quad (3.161)$$

Note that the trip current must be positive. If a negative trip current is calculated, zero is used. The worst case initial resonant capacitor current thus equals

$$i_{Cr}(t_1)_{min} = \omega_r C_r B_{min} = -I_{o1,max} \quad (3.162)$$

The maximum discharge current, i.e. minimum capacitor current, at the end of the resonant link voltage ramp down interval thus equals

$$i_{Cr}(t_2)_{min} = -\sqrt{I_{o1,max}^2 + \frac{C_r}{L_r} V_{dc}\left(2V_e - V_{dc}\right)} \quad (3.163)$$

The inductor current at the end of the resonant link voltage ramp down interval is in any case given by

$$i_{Lr}(t_2) = -i_{Cr}(t_2) - I_{o1} \quad (3.164)$$

Note that by increasing the current margin I_{m1}, more energy than necessary is transferred to the resonant circuit. Furthermore, the energy storage capacitor voltage V_e increases somewhat, even if its capacitance is high. In Chapter 5 this is used for control purposes.

Zero voltage interval

During the zero voltage interval the resonant link voltage is clamped to zero, first by the converter freewheeling diodes and then by the converter transistors. This implies

$$v_{Cr}(t) = 0 \quad (3.165)$$

which means that the differential equation valid for this mode is given by

$$L_r \frac{di_{Lr}}{dt} + V_e = 0 \quad (3.166)$$

Through integration, the resonant inductor current is found to be

$$i_{Lr}(t) = i_{Lr}(t_2) - \frac{V_e}{L_r}(t - t_2) \tag{3.167}$$

The zero voltage interval is finished when the mode 3 trip current level is reached, i.e. when

$$i_{Lr}(t_3) = I_{r2} \tag{3.168}$$

Since the transistors of the converter are clamping the resonant link voltage immediately prior to the time instant t_3, this trip current has to be negative. For a positive resonant link output current it is thus given by

$$I_{r2} = -I_{o2} \tag{3.169}$$

However, for a negative resonant link output current the trip current is selected according to

$$I_{r2} = -I_{m2} \leq 0 \tag{3.170}$$

In both cases (3.167) gives

$$i_{Lr}(t_3) = I_{r2} = -I_{o1} - i_{Cr}(t_2) - \frac{V_e}{L_r}(t_3 - t_2) \tag{3.171}$$

The duration of the zero voltage interval is thus given by

$$(t_3 - t_2) = \frac{L_r}{V_e}\left(-I_{r2} - I_{o1} - i_{Cr}(t_2)\right) \tag{3.172}$$

Also in this case the current margin, I_{m2}, is allowed to vary, in order to control the energy storage capacitor voltage V_e. This is possible due to the fact that for a large margin, the energy storage capacitor C_e is discharged to a larger extent than for small margin. In Chapter 5, where the quasi resonant DC links are simulated, the current margins discussed here are used to control the voltage V_e. If it is to low, the current margin of mode 1, I_{m1}, is increased and if it is to high, the current margin of mode 3, I_{m2}, is increased.

Resonant link voltage ramp up interval

The system of differential equations valid for the resonant link voltage ramp up interval is given below.

$$\begin{cases} v_{Cr} - L_r \dfrac{di_{Lr}}{dt} - V_e = 0 \\ i_{Cr} = C_r \dfrac{dv_{Cr}}{dt} \\ i_{Lr} + i_{Cr} + I_{o2} = 0 \end{cases} \tag{3.173}$$

The corresponding second order differential equation becomes

$$\frac{d^2 v_{Cr}}{dt^2} + \frac{1}{L_r C_r} v_{Cr} = \frac{1}{L_r C_r} V_e \tag{3.174}$$

which has the general solution

$$v_{Cr}(t) = A\cos\omega_r(t - t_3) + B\sin\omega_r(t - t_3) + V_e \tag{3.175}$$

The corresponding resonant capacitor current is thus written

$$i_{Cr}(t) = -\omega_r C_r A\sin\omega_r(t - t_3) + \omega_r C_r B\cos\omega_r(t - t_3) \tag{3.176}$$

The initial conditions for this mode are calculated from the final values of the zero voltage interval, which also determines the constants of the general solution

$$\begin{cases} v_{Cr}(t_3) = A + V_e = 0 \\ i_{Cr}(t_3) = \omega_r C_r B = -I_{r2} - I_{o2} \end{cases} \tag{3.177}$$

The constant *B* can also be expressed as

$$B = \sqrt{\frac{L_r}{C_r}} i_{Cr}(t_3) \tag{3.178}$$

The resonant link voltage interval is completed when

$$v_{Cr}(t_4) = V_{dc} \tag{3.179}$$

The resonant capacitor current must be non-negative at this time instant, i.e.

$$i_{Cr}(t_4) \geq 0 \tag{3.180}$$

Application of the method of calculating final values, given in Appendix C.1, gives

$$i_{Cr}(t_4) = \sqrt{\frac{C_r}{L_r} V_{dc}\left(2V_e - V_{dc}\right) + i_{Cr}^2(t_3)} \tag{3.181}$$

which shows that the constraint (3.180) is fulfilled as long as V_e exceeds 0.5. Furthermore, if the trip current is selected according to (3.169) it is found that

$$i_{Cr}(t_4)_{min} = \sqrt{\frac{C_r}{L_r} V_{dc}\left(2V_e - V_{dc}\right)} \tag{3.182}$$

Resonant energy recovery interval

During the resonant energy recovery interval, mode 5, the excess energy stored in the resonant inductor L_r is transferred back to the DC link capacitor C_{dc} via the resonant link series diode D_s. Furthermore, this also implies that the resonant link voltage is clamped to the DC link voltage level. During the energy recovery interval the resonant link series transistor S_s is turned on, to be able support the current fed to the converter during the off resonance period. The differential equation valid for this mode is thus written

$$V_{dc} - L_r \frac{di_{Lr}}{dt} - V_e = 0 \tag{3.183}$$

The resonant inductor current is derived by integration, giving

$$i_{Lr}(t) = i_{Lr}(t_4) + \frac{V_{dc} - V_e}{L_r}(t - t_4) = \frac{V_{dc} - V_e}{L_r}(t - t_4) \tag{3.184}$$

The excess resonant energy is fully restored when

$$i_{Lr}(t_5) = 0 \tag{3.185}$$

which gives that the duration of the resonant energy recovery interval is expressed as

$$\begin{aligned}(t_5 - t_4) &= -\frac{L_r}{V_{dc} - V_e} i_{Lr}(t_4) = \\ &= \frac{L_r}{V_{dc} - V_e}\left(I_{o2} + \sqrt{\frac{C_r}{L_r} V_{dc}\left(2V_e - V_{dc}\right) + i_{Cr}^2(t_3)}\right)\end{aligned} \tag{3.186}$$

For this circuit, either the series transistor or diode of the resonant link, i.e. S_s or D_s, is conducting the current drawn by the converter during the off resonance interval. This also means that the resonant link voltage v_{Cr} is clamped to the DC link voltage level V_{dc}. Consequently, no oscillations are observed during the off resonance interval, i.e. in between the resonant cycles.

Design expressions

For the parallel quasi resonant DC link converter investigated here, only two parameter values are possible to use as design parameters, L_r and C_r. This means that the design constraints on the duration of the zero voltage interval and the maximum resonant link voltage derivative together determines the resonant link passive components.

The energy storage capacitor C_e is selected in such a way that its voltage variation during one resonant cycle, does not become unacceptably high.

The constraint to ensure completion of the resonant cycle is not guaranteed by proper passive component selection, as it was for the passively clamped resonant circuits. Instead, this is ensured by proper selection of the mode 1 trip current level I_{r1}.

First, the maximum duration of the zero voltage interval, encountered for the maximum resonant link output current increase, is determined according to (3.172)

$$(t_3 - t_2)_{max} = \frac{L_r}{V_e}\left(I_{o2} - I_{o1}\right)_{max} + \\ + \frac{L_r}{V_e}\sqrt{I_{m1}^2 + 2I_{m1}\sqrt{\frac{C_r}{L_r}}V_{dc}\left(2V_e - V_{dc}\right)} \tag{3.187}$$

In the expression above, the current margin I_{m2} is set to zero, since this is only used for control purposes, i.e. the resonant link is able to complete its cycle even if I_{m2} is set equal to zero.

The mode 1 current margin I_{m1} is used both for control purposes and to ensure that zero resonant link voltage is reached. Therefore, I_{m1} is included in the expression above.

The voltage derivative is analysed both for the resonant link voltage ramp down (mode 2) and ramp up (mode 4) intervals. For mode 2, the minimum value of the constant B is given by

$$B_{min} = -\sqrt{\frac{L_r}{C_r}} I_{o1,max} \tag{3.188}$$

resulting in a maximum voltage derivative for this mode according to

$$\begin{aligned} \left.\frac{dv_{Cr}}{dt}\right|_{max} &= \omega_r \sqrt{A^2 + \left(B^2\right)_{max}} = \omega_r \sqrt{A^2 + B_{min}^2} = \\ &= \omega_r \sqrt{\left(V_{dc} - V_e\right)^2 + \left(\frac{I_{o1,max}}{\omega_r C_r}\right)^2} \end{aligned} \tag{3.189}$$

For mode 4, the maximum value of the constant B in the general solution of the corresponding differential equation, is given by

$$B_{max} = \sqrt{\frac{L_r}{C_r}} \left(I_{m2} - I_{o2,min}\right) \tag{3.190}$$

The maximum voltage derivative for this mode thus equals

$$\begin{aligned} \left.\frac{dv_{Cr}}{dt}\right|_{max} &= \omega_r \sqrt{A^2 + B_{max}^2} = \\ &= \omega_r \sqrt{V_e^2 + \left(\frac{I_{m2} - I_{o2,min}}{\omega_r C_r}\right)^2} \end{aligned} \tag{3.191}$$

If it is assumed that the minimum value of the resonant link output current i_o, equals the maximum with opposite sign, i.e.

$$I_{o2,min} = -I_{o1,max} \tag{3.192}$$

it is found that the resonant link maximum voltage derivative is obtained for the resonant link voltage ramp up interval, i.e. mode 4, since

$$V_e = 0.6V_{dc} > V_{dc} - V_e = 0.4V_{dc} \tag{3.193}$$

In [41], a control expression regarding selection of the mode 1 trip current level, is presented. This expression is also derived here (3.159), by use of the method for calculating final values, given in Appendix C.1. Unfortunately, the derivation of the expression for selection of the resonant link voltage ramp down trip current level is not part of [41].

3.4 The actively clamped quasi resonant circuit

The actively clamped quasi resonant DC link converter is presented in [55]. In Figure 3.7 this resonant link is shown together with a simplified converter equivalent, consisting of an ideal current source and a transistor and a diode connected across the resonant link. The transistor and diode are needed for the analysis of the circuit, since the resonant link inductor current i_{Lr} flows through these components during the zero voltage interval. In fact, the zero voltage interval is inhibited by setting the transistor switch state according to the modulator command. Prior to this, the resonant link is shorted by keeping all the converter transistors on, which was also the case for the previously investigated parallel quasi resonant DC link converter.

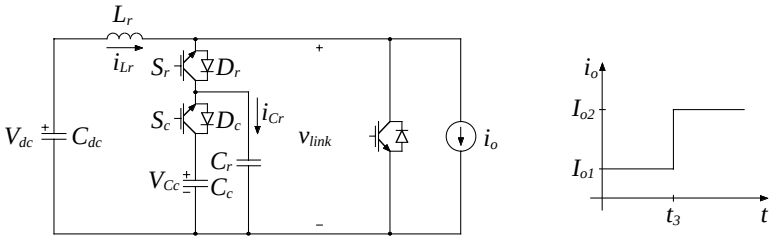


Figure 3.7 The simplified actively clamped quasi resonant DC link converter, where the converter is represented as an ideal current source and an equivalent transistor-diode combination connected across the resonant link. To the right, a resonant link output current step is shown.

Throughout the entire analysis, the clamping voltage V_{Cc} is considered being constant, i.e.

$$V_{Cc} = KV_{dc} \tag{3.194}$$

Here, K denotes the clamping factor. Note that in the simulations, see Chapter 5, the clamping voltage has to be controlled.

In Figure 3.8, normalised waveforms of the basic quantities for this circuit are shown for the case with a clamping factor equal to 1.2. The DC link voltage V_{dc} is the voltage normalisation base value and the maximum output current change designed to meet, is the current base value.

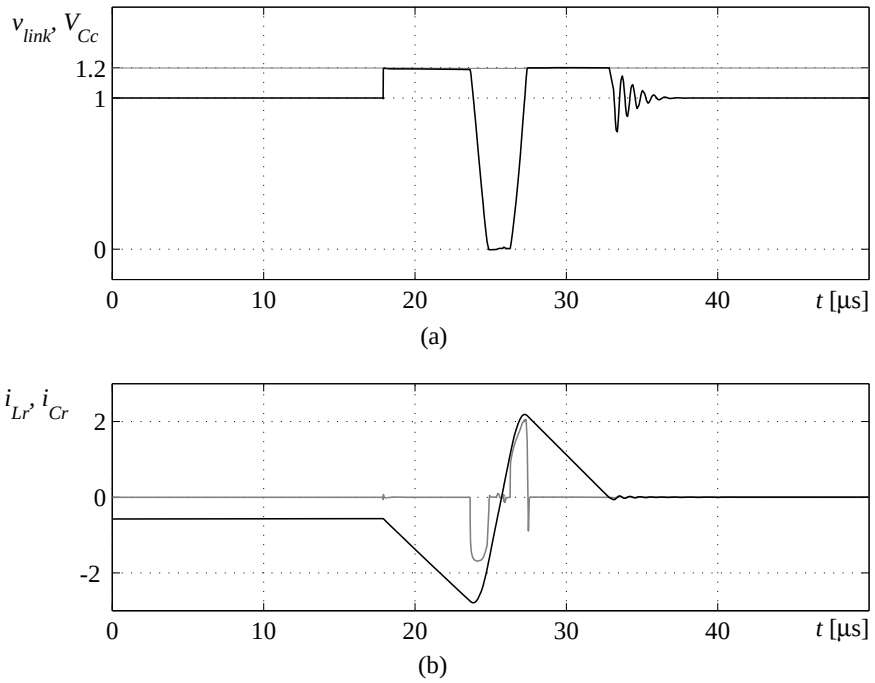


Figure 3.8 Normalised (a) resonant link voltage v_{link} (black) and clamping voltage V_{Cc} (grey), and (b) resonant inductor current i_{Lr} (black) and resonant capacitor current i_{Cr} (grey).

Note the oscillations at the end of the resonant cycle, see Figure 3.8.

In [55], almost no mathematical derivations are presented. Consequently, no design expressions are given. Here, mathematical derivations for the resonant link operation of each mode is presented together with the design expressions selected.

Energy storage interval

For the actively clamped quasi resonant DC link, a resonant transition is started by turning on both the resonant link transistors, S_r and S_c, causing the resonant link voltage v_{link} to equal the clamping voltage V_{Cc}. The differential equation valid for this mode is thus written

$$V_{dc} - L_r \frac{di_{Lr}}{dt} - V_{Cc} = 0 \tag{3.195}$$

Consequently, the resonant inductor current derivative is expressed as

$$\frac{di_{Lr}}{dt} = \frac{V_{dc} - V_{Cc}}{L_r} = -\frac{(K-1)V_{dc}}{L_r} \tag{3.196}$$

Integration gives

$$i_{Lr}(t) = i_{Lr}(t_0) - \frac{(K-1)V_{dc}}{L_r}(t - t_0) = I_{o1} - \frac{(K-1)V_{dc}}{L_r}(t - t_0) \tag{3.197}$$

The energy storage interval (mode 1) is finished when

$$i_{Sr}(t_1) = I_{r1} \tag{3.198}$$

where I_{r1} is the mode 1 trip current level. The resonant inductor current at this time instant is

$$i_{Lr}(t_1) = I_{o1} - i_{Sr}(t_1) = I_{o1} - I_{r1} \tag{3.199}$$

Substitution into (3.197) gives

$$i_{Lr}(t_1) = I_{o1} - \frac{(K-1)V_{dc}}{L_r}(t_1 - t_0) = I_{o1} - i_{Sr}(t_1) = I_{o1} - I_{r1} \tag{3.200}$$

Hence, the duration of the energy storage interval is given by

$$(t_1 - t_0) = \frac{L_r I_{r1}}{(K-1)V_{dc}} \tag{3.201}$$

When the trip current level is reached, the resonant link transistor S_c is turned off, causing discharge of the resonant link capacitor C_r. Here it is important that C_c is much larger than C_r, by means of capacitance. Otherwise, the clamping voltage can not be regarded as constant.

Resonant link voltage ramp down interval

As soon as S_c is turned off the resonant link voltage will start to decrease, since a resonant inductor current is built up during the energy storage interval. However, for the resonant link voltage to reach zero, it is very important that the trip current level I_{r1} is high enough. In this section an appropriate value for the trip current is derived. The system of differential equations valid for the resonant link voltage ramp down interval (mode 2) is given below

$$\begin{cases} V_{dc} - L_r \dfrac{di_{Lr}}{dt} - v_{Cr} = 0 \\ i_{Cr} = C_r \dfrac{dv_{Cr}}{dt} \\ i_{Lr} - i_{Cr} - I_{o1} = 0 \end{cases} \tag{3.202}$$

Substituting the differential equations of the system above gives a second order differential equation

$$\frac{d^2 v_{Cr}}{dt^2} + \frac{1}{L_r C_r} v_{Cr} = \frac{1}{L_r C_r} V_{dc} \tag{3.203}$$

The general solution to the second order differential equation is

$$v_{Cr}(t) = A\cos\omega_r(t - t_1) + B\sin\omega_r(t - t_1) + V_{dc} \tag{3.204}$$

where the characteristic angular frequency ω_r is expressed as

$$\omega_r = \frac{1}{\sqrt{L_r C_r}} \tag{3.205}$$

The resonant capacitor current becomes

$$i_{Cr}(t) = -\omega_r C_r A\sin\omega_r(t - t_1) + \omega_r C_r B\cos\omega_r(t - t_1) \tag{3.206}$$

The constants A and B of the general solution are given by the initial capacitor voltage and current, respectively

$$\begin{cases} v_{Cr}(t_1) = A + V_{dc} = V_{Cc} = KV_{dc} \\ i_{Cr}(t_1) = \omega_r C_r B = i_{Lr}(t_1) - I_{o1} = -I_{r1} \end{cases} \tag{3.207}$$

Mode 2 is finished when zero resonant link voltage are obtained, i.e. when

$$v_{Cr}(t_2) = 0 \tag{3.208}$$

A necessary condition for this to be met is

$$i_{Cr}(t_2) \le 0 \tag{3.209}$$

Applying the method for calculating final values, see Appendix C.1, gives

$$\left(0 - V_{dc}\right)^2 + \left(\frac{0}{\omega_r C_r}\right)^2 = \left((K-1)V_{dc}\right)^2 + \left(-\frac{I_{r1,min}}{\omega_r C_r}\right)^2 \qquad (3.210)$$

By solving the second order algebraic equation it is found that the minimum trip current is written

$$I_{r1,min} = V_{dc}\sqrt{\frac{C_r}{L_r}\left(K(2-K)\right)} \qquad (3.211)$$

By adding a small current margin

$$I_{m1} > 0 \qquad (3.212)$$

the trip current is given by

$$I_{r1} = I_{m1} + I_{r1,min} = I_{m1} + V_{dc}\sqrt{\frac{C_r}{L_r}\left(K(2-K)\right)} \qquad (3.213)$$

The initial capacitor current, used for determining the constant *B* of the general solution, thus becomes equal to

$$i_{Cr}(t_1) = \omega_r C_r B = -I_{m1} - V_{dc}\sqrt{\frac{C_r}{L_r}\left(K(2-K)\right)} \qquad (3.214)$$

Applying the method for calculating final values gives

$$i_{Cr}(t_2) = -\sqrt{I_{m1}^2 + 2I_{m1}V_{dc}\sqrt{\frac{C_r}{L_r}K(2-K)}} \qquad (3.215)$$

In the last expression, it is clearly seen that for a current margin I_{m1} equal to zero, the resonant link voltage reaches zero at zero capacitor current.

Zero voltage interval

During the zero voltage interval, mode 3, the resonant link voltage is clamped by the converter semiconductors. Also for this circuit, the zero voltage interval is inhibited by turning off one transistor of each converter half bridge. However, for the actively clamped quasi resonant DC link, the duration of the zero voltage interval can equal zero. This occurs if the output current to be set has a lower magnitude than the inductor current i_{Lr} when the zero voltage interval is entered. The differential equation valid for the zero voltage interval is written

$$V_{dc} - L_r \frac{di_{Lr}}{dt} = 0 \tag{3.216}$$

Integration gives

$$i_{Lr}(t) = i_{Lr}(t_2) + \frac{V_{dc}}{L_r}(t - t_2) \tag{3.217}$$

Thus, the duration of the zero voltage interval is expressed as

$$(t_3 - t_2) = \frac{L_r}{V_{dc}}\left(i_{Lr}(t_3) - i_{Lr}(t_2)\right) \tag{3.218}$$

The inductor currents inserted in the expression above are given by

$$i_{Lr}(t_2) = I_{o1} - \sqrt{I_{m1}^2 + 2I_{m1}V_{dc}\sqrt{\frac{C_r}{L_r}K(2-K)}} \tag{3.219}$$

and

$$i_{Lr}(t_3) = I_{r2} \tag{3.220}$$

Ideally, the second trip current level is determined by

$$I_{r2} = I_{m2} + I_{o2} \tag{3.221}$$

However, if the desired trip current level is lower than the inductor current at the end of the resonant link voltage ramp down interval, according to the expressions above, i.e. if

$$I_{m2} + I_{o2} \le I_{o1} - \sqrt{I_{m1}^2 + 2I_{m1}V_{dc}\sqrt{\frac{C_r}{L_r}K(2-K)}} \tag{3.222}$$

the duration of the zero voltage interval equals zero. In this case the trip current is expressed as

$$I_{r2} = i_{Lr}(t_3) = i_{Lr}(t_2) = I_{o1} - \sqrt{I_{m1}^2 + 2I_{m1}V_{dc}\sqrt{\frac{C_r}{L_r}K(2-K)}} \tag{3.223}$$

In any case, the duration of the zero voltage interval is given by

$$(t_3 - t_2) = \frac{L_r}{V_{dc}} \cdot \left(I_{r2} - I_{o1} + \sqrt{I_{m1}^2 + 2I_{m1}V_{dc}\sqrt{\frac{C_r}{L_r}K(2-K)}} \right) \tag{3.224}$$

For the case when the trip current is determined by (3.221), the duration of the zero voltage interval is rewritten as

$$(t_3 - t_2) = \frac{L_r}{V_{dc}}\left(I_{o2} - I_{o1}\right) + \frac{L_r}{V_{dc}}\sqrt{I_{m1}^2 + 2I_{m1}V_{dc}\sqrt{\frac{C_r}{L_r}K(2-K)}} + \\ + \frac{L_r}{V_{dc}}I_{m2} \tag{3.225}$$

Actually this is used to calculate the time needed to prolong the zero voltage interval in order to increase the clamp voltage V_{Cc}. This is achieved by allowing the margin I_{m2} to vary, and to calculate the corresponding additional time the zero voltage should be maintained by short circuiting each half bridge of the converter. The additional time is given by the last term of the previous expression, i.e.

$$(t_3 - t_2)_{boost} = \frac{L_r}{V_{dc}}I_{m2} \tag{3.226}$$

When simulating this circuit, this is used to control the clamp capacitor voltage V_{Cc}. If the clamp voltage is to low, the zero voltage interval is prolonged resulting in storage of excess energy in the inductor L_r. This excess energy is transferred to the clamp capacitor C_c after the resonant link voltage ramp up interval.

Resonant link voltage ramp up interval

The resonant link voltage ramp up interval, mode 4, starts as soon as the new switch state is applied, which forces a part of the resonant inductor current i_{Lr} to flow through the resonant link capacitor C_r, whereby its voltage starts to increase. Mathematically this mode is expressed by

$$\begin{cases} V_{dc} - L_r\dfrac{di_{Lr}}{dt} - v_{Cr} = 0 \\ i_{Cr} = C_r\dfrac{dv_{Cr}}{dt} \\ i_{Lr} - i_{Cr} - I_{o2} = 0 \end{cases} \tag{3.227}$$

From the system of differential equations, one second order differential equation is formed

$$\frac{d^2 v_{Cr}}{dt^2} + \frac{1}{L_r C_r} v_{Cr} = \frac{1}{L_r C_r} V_{dc} \tag{3.228}$$

The general solution is also in this case written

$$v_{Cr}(t) = A\cos\omega_r(t - t_3) + B\sin\omega_r(t - t_3) + V_{dc} \tag{3.229}$$

Consequently, the resonant capacitor current is written

$$i_{Cr}(t) = -\omega_r C_r A\sin\omega_r(t - t_3) + \omega_r C_r B\cos\omega_r(t - t_3) \tag{3.230}$$

The initial conditions determine the constants A and B of the general solution

$$\begin{cases} v_{Cr}(t_3) = A + V_{dc} = 0 \\ i_{Cr}(t_3) = \omega_r C_r B = i_{Lr}(t_3) - I_{o2} = I_{r2} - I_{o2} \end{cases} \tag{3.231}$$

Note that the initial resonant capacitor current is dependent on the trip current. Mode 4 ends as soon as

$$v_{Cr}(t_4) = KV_{dc} \tag{3.232}$$

A necessary condition for this to occur is

$$i_{Cr}(t_4) \geq 0 \tag{3.233}$$

By applying the method for calculating final values, see Appendix C, the capacitor current at the end of mode 4 is expressed as

$$\begin{aligned} i_{Cr}(t_4) &= \omega_r C_r \sqrt{\left(\frac{i_{Cr}(t_3)}{\omega_r C_r}\right)^2 + V_{dc}^2\left(1 - (K-1)^2\right)} = \\ &= \sqrt{i_{Cr}^2(t_3) + \frac{C_r}{L_r} V_{dc}^2 K(2-K)} \end{aligned} \tag{3.234}$$

The last expression shows that this resonant link is always capable of returning from zero voltage since there is always excess energy stored in the resonant inductor L_r. This excess energy is transferred to the clamp capacitor C_c, thereby charging it. Consequently, its capacitance has to be high enough to prevent the voltage from increasing to much.

Clamping interval

During the clamping interval, mode 5, the resonant circuit recovers. The differential equation for this mode is written

$$V_{dc} - L_r \frac{di_{Lr}}{dt} - V_{Cc} = 0 \tag{3.235}$$

The solution to the differential equation is found by integration, which gives

$$i_{Lr}(t) = i_{Lr}(t_4) - \frac{(K-1)V_{dc}}{L_r}(t - t_4) \tag{3.236}$$

The initial inductor current is determined according to

$$i_{Lr}(t_4) = i_{Cr}(t_4) + I_{o2} \tag{3.237}$$

The final inductor current, equals the resonant link output current, i.e.

$$i_{Lr}(t_5) = I_{o2} \tag{3.238}$$

The duration of the clamping interval is thus expressed by

$$(t_5 - t_4) = \frac{L_r}{(K-1)V_{dc}}\left(i_{Lr}(t_4) - I_{o2}\right) = \frac{L_r}{(K-1)V_{dc}} i_{Cr}(t_4) \tag{3.239}$$

When the clamping interval is finished, the resonant link voltage returns to V_{dc}. Note that the slope the voltage returns with, see Figure 3.8, is not determined by the resonant link passive components, but by its semiconductors.

Design expressions

Also this circuit has only two passive component values to be selected. Consequently, only two design constraints can be met. The constraints are, as for the other circuits, the duration of the zero voltage interval and the maximum resonant link derivative. Note that this is not really true for this circuit since the maximum resonant link voltage derivative is not determined by the passive components, as discussed above.

First, the maximum duration of the zero voltage interval is determined from (3.225)

$$(t_3 - t_2)_{max} = \frac{L_r}{V_{dc}}\left(I_{o2} - I_{o1}\right)_{max} + \frac{L_r}{V_{dc}} I_{m2} + \\ + \frac{L_r}{V_{dc}} \sqrt{I_{m1}^2 + 2 I_{m1} V_{dc} \sqrt{\frac{C_r}{L_r} K(2-K)}} \tag{3.240}$$

The maximum resonant link voltage derivative, obtained for mode 2, appears for the minimum value of the constant *B*, i.e. when

$$B = -\frac{1}{\omega_r C_r} \cdot \left(I_{m1} + V_{dc} \sqrt{\frac{C_r}{L_r}\left(K(2-K)\right)} \right) \tag{3.241}$$

which gives

$$\frac{dv_{Cr}}{dt} = \omega_r \sqrt{A^2 + B^2} = \\ = \omega_r \sqrt{V_{dc}^2 + \left(\frac{I_{m1}}{\omega_r C_r}\right)^2 + \frac{2 I_{m1} V_{dc}}{\omega_r C_r} \sqrt{K(2-K)}} \tag{3.242}$$

For mode 4 instead, the maximum resonant link voltage derivative appears when the constant *B* is at its maximum, i.e.

$$i_{Cr}(t_3)_{max} = \omega_r C_r B_{max} = \left(i_{Lr}(t_3) - I_{o2}\right)_{max} = \\ = \left(I_{o1} - I_{o2}\right)_{max} - \sqrt{I_{m1}^2 + 2 I_{m1} V_{dc} \sqrt{\frac{C_r}{L_r} K(2-K)}} \le \left(I_{o1} - I_{o2}\right)_{max} \tag{3.243}$$

resulting in

$$\left.\frac{dv_{Cr}}{dt}\right|_{max} = \omega_r \sqrt{A^2 + B_{max}^2} \le \omega_r \sqrt{V_{dc}^2 + \frac{L_r}{C_r}\left(\left(I_{o1} - I_{o2}\right)_{max}\right)^2} \tag{3.244}$$

For proper selection of the passive component values both these derivatives have to be considered.

4

Devices for resonant converters

Power semiconductor data sheet information is not valid for soft switching conditions. In order to interpret the simulated results in Chapter 5, some basic knowledge on power semiconductors is given and phenomena related to soft switching is discussed. The discussion is limited to diodes and insulated gate bipolar transistors since these are the only semiconductor devices used in the simulations. In the literature, more in dept discussions on power electronic semiconductor devices are found, for example [25], [44], [63]. General semiconductor physics is introduced in [60], [61]. Also, passive components like inductors and capacitors are to some extent discussed in this section. The discussion on passive components ends up with a presentation of the loss models used for these devices. In the literature, [42], [44], [62], [63], thorough presentations on passive components and their design are found.

4.1 Power diodes

Power diodes are usually separated into two categories, rectifier and switching diodes. The doping structures for both categories consist of the same layers, at least for the voltage levels discussed here. However, they behave different from each other, due to the fact that the length of the layers (in the direction of the current) and their doping densities are not the same. Therefore, the discussion is applied to power diodes in general, and then the differences between rectifier and switching diodes are explained.

Basic doping structure

The doping structure for a power diode differ, to some extent, from that of a low power and low voltage diode. The main difference originates from the fact that the power diode has to sustain high reverse voltages, implying that the doping structure has to withstand a high electric field, without failure. For this reason, all power electronic semiconductor devices are equipped with a long (in the direction of the electric field)

doping layer with low doping density. This doping layer, not found in low voltage and low power devices, is often termed drift layer. In Figure 4.1, the principal doping structure of a power diode is shown. Note that for real devices, the drift layer is considerably thicker than the other. However, in Figure 4.1, the thickness of the other layers are exaggerated for visibility.

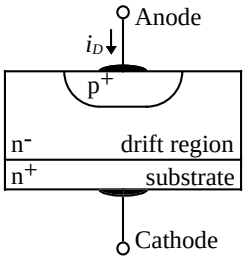


Figure 4.1 Principal power diode doping structure.

From the low power counterpart, the highly doped anode and cathode layers are recognised. The idea of having one thick layer of low doping density, is that the depletion region formed in the blocking state should mainly be located to this layer. The low doping results in a low peak electric field, and the large thickness means that the entire depletion region is held inside the drift layer, i.e. it does not extend into the cathode layer.

However, for so called punch through (PT) or buffer layer devices a geometrically short but highly doped buffer layer is located in between the drift and cathode layers. In this case, the idea is the same but the drift region has in this case an even lower doping density. Also, the drift region is allowed to extend across the entire drift region to reach the buffer layer. The result of this manipulation is that the drift region can be less thick. According to [44], the thickness can be approximately halved compared to the non punch through (NPT) case.

The diode is called a natural PT device since no additional drawbacks arises for the PT compared to the NPT device. Also, the highly doped substrate serves as buffer layer for PT-diodes.

For other types of devices, buffer layer devices are often referred to as asymmetrical. The reason is that the PT device can not block voltage of the opposite polarity, since none of the junctions sustain the high electric field strength resulting from the high doping densities on both sides of the blocking junction. For the diode, no forward blocking capability is provided, implying that this does not matter in this case.

Steady state operation

When a power diode is forward biased, heavy injection of minority carriers into the low doped drift region occurs. In fact, the density of free carriers can become orders of magnitude higher than depicted by the doping atom density. Consequently, the resistivity of the drift region becomes considerably lower than expected from the doping density. This phenomena is often referred to as conductivity modulation. Due to conductivity modulation, the forward voltage drop thus becomes rather low.

For conductivity modulation to be established, it is of course important that the diffusion length in the drift region is not too short compared to the thickness (in the direction of the minority carrier movement) of the drift region. Otherwise, recombination effects will cause a low minority carrier density in the bulk of the drift region.

When the diode is reverse biased, the anode-drift junction supports the voltage, i.e. a depletion region is formed at the junction. The depletion region extends mostly into the low doped drift region, see [44]. In this case a low doping atom density of the drift region is advantageous since the peak electric field strength is reduced. However, the depletion region also expands, implying that the drift region must be thick if it is desired that the depletion region must not extend across the entire drift region. However, since the diode is a natural PT device, the high doping of the cathode layer effectively prevents the depletion region from reaching the cathode contact.

Switching

When a semiconductor device traverses from the conduction state to the blocking, or vice versa, is termed a switching. For a power diode, several phenomena not seen for the low power counterpart appears. In Figure 4.2, typical turn-on and turn-off waveforms are shown for a freewheeling diode in a bridge application. The diode voltage v_D shown in Figure 4.2, is the voltage between the anode and cathode of the diode, i.e. $v_D=v_{AC}$.

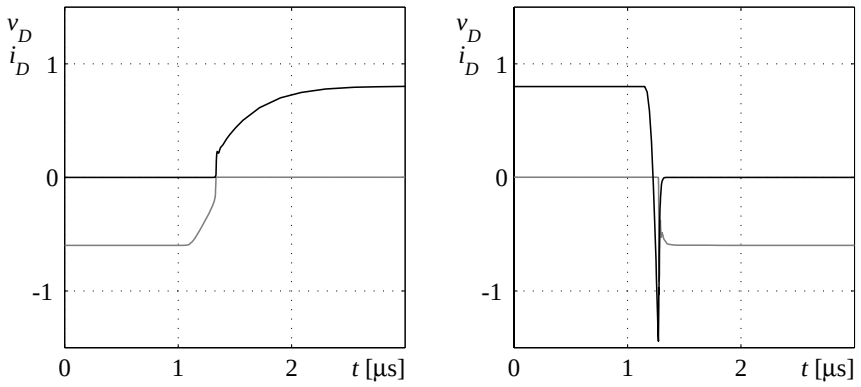
At turn-on, the diode reverse voltage first declines to zero. Then, the rectifying junction becomes forward biased. Consequently, the diode current starts to increase. The diode current rate of change, i.e. the diode current time derivative, is determined by the transistor turning off.

If the current rate of change is extremely high, a diode forward voltage peak is observed [44], depending on the fact that excess carriers are not

injected into the drift region at the corresponding rate. Hence, a conductivity modulation lag is observed. This results in a higher forward voltage drop than expected from the data sheets, due to the higher resistivity of the drift region. To some extent, the voltage peak observed is also due to stray inductance of the bonding wires of the diode housing. As seen in Figure 4.2, a turn-on voltage peak do not show up here.

When the diode current has reached the level determined by the load, the diode voltage returns from its peak level, to eventually reach its steady state. The phenomena where the forward voltage drop becomes considerably higher than what is expected from the data sheets is termed forward recovery.

The steady state forward voltage drop is determined both by the height of the junction potential barrier and the resistivity of the doping layers, mainly the drift region.



(a) (b)

Figure 4.2 The freewheeling diode current i_D (black) and forward voltage v_D (grey) during (a) turn-on, and (b) turn-off. Note that the corresponding transistor, an IGBT in this case, is non-ideal, i.e. it affects the diode switching waveforms.

A freewheeling diode turns off when the complementary transistor is turned on. First, the diode current starts to decrease at a rate determined by the power transistor. On the contrary to what is observed for the low power counterpart, the power diode turn-off current continues to decrease to become negative. This is due to the fact that the excess carriers stored in the drift region forward biases the anode-drift junction.

As soon as these excess carriers are swept out, the anode-drift junction can support the blocking voltage. Thus, the diode voltage becomes negative and the diode current decrease is inhibited. Now, the diode current starts to increase towards zero. The diode current in this part removes the free carriers in the anode and drift layers to create a depletion region. Also, at turn-off a negative voltage peak is observed. The voltage peak in this case is due to the stray inductance of the entire power electronic circuit. Note that the power diode reverse blocking voltage must be selected to sustain this peak level. The phenomena in which the diode current becomes negative is termed reverse recovery.

The main difference between freewheeling and rectifier diodes is that conductivity modulation is more pronounced for the latter, i.e. a larger amount of charge is stored in the drift region when a rectifier diode is conducting compared with a freewheeling diode. This implies that the rectifier diode will have a lower forward voltage drop, due to its lower on-state resistance. However, the switching transients will have a longer duration due to the larger amount of charge stored. This implies that the rectifier diode is more sensitive to high diode current derivatives. Both the forward recovery voltage peak and the reverse recovery current peak will thus be higher for a rectifier diode compared to a freewheeling diode of the same rating for a given diode current time derivative.

4.2 IGBTs

The IGBT [25], [44], [48], [63], was introduced to be a compromise between the bipolar junction transistor (BJT) and the metal oxide semiconductor field effect transistor (MOSFET). However, the IGBT has become more than just a compromise, due to its high ruggedness, moderate voltage drop and fairly high switching speed. Actually, in many modern designs it is the only reasonable device choice. The main reasons for its popularity is the high blocking voltage, up to 6 kV, its moderate driving requirements and its limited need for protective devices, i.e. snubbers.

Basic doping structure

The IGBT is a three terminal semiconductor device. The terminal named emitter is common to both input and output. The device is controlled by applying a voltage between the gate and emitter terminals. The output current flows between the collector and emitter terminals. The gate-emitter region is split into thousands of cells. In Figure 4.3, one such cell of a NPT-IGBT and also one of a PT-IGBT are shown. The only

structural difference between these two, is that the PT device has an additional doping layer, termed buffer.

The description presented here, focuses on the NPT device. The most commonly used n-channel IGBT circuit symbol is used throughout the entire text and is therefore not shown here. Other circuit symbols for the IGBT do exist, but this is the most frequently used.

The reason for dividing the gate-emitter structure into cells, is to keep the channel resistance low by increasing its cross-sectional area and decreasing its length. Further on, the emitter metallisation extends over the body region, which is done to short circuit the body-emitter junction. This is used to reduce the risk of entering latchup, a fault condition discussed later on.

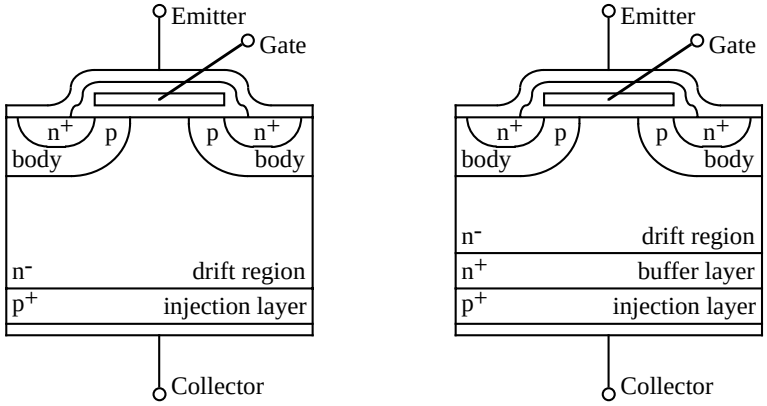


Figure 4.3 Principal doping structure for (a) the NPT-IGBT, and (b) the PT-IGBT.

Steady state operation

From Figure 4.3 it is seen that the doping structure of an IGBT looks similar to the one of a MOSFET. For the NPT device the only difference is the presence of a heavily doped injection layer at the IGBT collector metallisation. The reason for having this layer, is that holes should be injected into the drift region to obtain conductivity modulation when the device operates in the conduction state. The lack of conductivity modulation is the main drawback of the MOSFET, being a majority carrier device.

In the on state, similar to the MOSFET, a channel is created in the body region underneath the gate oxide, connecting the n-doped emitter and

drift regions. The channel supports an electron current, flowing from the emitter into the drift region. The negative charge of the electrons, attracts holes from the injection layer, which in turn causes conductivity modulation of the drift region.

When the IGBT operates in the forward blocking state, the drift region supports the voltage. Similar to the power diode case, a depletion region is formed in the drift region. For a NPT device, this is also true for the reverse blocking state, i.e. when the IGBT is blocking a collector-emitter voltage of reverse polarity. However, the PT-IGBT can not block a collector-emitter voltage of negative polarity, since the injection-buffer junction should support the voltage in this case. Both these regions are highly doped, resulting in a high electric field strength even at low blocking voltages. Consequently, avalanche breakdown will occur for low reverse blocking voltage. This is the reason why the PT-IGBT is often termed asymmetric.

In Figure 4.4 the current-voltage characteristics of a typical IGBT is shown. The output characteristic of an IGBT shows the collector current, i_C, as a function of the collector-emitter voltage v_{CE}, for different gate-emitter voltages v_{GE}.

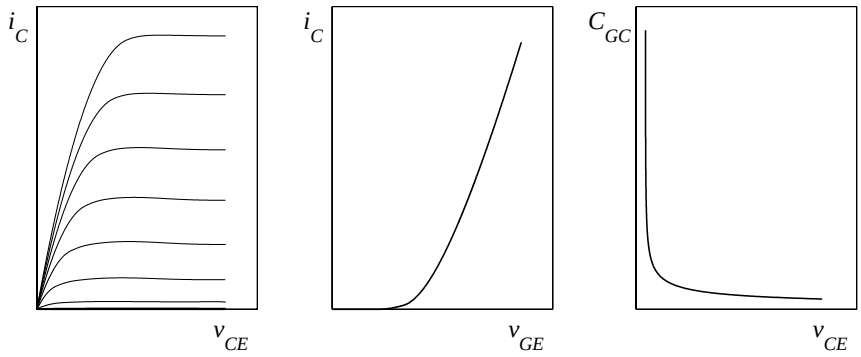


Figure 4.4 Output characteristic for low collector-emitter voltages (a), transfer characteristic (b), and gate-collector capacitance as a function on the collector-emitter voltage (c).

The transfer characteristic shows the collector current as a function of the gate-emitter voltage, when the IGBT is in the active region. The transfer characteristic is thus mainly interesting for the switching transients, since otherwise the device should operate in the on-state or off-state regions.

Switching at inductively clamped load

Figure 2.2 shows typical switching waveforms for an IGBT operating at inductively clamped load in a bridge application. The corresponding freewheeling diode is regarded as being ideal. At turn-on of the IGBT, the gate-emitter voltage v_{GE} must first reach its threshold level, $v_{GE(th)}$, before the collector current i_C starts to increase. The time needed to do this is termed the turn-on delay time $t_{d(on)}$.

The gate-emitter threshold voltage is seen in the transfer characteristic of Figure 4.4 as a sharp bend where the collector current becomes non-zero.

Note that since the IGBT has a capacitive input, the gate resistor determines the delay time. Also note that the internal capacitance is varying due to depletion layer thickness, i.e. collector-emitter voltage. The gate-collector capacitance is the most affected. Its typical dependence on collector-emitter voltage is shown in Figure 4.4, where the fairly sharp knee approximately corresponds to a collector-emitter voltage equal to the applied gate-emitter voltage.

After the turn-on delay time, the gate-emitter voltage continues to increase and the collector current starts to increase. The collector current time derivative is determined by the transfer characteristics, see Figure 4.4, which implies that it is determined by the size of the gate resistor. The duration of this current rise interval is termed current rise time t_{ri}.

Following the current rise interval, the voltage fall interval commences. The duration of this interval is termed voltage fall time t_{fv}. The voltage fall interval can be subdivided into two portions. The first part is similar to the voltage fall of a MOSFET, i.e. the Miller plateau. The second part has considerably lower fall rate mainly due to conductivity modulation lag.

IGBT turn-off also starts with a delay time, $t_{d(off)}$, due to the fact that the gate-emitter voltage has to decrease to the level determined by the transfer characteristic before the collector-emitter voltage starts to increase. During the voltage rise time t_{rv} the collector-emitter voltage increases and the gate-emitter voltage is constant due to the Miller effect.

When the collector-emitter voltage has reached the level of the DC link voltage, the freewheeling diode becomes forward biased. Hence, the IGBT collector current starts to decrease. The collector current fall rate is also determined by the gate-emitter voltage through the transfer characteristic, i.e. the fall rate is essentially determined by the gate resistor value. When

the gate-emitter voltage has decreased to its threshold level $v_{GE(th)}$, the channel in the body region is removed, corresponding to that the MOSFET part of the IGBT is turned off. In IGBT data sheets this part of the collector current fall is termed t_{fi}.

However, there are still excess carriers stored in the IGBT drift region. Since the channel is not present, these carriers can not be removed through the channel. Instead, there will be a long collector current tail where the current falls at a very low rate. This low rate is due to the fact that the excess carriers are removed by internal recombination, which is a very slow process [44]. Note that the current tail fall rate is not affected by the gate resistor value. However, the gate resistor value has some influence since the initial magnitude of the current tail is dependent on the amount of excess carriers removed from the drift region during t_{fi} [25]. For a low gate resistor value, t_{fi} will be short and hence the density of excess carriers is almost unaltered during t_{fi}. For a high gate resistor value on the other hand, a large amount of the excess carriers are removed during the comparably long t_{fi}. Thus, the initial magnitude of the collector current tail will be lower in the second case.

Latchup

The doping structure of the IGBT contains a parasitic thyristor (pnpn) structure, see Figure 4.3. The injection layer and the emitter region forms the anode and cathode, respectively, of the parasitic thyristor structure. The body region forms the gate (p-base) and the drift region the n-base of this structure. The parasitic thyristor structure must not be triggered, a state termed latchup, since the thyristor can not be turned off unless its anode current is forced to zero by surrounding circuit elements.

Though not obvious, the thyristor structure can be trigged by a lateral current, forward biasing the body-emitter junction. The lateral current flow arises from a part of the hole current, injected from the collector, first being attracted by the negative charge of the channel. When the holes enters the body region, electrons from the emitter metallisation covering the body are attracted, which the injected holes recombine with. Hence, a lateral current flow in the body region results. If the resistivity of the body is high enough, the lateral current can forward bias the body-emitter junction. Note that even though the emitter metallisation also covers the body, i.e. short circuits the emitter and body regions, the body-emitter junction can be forward biased in the interior of the structure.

Actually, latchup is distinguished into two different cases, static which occurs in the on-state and dynamic which occurs during turn-off. Static latchup is due to a too high collector current, resulting in a lateral voltage drop forward biasing the body-emitter junction. Hence, static latchup is avoided by not allowing a higher collector current than specified by the manufacturer.

Dynamic latchup occurs at turn-off, after the channel has been removed. Since the collector-emitter voltage already is at the blocking level, see Figure 2.2, the depletion region is being established in the drift region. As a consequence, the emitter efficiency for the remaining pnp-structure increases, since the effective base length decreases. The effective base length is the portion of the drift region remaining undepleted. The emitter efficiency increases due to the fact that the possibility of recombination decreases if the base length is short.

The problem is that an increased emitter efficiency results in the fact that a larger part of the total current is collector current of the pnp-structure, which also is the lateral current in this case. Hence, if a gate resistor of low resistance is used, the lateral current might increase when the channel is removed, compared to the on-state case. Then, dynamic latchup will occur for a lower IGBT collector current than static would. Therefore, it is also important not to use a gate resistor value lower than specified by the manufacturer.

Switching under zero voltage conditions

One of the main problems related with soft switching appears due to poor understanding of power semiconductor physics, since it is assumed that data sheet information is still valid at soft switching. However, data sheet information for IGBTs is in most cases given for inductively clamped load, i.e. constant load current during the switching transients [34]. Also, the information is only valid for a certain constant DC link voltage. In the literature [34], [43], [52], a lot of problems appearing due to soft switching are discussed.

One of the most discussed phenomena observed, is the current tail bump occurring at IGBT zero voltage turn-off. In Figure 2.9, the current tail bump is clearly seen. According to [52] the reason for this bump is that during ZVS turn-off the excess carriers stored in the drift region are not forced out by the expanding depletion region as for hard switched turn-off. Consequently, after the channel is removed the collector current continues its decrease and no current tail is observed until the IGBT

collector-emitter voltage begins to increase. The current tail bump results in higher losses at ZVS turn-off than expected from data sheet information. Nevertheless, the turn-off losses are lower for ZVS than for hard switching [34].

Another problem observed, is due to the conductivity modulation lag [34], [43], appearing for high collector current time derivatives. For an IGBT, the origin of this lag is the same as for the power diode discussed earlier. This means that the collector current increases at a rate higher than the rate which excess carriers are injected into the drift region, needed to establish conductivity modulation.

In [34] problems arising from device packaging are also discussed. Here, the problem is that bonding wire inductance not only gives an increased forward voltage drop but also can result in uneven current distribution among several IGBT chips packaged in the same module, at high current time derivatives. Uneven current distribution leads to increased losses and also increased device stress.

The soft switching problems discussed above are investigated in the simulations presented in Chapter 5, where at least the current tail bump is clearly seen.

4.3 Inductive elements

A resonant converter has at least one inductive element being a part of the oscillatory circuit. Moreover, a VSC also has a current stiff output filter, i.e. the output filter must contain inductive elements connected to the converter output terminals. To be able to calculate the overall efficiency from simulations, inductor models are needed. The simulation models used and methods to determine their parameters are discussed.

Magnetic materials

Inductive elements consist of one or several copper wire windings which in most cases are wound upon an iron core. In this section the different core materials used in most cases are discussed. Core materials and inductor design are thoroughly discussed in for example [42], [44], [62], [63].

Magnetic components for power electronic applications, such as inductors and transformers, are often designed only for the intended application, due to the fact that it is impossible to maintain a storage of the wide

variety of components needed. This means that for most power electronic applications, inductor design is a natural part of the development, since almost every power electronic circuit contains this kind of components.

Selection of appropriate core material is an important issue in magnetic component design. The material choice is to a large extent determined by the frequency spectra of the magnetising current. The frequency spectra of interest for power electronics, range from 50 Hz (thyristor bridge commutation inductors) to several MHz (pulse transformers in for example transistor drive circuitry). There are mainly three types of core materials used to cover this frequency spectra.

For the low frequency region (50 Hz to some tens of kHz), alloys of iron and for example chrome, silicon or cobalt are used. These alloys are characterised by high electric conductivity and high saturation flux density (up to 1.8 T). The high conductivity make this material subject to eddy current losses, i.e. the applied magnetic flux easily induces current in the core. The induced currents results in resistive losses, referred to as eddy current losses. To partly overcome this problem these cores are laminated, or in some cases manufactured as steel tape, to decrease the length of the current paths and the magnitude of the currents induced.

For the mid frequency region (1 kHz to 100 kHz), cores made from powder of the same mixtures as in the previous case, are used. The iron powder particles are covered with an insulating layer, and forced together with pressure. Since the powder particles are electrically insulated from each other, the conductivity and thus the eddy current losses of the core become low. However, another loss component referred to as hysteresis loss, becomes more significant compared to the case for the previously discussed laminated cores.

In the upper frequency region (30 kHz to 10 MHz), soft ferrite cores are commonly used. Ferrites are ceramic compounds, consisting of iron oxide together with usually zinc or nickel. Other compound materials are also used, and also mixtures of several compound materials are possible. The crystals of the ferrite are typically 10–20 μm in dimension, thus limiting the eddy current path length and the magnitude of the current induced.

Ferrites, like other magnetic materials have losses associated with the hysteresis of the *B-H* loop. Hysteresis occurs due to friction associated with magnetic domain wall movement and magnetic domain rotation when an external magnetic field *H* is applied, causing the change in magnetic flux density to lag the change in magnetic field. This lag is known as hysteresis. For an AC magnetic field, a loop is formed in the *B-H* plane,

forming the hysteresis curve. The area enclosed by such a loop corresponds to the hysteresis loss.

In most cases the manufacturer specifies the core losses as curves showing the loss per volume or mass unit, depending on the flux density and the frequency. In some cases, empirically derived expressions are given instead of curves. There are however also analytically derived loss models like the Steinmetz formula [44] where the specific losses are given by

$$p_{Fe} = k_h f^{a_1} \hat{B}_{ac}^{a_2} + k_{ec} f^2 \hat{B}_{ac}^2 \tag{4.1}$$

where a_1, a_2, k_h, and k_{ec} are material dependent constants. The first term of the Steinmetz formula above, is due to hysteresis losses and the second term due to eddy current losses. Note that the AC peak magnetic flux density is needed to calculate the iron losses. Several other forms of Steinmetz formula are often used. For example, the hysteresis loop is travelled once each period, implying that a_1=1. Also, if the hysteresis loop is approximated as being rectangular, a_2=2 can be assumed.

For the magnetic core materials used in the simulations of Chapter 5, the manufacturer [67] gives the specific iron losses according to the empirical relationship

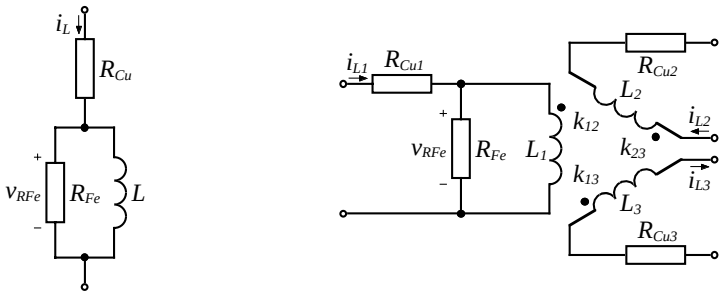
$$p_{Fe} = \frac{f}{\frac{a}{\hat{B}_{ac}^3} + \frac{b}{\hat{B}_{ac}^{2.3}} + \frac{c}{\hat{B}_{ac}^{1.65}}} + \left(d f^2 \hat{B}_{ac}^2 \right) \tag{4.2}$$

where a, b, c and d are material dependent constants. Specific iron losses in this case means that the losses are given in the unit mW/cm^3.

Simulation models

To be able to simulate the battery chargers with quasi resonant DC links, models of the magnetic components are needed. To estimate the efficiency, the losses of these components have to be included. This is due to the fact that these losses must be compensated for, to maintain the output power. This means that the losses in other parts of the circuit may increase, since the input power becomes higher.

In Figure 4.5, simulation models for an inductor and a three winding transformer are shown. The two winding transformer model used is similar to the three winding counterpart with the tertiary winding removed.



(a) (b)

Figure 4.5 Simulation models for (a) an inductor, and (b) a three winding transformer.

In Figure 4.5, resistors are included in the magnetic component equivalents to model power dissipation. The resistors named R_{Cu} are used to model the copper winding losses. Consequently, for the three winding transformer there is one such resistor for each winding. Note that the copper winding resistance is temperature dependent, implying that the operating winding temperature has to be assumed. The average winding losses, for each winding, is calculated from

$$P_{Cu} = R_{Cu} I_L^2 \tag{4.3}$$

where I_L is the RMS current through the corresponding winding with resistance R_{Cu}.

The resistor used to model the iron losses of the entire core is denoted R_{Fe}. Here, the magnetising current i_m is used to calculate the flux density of the core. The magnetising current, referred to the primary winding, is calculated as

$$i_m = i_{L1} + \frac{N_2}{N_1} i_{L2} + \frac{N_3}{N_1} i_{L3} \tag{4.4}$$

where N_1, N_2 and N_3 denotes the number of winding turns for the primary, secondary and tertiary windings, respectively. Note that for the single winding inductor and the two winding transformer, the magnetising current is found just by setting the currents of the absent windings equal to zero. According to Appendix D, the flux density depends on the magnetising current as

$$B = \frac{L_1 i_m}{N_1 A_{Fe}} \tag{4.5}$$

where L_1 denotes the self inductance of the primary and A_{Fe} the iron core cross-sectional area, perpendicular to the magnetic flux. By performing spectral analysis on the flux density calculated, the loss associated with each frequency component is calculated according to (4.2). The iron losses for these frequencies are summed and multiplied with the iron core volume, giving the total iron losses P_{Fe}, in the unit W. The resistor R_{Fe}, used to model the iron losses in the simulation equivalent model, is calculated from

$$R_{Fe} = \frac{V_{RFe}^2}{P_{Fe}} \tag{4.6}$$

where V_{RFe} is the RMS value of the magnetising voltage, see Figure 4.5. Note that the equivalent models are only used to estimate the influence of the magnetic component losses on the other devices of the entire circuit. To calculate the actual losses of the magnetic components, equation (4.2) is used on the simulated data.

Note that also the magnetic coupling factors, k_{12}, k_{13} and k_{23}, are included in the three winding transformer model shown in Figure 4.5.

4.4 Capacitors

Different kinds of capacitors are used in power electronic circuits. Here, only two are discussed, the non-polarised metallised film polypropylene capacitor and the polarised wet aluminium electrolytic capacitor. Non-polarised capacitors are used in output filters and for applications with high capacitor voltage time derivative, like commutation circuits. Polarised capacitors are used when a high capacitance is needed, for example for DC link capacitors.

Design

Metallised film polypropylene capacitors have a thin plastic film to support the metal layer of the electrodes. The plastic used for the film can for example be polyester. If the plastic film has electrodes (of the same polarity) on both sides it is referred to as double metallised film. The dielectric consists of a polypropylene film. To avoid air pockets resulting in a locally high electric field strength, the polypropylene film should be somewhat porous to be able to absorb oil, according to [62].

Wet aluminium electrolytic capacitors contains a fluid, the electrolyte, between the aluminium electrodes. The electrolyte is absorbed by paper in between the aluminium electrodes, in order to avoid air pockets. Since the electrolyte is conductive, the aluminium electrodes are electrically close together, only separated by the dielectric of the capacitor. The dielectric constitutes of a thin aluminium oxide layer on the positive electrode.

Simulation model

Both the metallised polypropylene and the wet aluminium electrolytic capacitors are modelled by the capacitor equivalent shown in Figure 4.6.

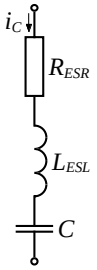


Figure 4.6 Capacitor simulation model.

In Figure 4.6 two parasitic elements are shown, L_{ESL} and R_{ESR}. The equivalent series inductance L_{ESL} is due to stray inductance of the leads and the metal layers forming the electrodes. A numerical value for L_{ESL} is often specified in the manufacturer data sheets. The equivalent series resistance R_{ESR} is due to the resistance of the leads and also dielectric losses. Therefore, R_{ESR} is frequency dependent according to

$$R_{ESR}(f) = R_s + \frac{\tan\delta_0}{2\pi f C} \tag{4.7}$$

where the term tan δ_0 is referred to as the dielectric dissipation factor. As the name hints, the dielectric dissipation factor is due to losses within the dielectric itself. This term is regarded as constant for the possible operating frequencies. However, since the voltage across the dielectric decreases with increasing frequency for a constant RMS value of the capacitor current i_C, the dielectric losses also decrease with increasing frequency as concluded from (4.7). The constant term R_s contained in the expression for R_{ESR} is due to the resistance of the leads and the electrodes.

However, since the equivalent series resistance is frequency dependent, it can not be used directly in an online simulation model. Instead, spectral

analysis is used to calculate the RMS capacitor current for each frequency. Then the loss of the corresponding frequency is calculated from

$$P_{ESR}(f) = R_{ESR}(f) \cdot I_C^2(f) \tag{4.8}$$

The loss contribution for the different frequency components are summed, which gives the total losses P_{ESR}. Finally, an equivalent series resistance without frequency dependency is calculated according to

$$R_{ESR} = \frac{P_{ESR}}{I_C^2} \tag{4.9}$$

where I_C is the RMS value of the total capacitor current. Also in this case, the simulation model R_{ESR} is only used to influence the rest of the power electronic circuit. To calculate the capacitor losses, each frequency component is treated separately, as in expression (4.8).

5

Simulation

Simulations are used in order to evaluate the battery charger equipped with the different quasi resonant DC links investigated. The passive component values used for the resonant links are calculated according to the design expressions developed in Chapter 3. The simulations are used to verify the design expressions and to estimate the energy efficiency of the battery charger using the different quasi resonant DC links. The simulations, giving the waveforms and efficiency, are performed for battery charging at rated power. A hard switched battery charger is also simulated as a reference to investigate the improvement in efficiency, if any, gained by the use of an quasi resonant DC link. The Analogy software SABER™ is used for all the simulations in this chapter.

5.1 General simulation model

The general simulation model used throughout all the simulations is shown in Figure 5.1. Note that both the line side and the battery side output filters consist of inductors only, to simplify the controller. The quasi resonant DC link is shown as a block named QRDCL, to show its location independent of the resonant circuit used. The DC link capacitor is not included in this block, but drawn outside for visibility. For the hard switched battery charger, the DC link supply rails of the battery charger is directly connected to the DC link capacitor. This is achieved simply by creating a QRDCL block with two feed through connections.

The resonant link controller block is needed both to delay the modulator control signals until zero voltage is achieved and also to control the resonant link switches. To accomplish the latter need, different signals depending on the type of resonant link used, are measured. The control of some of the circuits even relies on knowledge about the resonant link output current both prior to and after each resonant cycle. To control these circuits, the load currents are also used by the resonant link controller. The controller and modulator block is independent of the circuit used and is described in Appendix A and Appendix B.

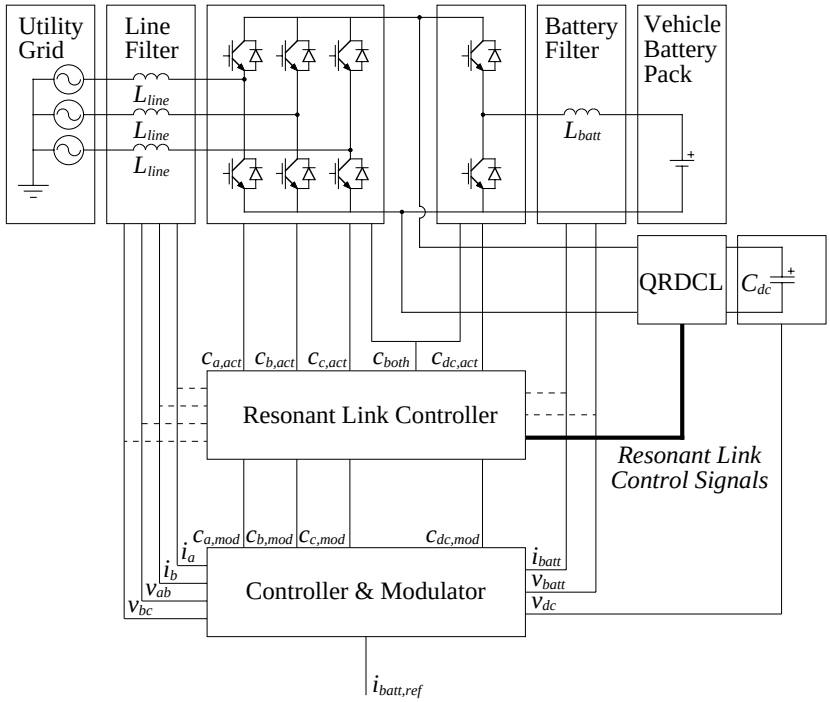


Figure 5.1 General simulation model.

The utility grid considered in the simulations is a symmetric 400 V, 50 Hz three phase AC system. This corresponds to the consumer level of the Swedish power grid. The rated DC link voltage used in the simulations is set to 750 V. The rated battery voltage is 375 V, which is approximately two times higher than the battery voltage of most present electric vehicles. However, the battery charger simulated has the same ratings as the one designed and tested in [3], except for the rated power which is 10 kW in this case but 75 kW in [3]. The frequency of the modulation carrier is selected to equal 4.95 kHz, implying that the modulator switching frequency is 4.95 kHz. Note that the switching delay introduced by the resonant link operation, might result in a decreased actual converter switching frequency.

General simulation devices and passive components

The semiconductor switches used in the simulations are selected to work as close to as possible, but below, the level given by (2.1). The line and battery side converter IGBTs used in the simulations are of the medium fast types International Rectifier IRGPH40M and IRGPH50M, respectively. The quasi resonant DC link IGBTs are all of the fast type

IRGPH50K from the same manufacturer. The power diodes are of type Harris MR10150. To meet the constraint (2.1) several diodes are series or parallel connected, when needed. The IGBTs have a voltage rating of 1200 V, implying that only parallel and not series, connection is needed. These semiconductor devices are selected since they are the only suitable by means of ratings, contained in the Analogy software SABER™ used for the simulations.

As mentioned in Chapter 4, the resistance of the IGBT gate resistor affects the switching times. For all IGBTs used in the simulations, the gate resistors are selected to the minimum values recommended in [66]. This is done due to the fact that the switching times are only specified for these values in [66]. Thus, the model validity by means of switching times for the hard switched case, can only be investigated for these gate resistor values. Therefore, each IGBT of type IRGPH50M and IRGPH50K is equipped with a 5.0 Ω gate resistor and each IRGPH40M is equipped with a 10.0 Ω gate resistor. The case temperature, for all semiconductors used in the simulations, is set to 70 °C.

Besides the gate resistors each IGBT gate drive circuit consists of an ideal voltage source which assumes the discrete values ±15 V, depending on the gate drive circuit input signal level. In the hard switched case a blanking time is also implemented in the gate drive circuits, to prevent from transient short circuit during switching. Essentially, blanking time is provided by delaying IGBT turn-on by 2 μs but not delaying turn-off.

The output filter inductors on both the line and battery sides are simulated as being based on iron powder cores, to eliminate the problem of air gap losses, see Appendix D. However, for the iron powder cores manufactured by Micrometals the operating temperature is of great concern. In the data book [67] it is stated that phenomena like thermal runaway can become a problem at operational temperatures as low as 75 °C. It is also stated that the core materials is especially prone to thermal runaway if the core loss exceeds the copper loss, which should be avoided.

The inductive elements of the quasi resonant DC links used in the simulations are therefore designed to operate at a temperature close to 90 °C at an ambient temperature of 40 °C, which make the inductors rather bulky with respect to the rating. For the line and battery side inductors such a moderate temperature rise would make the inductors even too bulky. Therefore, the filter inductor operating temperature is limited to 125 °C instead. According to the data book provided by Micrometals, this is not a severe problem due to the fact that at this rather low frequency, the dominating core loss is likely to be hysteresis loss which is not prone

to thermal runaway. Furthermore, it is also assumed that only one side of the inductor is actually a cooling surface, since the inductors must be mounted somehow. This results in quite conservative output filter designs. The design procedure is similar to the one for a tape wound C-core discussed in Appendix D. However, iron powder cores are usually not equipped with an explicit air gap but instead several distributed air gaps resulting from the insulation between the iron powder grains. This means that the material choice depends on both the iron losses and the desired inductance. The manufacturers provide an quantity, the A_L value, for each core and material it is available in. The inductance L is related to the A_L value according to

$$L = A_L N^2 \tag{5.1}$$

Selection of appropriate line side output filter inductance values is covered in [4]. The battery side inductance value is determined in a similar way and is therefore not discussed here. The most important data for the output filters used in the simulations are given in Table 5.1 below. In Table 5.1, the winding DC resistance is given, which is calculated based on the assumption that the winding temperature is 90 °C. Skin effect of the winding currents is neglected in all the simulations, since it is assumed that Litz wire [44], i.e. several parallel conductors, is used.

Table 5.1 Line and battery side inductors used in the simulations.

Inductor	Core	A_L (nH/N^2)	R_{Cu} (mΩ)	L (mH)	R_{th} (°C/W)
L_{line}	2×T650-28	254.0	206	15.2	0.60
L_{batt}	3×T650-28	381.0	168	14.9	0.47

The core material used in the output filters, i.e. Micrometals material -28, has the constants for calculation of the losses according to (4.2), given in Table 5.2 [67]. The same constants are also given for some other materials used for the resonant link inductors, which are discussed later in this chapter.

Table 5.2 Core material loss calculation constants.

Material	a	b	c	d
-2	$4.0 \cdot 10^{9}$	$3.0 \cdot 10^{8}$	$2.7 \cdot 10^{6}$	$8.0 \cdot 10^{-15}$
-8	$1.9 \cdot 10^{9}$	$2.0 \cdot 10^{8}$	$9.0 \cdot 10^{5}$	$2.5 \cdot 10^{-14}$
-28	$3.0 \cdot 10^{8}$	$3.2 \cdot 10^{7}$	$1.9 \cdot 10^{6}$	$3.1 \cdot 10^{-13}$

Since the core losses given by expression (4.2) is specific, i.e. presented in mW/cm^3, the volume of the core is needed to determine the actual losses. The volume of a single core of type T650 is 734 cm^3 according to [67].

The DC link capacitor is selected based on its current handling capability and on the capacitance. Furthermore, electrolytic capacitors usually do not have a rated voltage exceeding 500 V, implying that series connection is necessary. An appropriate capacitance value is determined in [4], and is not discussed here. The DC link capacitor selected for simulation actually consists of two series connected 4.7 mF, 450 V capacitors manufactured by Rifa [65]. The equivalent properties, for the two capacitors together are given in Table 5.3 below. Some of the data given in Table 5.3 are actually not given explicit in [65], but instead derived to fit the model of Figure 4.6. However, the data given in Table 5.3 do not contradict the data given by the manufacturer.

Table 5.3 Specification of the DC link capacitor used in the simulations.

Capacitor	Type	C (mF)	$\tan\delta_0$	R_s (mΩ)	L_{ESL} (nH)	R_{th} (°C /W)
C_{dc}	2×PEH200YV447DQ	2.35	0.020	14.0	70	1.5

General design criteria for the quasi resonant DC links

All the quasi resonant DC links are designed to exhibit a maximum output voltage derivative of 1000 V/µs. Furthermore, the maximum duration of the zero voltage interval is selected to be 1 µs. Nevertheless, the duration of the zero voltage interval is allowed to be longer for energy storage or clamp capacitor voltage control, i.e. 1 µs maximum duration is without application of such control. For all the quasi resonant DC links utilising clamp action, the clamping factor K is set to 1.2.

The maximum resonant link output current change assumed at the design stage, equals the battery charging current. Actually, this is the worst case resonant DC link output current change only if it is assumed that none of the line side converter half bridges are switched simultaneously, to contribute to a larger change.

5.2 Simulation of the two switch passively clamped quasi resonant DC link

First, appropriate passive component values are determined for the two switch passively clamped DC link. Then, the simulation model is discussed and suitable passive component parameter values for loss calculation are

given. Last, the simulation results verifying the design expressions, are shown and the losses calculated. Figure 5.2 shows the passively clamped two switch quasi resonant DC link, used in the simulation model in Figure 5.1. Note that the DC link capacitor is included in Figure 5.2, even though it is not a part of the QRDCL block shown in Figure 5.1.

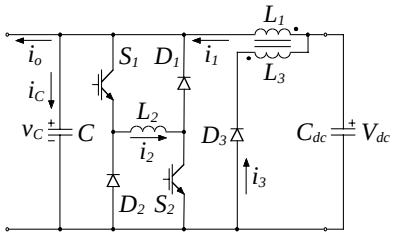


Figure 5.2 The passively clamped two switch quasi resonant DC link used in the simulation, including the DC link capacitor.

Simulation model and parameters

Since this circuit is passively clamped and has no energy storage capacitor, capacitor voltage control is not needed in this case. Also, this circuit has a third degree of freedom, which in this case is used to limit the resonant inductor current i_2 to the same level as the rated battery charging current. The design expressions for this circuit, i.e. (3.58), (3.63) and (3.64) determined in Section 3.1, gives approximately the following component values

$$\begin{cases} L_1 = 100.82\ \mu\text{H} \\ L_2 = 55.86\ \mu\text{H} \\ L_3 = 2520.5\ \mu\text{H} \\ C = 66\ \text{nF} \end{cases} \tag{5.2}$$

The passive component values selected, only approximately fulfils the design expressions since there are discrete steps between component values manufactured. The simulations are intended to be as realistic as possible and therefore only available component values are used.

The inductive components are designed according to Table 5.4 below. Note that in this design the magnetic coupling factor of the clamping transformer, i.e. L_1/L_3, is assumed to be perfect even though no precautions are made to fulfil this. In the next chapter, a battery charger using this quasi resonant DC link is implemented and in this case the magnetic coupling factor is considered in the design.

Table 5.4 Resonant link inductor specifications used in the simulations.

Inductor	Core	A_L (nH/N^2)	N (turns)	R_{Cu} (mΩ)	R_{th} (°C/W)
L_1/L_3	T520-2	20.0	71/355	39.6/1485	1.55
L_2	T300-2	11.4	70	39.2	4.24

The resonant capacitor C, actually consists of 3 parallel 22 nF polypropylene capacitors with loss parameters approximated from the Rifa PHE 428 series [64]. The loss parameters used for the resonant capacitors of all the quasi resonant links are given by

$$\begin{cases} R_s = 19.45\ \text{m}\Omega \\ \tan\delta_0 = 0.000278 \end{cases} \tag{5.3}$$

The thermal resistance, R_{th}, varies for the resonant link capacitors for the different circuits, depending on their different physical size. However, they are all designed not to exceed a temperature rise of 35 °C. The equivalent series inductance, L_{ESL} in Figure 4.6, is set to zero for all the resonant capacitors in the simulations due to lack of manufacturer data.

The resonant link IGBTs, S_1/S_2 according to Figure 5.2, actually consist of two parallel IGBTs of type IRGPH50K each. As previously mentioned, each IGBT is equipped with a 5.0 Ω gate resistor. The diodes D_1/D_2 are modelled by four parallel connected MR10150 diodes each. The clamping diode, D_3, consists of five series connected diodes of the same type. The reason for this is that D_3 has to withstand a blocking voltage of 4500 V. Since MR10150 is a 1500 V diode, five such are needed to fulfil the requirement given by (2.1).

Simulated waveforms and losses

To verify the design expressions given for the passively clamped two switch quasi resonant DC link, i.e. (3.58), (3.63) and (3.64), simulations are used. One period of the fundamental grid frequency is simulated in order to calculate the average losses, since the losses are likely to be dependent of the current level and thus vary with time. The simulated waveforms are presented in three different time scales. The shortest time scale is for investigation of the soft switching behaviour of the IGBTs in the circuit. The medium time scale is used to show the resonant link waveforms, similar to the ones shown in Chapter 3. The longest time scale equals one period of the fundamental grid frequency, to show how the line and battery currents are affected by soft switching.

First, the quasi resonant DC link quantities, i.e. voltages and currents, of interest are investigated. Figure 5.3 shows the resonant link waveforms at turn-on of the upper IGBT of the battery side converter at rated current, i.e. maximum increase of the resonant link output current i_o. As discussed in the previous section, this is the worst case increase only if it is assumed that no other half bridge is switched during the resonant cycle, contributing to a larger increase.

From Figure 5.3 it is seen that the resonant link voltage, v_C, enters clamping. According to the design constraints this should not happen at a maximum increase of the output current, since the resonant current i_1 should equal the output current before clamping occurs. This in turn results in a resonant link capacitor current i_C equal to zero which implies that the increase in v_C is finished.

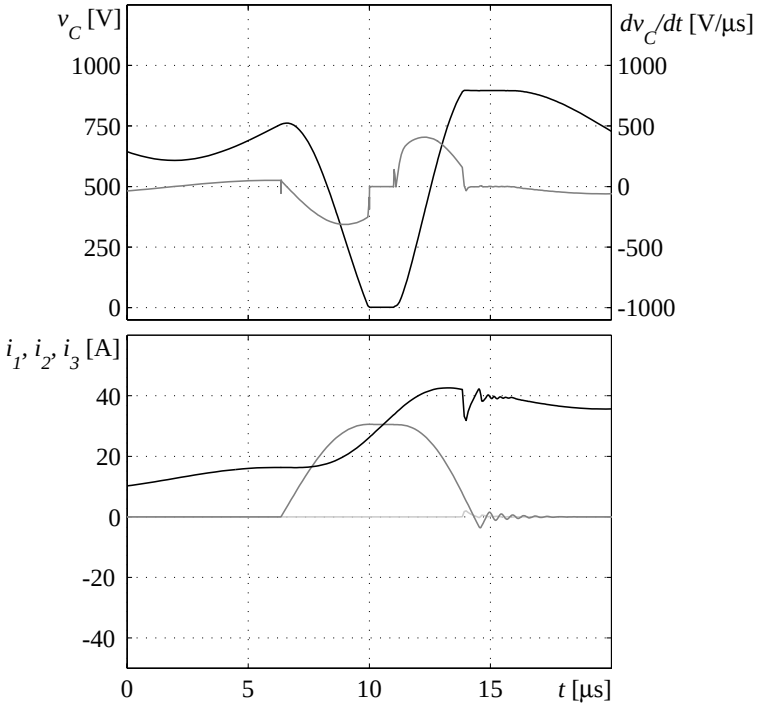


Figure 5.3 Resonant link waveforms at an output current increase corresponding to the rated maximum value. The waveforms shown are resonant link voltage v_C (top, black) and its time derivative (top, grey) and the resonant currents, i_1 (bottom, black), i_2 (bottom, dark grey) and i_3 (bottom, light grey).

There are mainly two reasons why clamping still occurs in Figure 5.3. First, the battery current ripple, due to the switched converter output

voltage, gives a maximum resonant link output current increase lower than the average battery current. Second, it was assumed in the derivation of the design expressions that the resonant cycle starts at steady state conditions, i.e. without oscillation between L_1 and C. As seen in Figure 5.3, v_C is increasing immediately before the resonant cycle is started implying a positive capacitor current i_C. This also implies that i_1 is higher than the resonant link output current i_o, which causes i_1 to be higher than needed at the end of the resonant cycle, thus clamping occurs. The positive initial resonant capacitor current i_C also results in that more energy is being transferred to L_2 since i_1 is larger than i_o, thereby counteracting the discharge of C. Therefore, the peak value of i_2 becomes somewhat higher than the value specified for the design constraint (3.64).

Figure 5.4 shows the resonant link waveforms at turn-off of the upper IGBT of the battery side converter, when the battery charger is operated at nominal load, i.e. maximum decrease of the resonant DC link output current i_o.

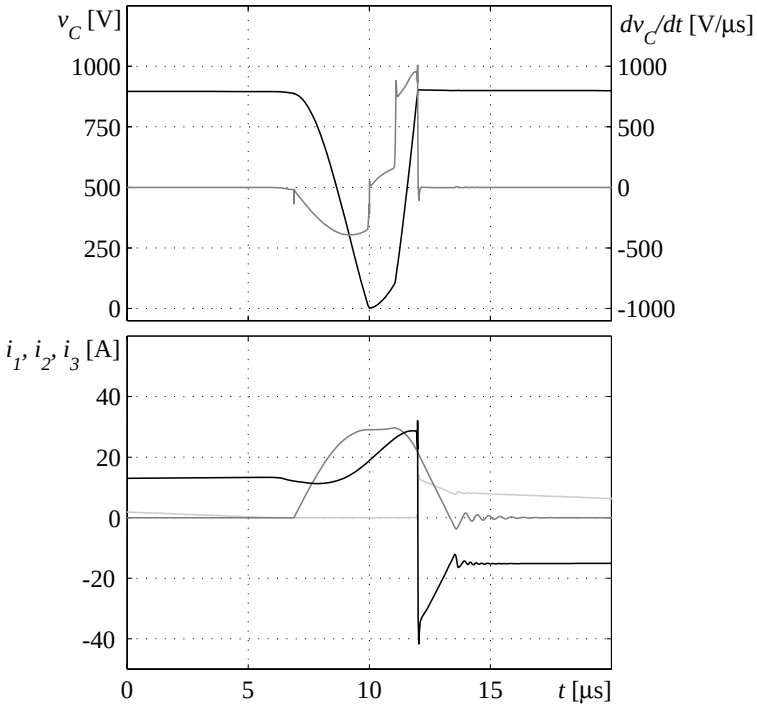


Figure 5.4 Resonant link waveforms at an output current decrease corresponding to the rated maximum value. The waveforms shown are resonant link voltage v_C (top, black) and its time derivative (top, grey) and the resonant currents, i_1 (bottom, black), i_2 (bottom, dark grey) and i_3 (bottom, light grey).

In Figure 5.4 above, it is seen that the resonant link voltage time derivative is approximately 1000 V/μs, which was the maximum value specified for the design constraint (3.63). Note that a larger output current decrease, which could result if several half bridges of the battery charger change switch state at the same resonant cycle, gives an even higher resonant link voltage time derivative. Also note that for these simulations, the duration of the zero voltage interval is kept constant at 1 μs independent of the resonant cycle.

From Figure 5.3 and Figure 5.4, it is concluded that the design expressions gives the desired behaviour of the resonant circuit. However, some important measures are not covered by the design expressions, for example the duration of the resonant cycle including the clamping interval. This is a severe drawback, since the maximum switching frequency obtainable is strongly affected.

The collector current and collector-emitter voltage at turn-off of the quasi resonant DC link switch S_1, for the cases shown in Figure 5.3 and Figure 5.4, are shown in Figure 5.5. The corresponding waveforms for S_2 looks exactly the same since the transistors are identical in the simulation model. In reality, there are parameter deviations between S_1 and S_2, resulting in slightly different waveforms for the two transistors.

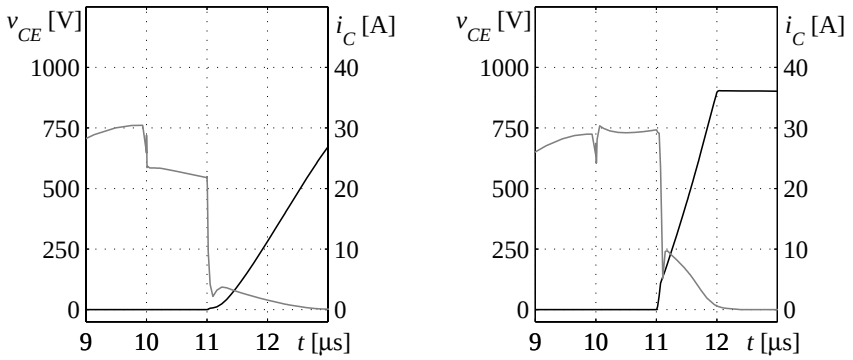


Figure 5.5 Turn-off waveforms for the resonant link IGBT S_1 when the resonant link output current is maximum increased (left) and maximum decreased (right). The quantities shown are the collector-emitter voltage (black) and collector current (grey).

Note the difference in the IGBT current tail for the two cases shown in Figure 5.5, which is due to the difference in the resonant link voltage derivative. The resonant current i_2 can partly commutate to the diodes D_1 and D_2 during the zero voltage interval, which is shown as a step decrease of the IGBT collector current in the leftmost part of Figure 5.5.

Figure 5.6 shows the collector-emitter voltage and the collector current for the upper IGBT of the battery side converter, for the resonant cycles shown in Figure 5.3 and Figure 5.4. Note the difference in the current tail bump at converter IGBT turn-off, compared to the case of the resonant link IGBT turn-off shown in Figure 5.5. The low magnitude of the current tail bump appearing for the converter IGBTs is probably due to the fact that internal recombination takes place during the zero voltage interval. This results in very low converter losses for the case where the passively clamped two switch quasi resonant DC link is used for the battery charger, which is shown later.

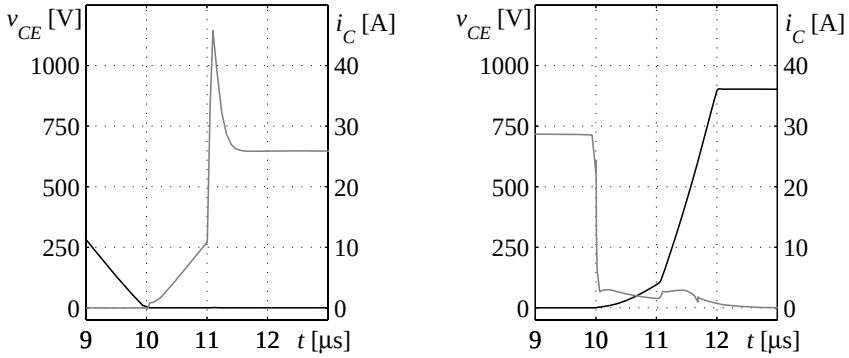


Figure 5.6 Switching waveforms for the upper IGBT of the battery side converter at rated power, turn-on (left) and turn-off (right). The quantities shown are the collector-emitter voltage (black) and collector current (grey).

In Figure 5.7, one of the line side phase currents and the battery current, for one period of the AC side fundamental, are shown for charging at rated power and battery voltage.

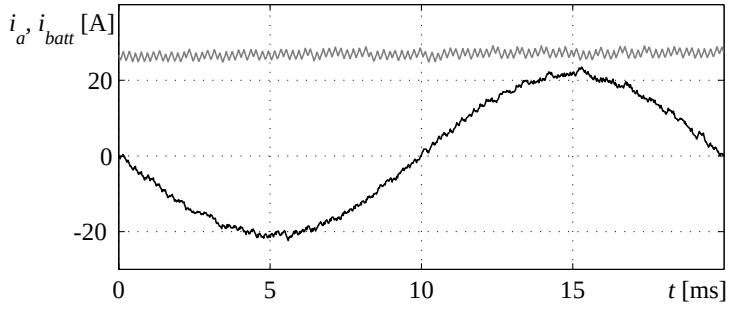


Figure 5.7 Line current in one phase (black) and battery current (grey). Both currents are defined as positive going out of the converters.

Note the presence of low order harmonics in the currents of Figure 5.7, which is due to the fact that the switching instants commanded by the modulator are delayed by the operation of the quasi resonant DC link. Furthermore, the length of this time delay varies due to the fact that the duration of the clamping interval is varying.

Efficiency

In order to compare the efficiency of the different quasi resonant DC links, the losses of the passive components are calculated as described in Chapter 4. The simulation software used, directly gives the instantaneous semiconductor losses which are integrated for one period of the fundamental frequency of the AC mains, to give the average losses.

The load condition considered corresponds to battery charging at rated power. However, since the battery charger current controllers have not reached steady state, the actual output power is likely to deviate slightly from the rated. In the simulation investigated here, the average power fed to the batteries was 10.104 kW. The losses of the quasi resonant link is listed in Table 5.5.

Table 5.5 Losses of the passively clamped two switch quasi resonant DC link.

Component	C	L_1/L_3	L_2	S_1/S_2	D_1/D_2	D_3
Losses (W)	1.3	30.5	9.8	78.0	3.2	8.6

The total losses for each of the blocks are listed in Table 5.6. Note that the output filters dissipate more than half the total losses.

Table 5.6 Losses for the entire battery charger at rated power.

Component/ Block	Line side		Battery side		DC link capacitor	Resonant circuit
	Converter	Filter	Converter	Filter		
Losses (W)	64.8	305.7	63.3	131.2	5.1	131.4

This gives a total efficiency of 93.5 %. The efficiency for the passively clamped quasi resonant circuit including the converters, equals 97.5 %, according to the simulations.

5.3 Simulation of the one switch passively clamped quasi resonant DC link

In this section passive component values for the one switch passively clamped DC link are determined from the expressions found in Chapter 3. Passive component parameter values for loss calculation are also given. Simulation results verifies the design expressions. The efficiency is calculated based on the loss parameters and the semiconductor losses given by the simulator.

Figure 5.8 shows the QRDCL block for simulation of the passively clamped one switch quasi resonant DC link, used in the simulation model in Figure 5.1. Note that the DC link capacitor is included in Figure 5.8.

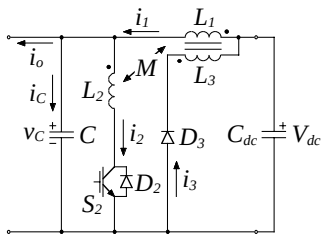


Figure 5.8 The passively clamped one switch quasi resonant DC link used in the simulation, including the DC link capacitor.

Simulation model and parameters

For the one switch passively clamped quasi resonant DC link shown in Figure 5.8, the resonant link voltage v_C has to be measured to detect both zero voltage and clamping, as for the previous circuit. Furthermore, the resonant current i_2 also has to be measured in order to detect its zero crossing during the zero voltage interval. When the zero crossing occurs, S_2 should be turned off by setting its gate-emitter voltage negative, since i_2 commutates to the freewheeling diode D_2. This is referred to as natural commutation and is favourable since no current tail appears for the resonant link IGBT S_2.

The design expressions determined in Section 3.2, i.e. (3.137), (3.138) and (3.139), are used to calculate appropriate passive component values based on the assumption that the magnetic coupling factor between the resonant inductors L_1 and L_2 is 0.9. The passive component values selected for the simulation model are thus given by

$$\begin{cases} L_1 = 64.0\ \mu\text{H} \\ L_2 = 17.64\ \mu\text{H} \\ L_3 = 1600\ \mu\text{H} \\ C = 165.0\ \text{nF} \end{cases} \tag{5.4}$$

Note that these passive component values are calculated for a maximum current step corresponding to a rated battery current ten percent higher than the specified. This is done to partly compensate for the reverse recovery current of the resonant link diode D_2, even though not necessary for reliable operation which is further discussed later on in this section.

The inductive components modelled for the simulation are designed according to Table 5.7. Also for this resonant circuit, the magnetic coupling factor of the clamping transformer, i.e. L_1/L_3, is assumed to be perfect. Still, no precautions are made in the design of the simulation model clamping transformer to fulfil this. The same is also true for the magnetic coupling factor between L_1 and L_2, i.e. it is assumed that it equals 0.9 though not considered from a design point of view.

Table 5.7 Resonant link inductor specifications used in the simulations.

Inductor	Core	A_L (nH/N^2)	N (turns)	R_{Cu} (mΩ)	R_{th} (°C/W)
$L_1/L_2/L_3$	2×T520-2	40.0	40/21/200	20.2/10.6/572.7	1.11

The resonant capacitor C is modelled by 11 parallel 15 nF capacitors with loss parameters approximated from the Rifa PHE 428 series, given in Section 5.2. Note that the rather high number of capacitors used here is needed primarily to limit the temperature rise and secondarily to adjust the total capacitance.

The resonant link IGBT S_2 is modelled as five IRGPH50K IGBTs connected in parallel. Each IGBT is equipped with a 5.0 Ω gate resistor. The diode D_2 is modelled by nine parallel diodes of type MR10150. As for the two switch counterpart, the clamping diode D_3, also in this case consists of five series connected diodes of the same type.

Simulated waveforms and losses

Simulations are used to verify the design expressions given for the passively clamped one switch quasi resonant DC link. Also for this circuit the results are presented in three different time scales, in order to focus on different performance criteria.

First the quasi resonant DC link quantities, i.e. voltages and currents, of interest are investigated. Figure 5.9 shows the resonant link waveforms at turn-on of the upper IGBT of the battery side converter at rated current, i.e. maximum increase of the resonant link output current i_o.

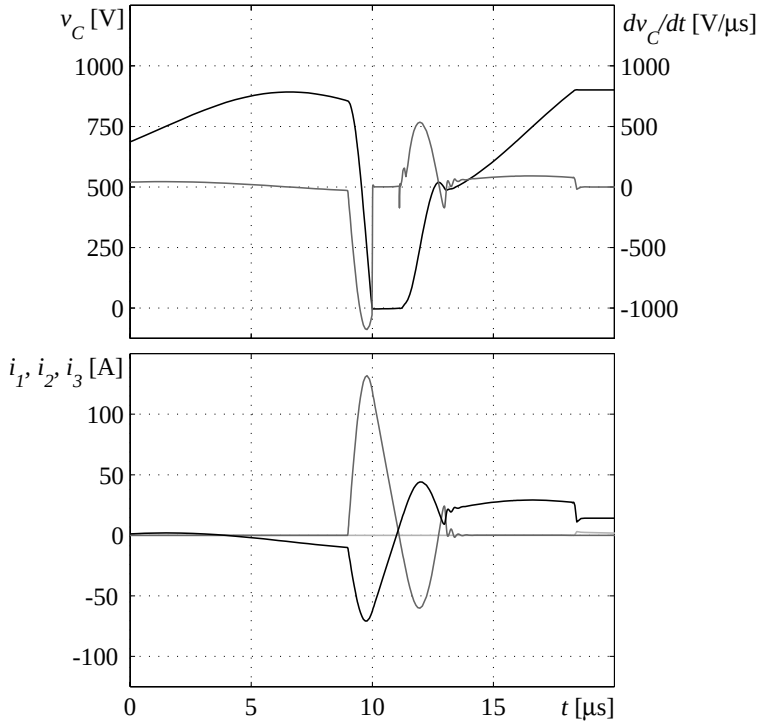


Figure 5.9 Waveforms for the passively clamped one switch quasi resonant DC link at an output current increase corresponding to the rated maximum. The waveforms shown are resonant link voltage v_C (top, black) and its time derivative (top, grey), and the resonant currents, i_1 (bottom, black), i_2 (bottom, dark grey) and i_3 (bottom, light grey).

From Figure 5.9 it is seen that the resonant link voltage, v_C, enters clamping. Still, the capacitor current becomes slightly negative due to reverse recovery of the diode D_2 appearing when i_2 crosses zero during the resonant link voltage ramp up interval. This also implies that i_1 is slightly lower than the output current fed to the converters. Clamping occurs due to the fact that v_C is lower than V_{dc} at this instant which implies that i_1 will continue to increase to become larger than the output current i_o. This phenomena is alleviated by the ten percent higher maximum output current increase used for the design. However, the dip in v_C when

i_2 crosses zero during the resonant link voltage ramp up interval is decreased by designing for a higher output current increase than expected.

In Figure 5.9 it is seen that the resonant link voltage derivative exceeds 1000 V/µs during the ramp down interval. This is due to the fact that the resonant cycle starts at a resonant link voltage close to the clamp level and at a slightly negative resonant link capacitor current.

Note the high peak value of the resonant inductor current i_2, shown in Figure 5.9. Also the peak value of i_1 is rather high. Together these two currents contribute to a resonant link capacitor peak current close to 200 A. The high peak current is the reason why 11 capacitors are needed to model the resonant link capacitor C, without unrealistic temperature rise appearing.

From Figure 5.9 it is also concluded that the maximum duration of the zero voltage interval is close to 1 µs, which is desired from the design constraints. Note that also for this circuit the duration of the resonant cycle is not considered by the design expressions, i.e. the maximum switching frequency obtainable is not controlled.

Figure 5.10 shows the resonant link waveforms at turn-off of the upper IGBT of the battery side converter, when the battery charger is operated at nominal load, i.e. maximum decrease of the resonant DC link output current i_o. Also in this case, the decrease equals the worst case only if none of the line side converter half bridges are switched during the resonant cycle. However, for this circuit the maximum time derivative of the resonant link voltage do not appear during the ramp up interval, i.e. the i_1 current step of Figure 5.10 do not correspond to the worst case anyway, which was also concluded in Section 3.2.

From Figure 5.10 it is also seen that the resonant link voltage during the ramp down interval is well below 1000 V/µs in this case, unlike the case shown in Figure 5.9. This is due to the fact that in Figure 5.10, the resonant cycle starts at a resonant link voltage level lower than the DC link voltage.

As seen in Figure 5.9 and Figure 5.10 the selected component values fulfil the design constraints. However, it is shown that the maximum voltage derivative is higher than the desired 1000 V/µs if the resonant cycle starts from a level exceeding the DC link voltage with a non-zero resonant capacitor current. This is due to the fact that the design expressions are derived based on the assumption that the resonant cycle starts from rest, i.e. with the resonant link voltage v_C equal to the DC link voltage V_{dc}.

Furthermore, it is also shown that reverse recovery of the diode D_2 influences the resonant link waveforms, especially at high output current increase. Here, this is solved by designing the resonant circuit for a ten percent higher output current increase than the actual.

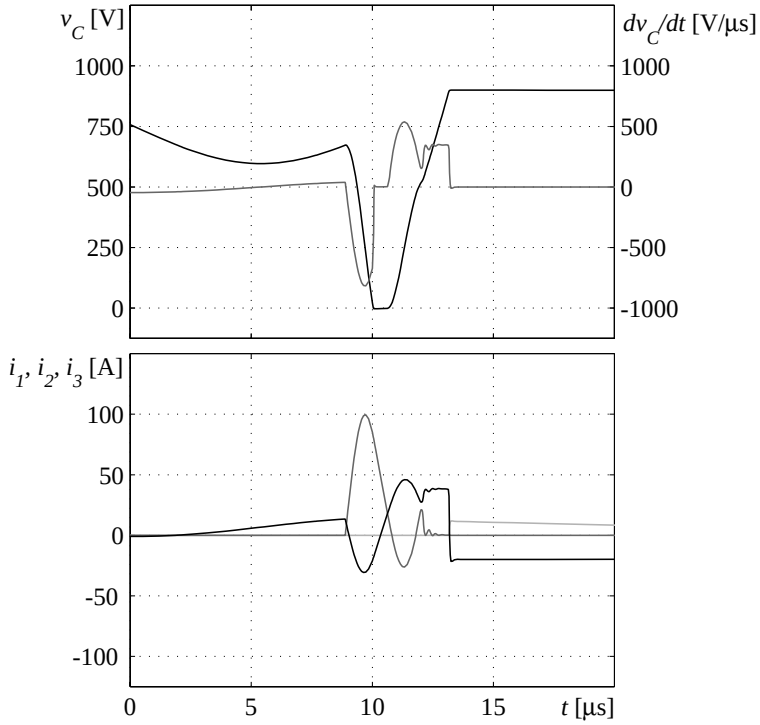


Figure 5.10 Resonant link waveforms at an output current decrease corresponding to the rated maximum value. The waveforms shown are resonant link voltage v_C (top, black) and its time derivative (top, grey) and the resonant currents, i_1 (bottom, black), i_2 (bottom, dark grey) and i_3 (bottom, light grey).

Figure 5.11 shows the collector-emitter voltage and the collector current for the upper IGBT of the battery side converter, for the resonant cycles shown in Figure 5.9 and Figure 5.10. Note the low current tail bump at converter IGBT turn-off.

The quasi resonant DC link transistor S_2, turns off naturally as discussed previously in this section. This means that no current tail appears, which is favourable since the switching losses becomes very low. The high peak value of the resonant current i_2 results in high conduction losses for S_2/D_2.

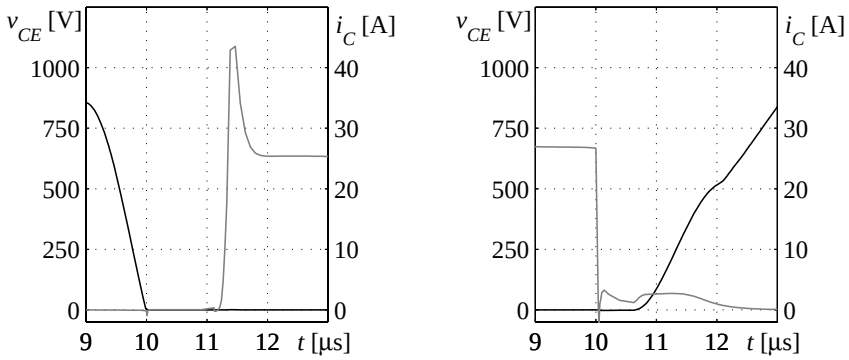


Figure 5.11 Switching waveforms for the upper IGBT of the battery side converter at rated power, turn-on (left) and turn-off (right). The quantities shown are the collector-emitter voltage (black) and collector current (grey).

In Figure 5.12, one of the line side phase currents and the battery current are shown for one period of the AC side fundamental, for charging at rated power and battery voltage. Compared to the corresponding currents for the previously discussed two switch counterpart, shown in Figure 5.7, it is clearly seen that the low frequency distortion is considerably lower. This is due to the fact that the average duration of the resonant cycle is shorter for the passively clamped one switch quasi resonant DC link, compared to the case for the two switch counterpart.

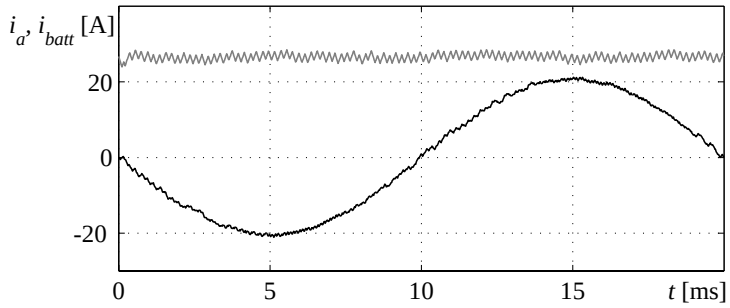


Figure 5.12 Line current in one phase (black) and battery current (grey). Both currents are defined as positive going out of the converters.

Efficiency

The average losses are calculated also for this circuit, based on simulation results. The load condition considered corresponds to battery charging at rated power. For a simulation time corresponding to the period of the

grid fundamental, i.e. 20 ms, the battery charger output power becomes 9.965 kW. The losses of the quasi resonant DC link is listed in Table 5.8.

Table 5.8 Losses of the passively clamped one switch quasi resonant DC link.

Component	C	$L_1/L_2/L_3$	S_2	D_2	D_3
Losses (W)	3.4	29.8	63.0	1.4	10.3

The total losses for each of the blocks are listed in Table 5.9. Table 5.9 gives a total efficiency equal to 94.0 %. The efficiency of the passively clamped one switch quasi resonant circuit including the converter is equal to 97.7 %, according to the simulations.

Table 5.9 Losses for the entire battery charger at rated power.

Component/ Block	Line side		Battery side		DC link capacitor	Resonant circuit
	Converter	Filter	Converter	Filter		
Losses (W)	64.0	273.1	58.8	127.9	7.6	107.9

5.4 Simulation of the parallel quasi resonant DC link

In this section appropriate passive component values are determined for the parallel quasi resonant DC link. The simulation model semiconductors and passive component parameters for loss calculation are given. Simulation results verifying the design expressions are shown and the battery charger efficiency is calculated.

In Figure 5.13, the QRDCL block for simulation of the parallel quasi resonant DC link, used in the simulation model in Figure 5.1, is shown.

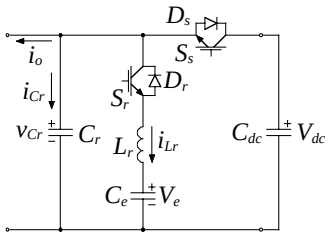


Figure 5.13 The parallel quasi resonant DC link used in the simulation, including the DC link capacitor.

Simulation model and parameters

For control of the parallel quasi resonant DC link the resonant link output current i_o must be measured, since the trip current levels are calculated based upon knowledge of i_o. The output current for each converter half bridge is measured (one of the output currents of the line side converter is actually calculated from the other two). Together with the actual switch state and the switch state to be set, the present and the next level of the output current, i.e. I_{o1} and I_{o2}, are calculated. Based on these output current levels, the trip currents are determined.

Note that also the resonant inductor current i_{Lr} has to be measured to detect the trip current crossings and to detect when the resonant link switch S_r can be turned off by means of an appropriate gate signal, which is after i_{Lr} has commutated from S_r to D_r.

The resonant link voltage v_{Cr} also has to be measured, since the converter half bridges should be shorted by applying appropriate gate signals to all the converter IGBTs when the zero voltage interval is entered. The resonant link voltage has to be measured also to detect the end of the resonant link voltage ramp up interval, where S_s should be turned on again.

Also, the energy storage capacitor voltage, V_e, is measured since it has to be controlled for proper operation of the parallel quasi resonant link.

This circuit has three passive component values to be selected, L_r, C_r and C_e, see Figure 5.13. The design expressions for this circuit determined in Section 3.3, i.e. (3.187) and (3.191), gives appropriate values for L_r and C_r. The energy storage capacitor value is selected from simulations. For the implementation in [41], the capacitance of C_e is selected as 700 times higher than the one of C_r. In [41], this means an energy storage capacitor C_e, of 100 μF which is a suitable value also here.

The passive component values selected for the simulation model of the parallel quasi resonant DC link are selected according to

$$\begin{cases} L_r = 17.09\ \mu\text{H} \\ C_r = 33\ \text{nF} \\ C_e = 94\ \mu\text{F} \end{cases} \tag{5.5}$$

The simulation model resonant link inductor L_r, is designed according to Table 5.10.

Table 5.10 Resonant link inductor specifications used in the simulations.

Inductor	Core	A_L (nH/N^2)	N (turns)	R_{Cu} (mΩ)	R_{th} (°C/W)
L_r	T200-2B	21.8	28	13.4	6.56

The resonant link capacitor C_r is considered as being selected from the Rifa PHE 428 series. The loss parameters for such capacitors are given in Section 5.2.

The energy storage capacitor C_e is modelled as two parallel polypropylene capacitors, MSR-D-47-45 manufactured by Icar. The relevant data for the resulting, i.e. parallel equivalent, capacitor is listed in Table 5.11 below.

Table 5.11 Specification of the energy storage capacitor used in the simulations.

Capacitor	Type	C (μF)	$\tan\delta_0$	R_s (mΩ)	L_{ESL} (nH)	R_{th} (°C /W)
C_e	2×MSR-D47-45	94	0.0002	0.92	60	3.2

The simulation model resonant link IGBTs, S_r and S_s, actually consist of three parallel IGBTs of type IRGPH50K each. As previously mentioned, each such IGBT is equipped with a 5.0 Ω gate resistor. The diodes D_r and D_s are modelled by six parallel connected Harris MR10150 diodes each.

The behaviour of the parallel quasi resonant DC link is simulated in the battery charger application in order to verify the design expressions given, i.e. (3.187) and (3.191).

However, it is somewhat complicated to validate the simulation results by means of waveforms for the circuits relying on energy stored in a capacitor, since the energy storage capacitor voltage is controlled which affects the resonant link waveforms. Still it is important to simulate the entire circuit, i.e. without replacing the energy storage capacitor with a constant voltage source, since the control action needed do indeed affect the efficiency obtained.

Figure 5.14 shows the resonant link waveforms at turn-on of the upper IGBT of the battery side converter at rated current, i.e. maximum increase of the resonant link output current i_o.

In Figure 5.14 it is seen both that the duration of the zero link voltage interval is longer than desired and that the resonant link voltage derivative is well below the maximum allowed.

The reason why the duration of the zero voltage interval is longer than expected from the design expressions, is that it is maintained longer on

purpose, in order to decrease the energy storage capacitor voltage V_e, i.e. due to control action. The maximum resonant link voltage derivative is only experienced for the minimum output current I_{o2}, which is not achieved for the case shown in Figure 5.14.

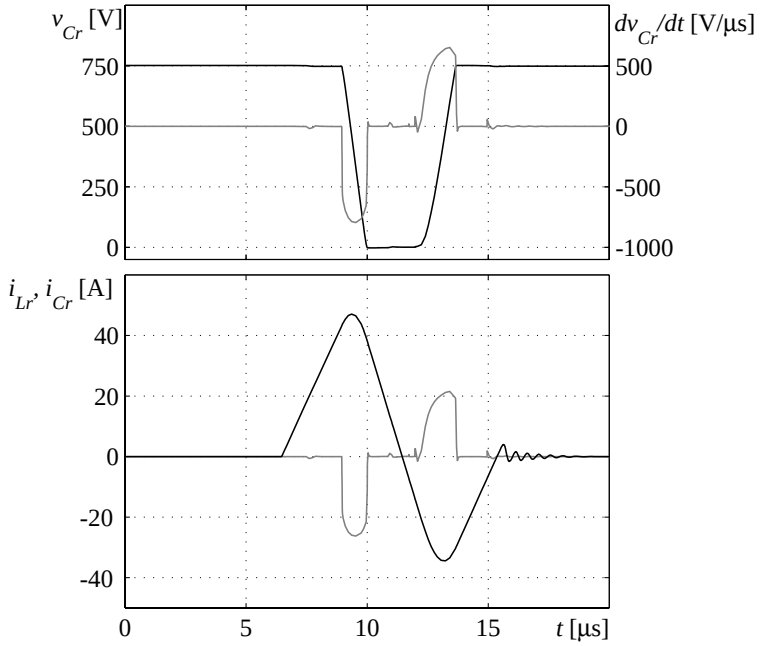


Figure 5.14 Resonant link waveforms at an output current increase corresponding to the rated maximum value. The waveforms shown are resonant link voltage v_{Cr} (top, black) and its time derivative (top, grey) and the resonant currents, i_{Lr} (bottom, black) and i_{Cr} (bottom, grey).

Figure 5.15 shows the resonant link waveforms at turn-off of the upper IGBT of the battery side converter, when the battery charger is operated at nominal load, i.e. maximum decrease of the resonant DC link output current i_o.

In Figure 5.15 the duration of the zero voltage interval is shorter than the one shown in Figure 5.14, due to the fact that the current decrease at its most. Still, it is longer than predicted from the analysis in Section 3.3, due to the control actions made to decrease the energy storage capacitor voltage V_e. As shown in Figure 5.15, the resonant link voltage derivative is well below the specified maximum also in this case.

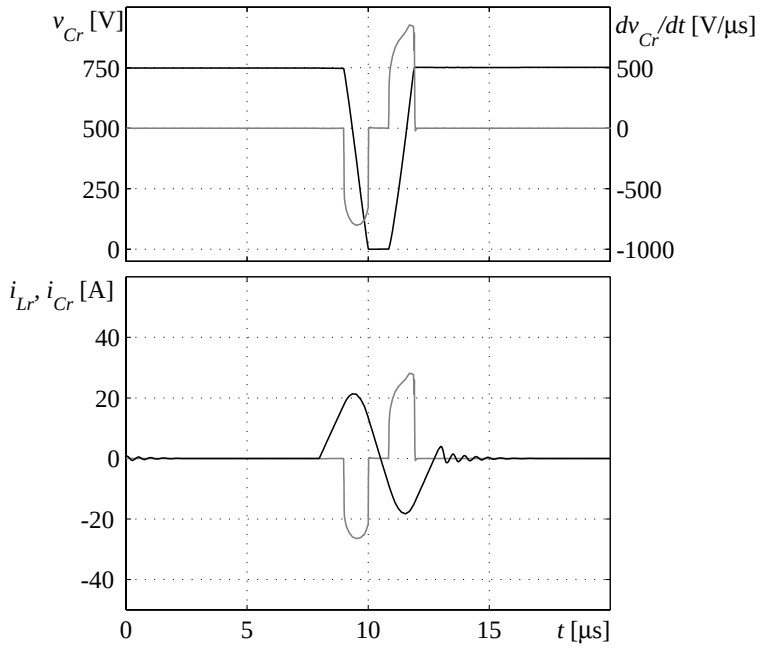


Figure 5.15 Resonant link waveforms at an output current decrease corresponding to the rated maximum value. The waveforms shown are resonant link voltage v_{Cr} (top, black) and its time derivative (top, grey) and the resonant currents, i_{Lr} (bottom, black) and i_{Cr} (bottom, grey).

The reason why the maximum allowed resonant link voltage derivative is not appearing for the cases shown in Figure 5.14 and Figure 5.15, is that the circuit is designed for a minimum output current equal to discharging of the battery charger at rated current.

In Chapter 1, it is stated that the battery charger should be able to operate as an electronic gasturbine, i.e. to support the power grid with peak power during periods of high power demand. This means that the battery could be discharged with a current corresponding to the rated, which for this circuit becomes the limiting case by means of maximum resonant link voltage derivative.

The resonant cycle time is not considered for this circuit either. However, the cycle time for this quasi resonant DC link is the shortest of the four investigated.

The collector current and collector-emitter voltage at turn-off of the quasi resonant DC link IGBTs, S_s and S_r, for the case shown in Figure 5.15 i.e.

turn-off of the upper IGBT of the battery side converter, are shown in Figure 5.16.

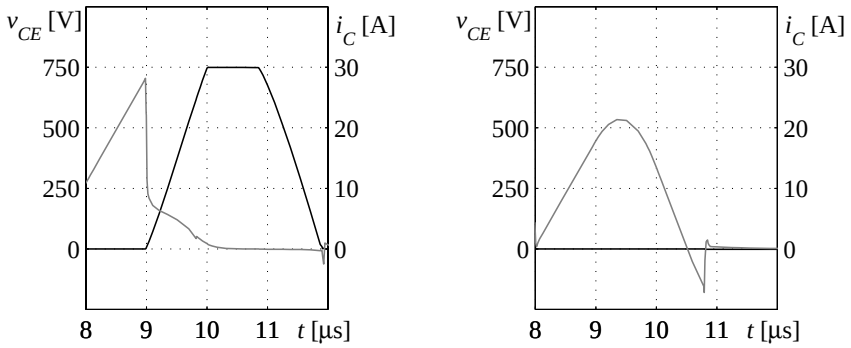


Figure 5.16 Turn-off waveforms for the resonant link IGBTs S_s (left) and S_r (right) when the resonant link output current is decreased by its maximum. The quantities shown are the collector-emitter voltage (black) and collector current (grey).

Note the difference in the current tail for the two IGBTs shown in Figure 5.16. The series IGBT S_s turns off at a typical zero voltage condition, resulting in the appearance of a long collector current tail. The resonant link IGBT S_r turns off naturally by commutation to its freewheeling diode D_r, hence no current tail appears.

Figure 5.17 shows the collector-emitter voltage and the collector current for the upper IGBT of the battery side converter, for the resonant cycles shown in Figure 5.14 and Figure 5.15. Note the difference in the current tail at turn-off of the converter IGBT, compared to the resonant link IGBT, S_r, turn-off shown in Figure 5.16.

The pronounced collector current tail appearing at converter IGBT turn-off, gives a considerable contribution to the converter losses when the parallel quasi resonant DC link is used for the battery charger. This is seen later when the efficiency is investigated.

The reason why this current tail appears for this resonant link but not for the passively clamped previously investigated, is that for the parallel quasi resonant circuit, it is the turn-off of one IGBT of each half bridge that initiates the resonant link voltage ramp up interval. Thus, no converter IGBT internal recombination takes place prior to the ramp up interval.

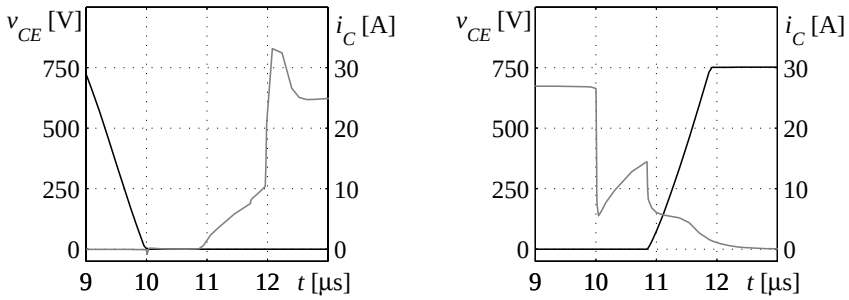


Figure 5.17 Switching waveforms for the upper IGBT of the battery side converter at rated power, turn-on (left) and turn-off (right). The quantities shown are the collector-emitter voltage (black) and collector current (grey).

In Figure 5.18, one of the line side phase currents and the battery current, for one period of the AC side fundamental, are shown for charging at rated power and battery voltage.

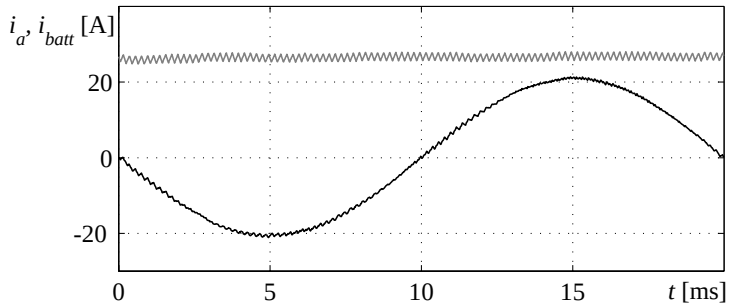


Figure 5.18 Line current in one phase (black) and battery current (grey). Both currents are defined as positive going out of the converters.

Note the small amount of low order harmonics appearing in the currents shown in Figure 5.18. This is due to the fact that the switching instants commanded by the modulator are only slightly delayed by the operation of this quasi resonant DC link, due to the rather short duration of the resonant cycle.

Efficiency

The passive component losses for the battery charger using the parallel quasi resonant DC link are calculated as described in Chapter 4. The instantaneous semiconductor losses are directly given by the simulation software used, and the average losses are calculated by integration. The load condition considered corresponds to battery charging close to rated

power. In the simulation the average power fed to the batteries becomes 9.960 kW. The losses of the quasi resonant link are listed in Table 5.12.

Table 5.12 Losses of the parallel quasi resonant DC link.

Component	C_e	C_r	L_r	S_r	S_s	D_r	D_s
Losses (W)	0.1	1.1	6.6	9.2	60.3	2.6	9.2

The total losses for each of the blocks are listed in Table 5.13. Note that the output filters dissipate more than half the total losses.

Table 5.13 Losses for the entire battery charger at rated power.

Component/ Block	Line side		Battery side		DC link capacitor	Resonant circuit
	Converter	Filter	Converter	Filter		
Losses (W)	123.7	276.0	77.4	126.0	3.4	85.6

This gives a total efficiency of 93.5 %. The simulated efficiency for the parallel quasi resonant DC link including both the converters is equal to 97.2 %.

5.5 Simulation of the actively clamped quasi resonant DC link

The simulation model of the actively clamped quasi resonant DC link used for the battery charger considered, is discussed and suitable passive component simulation model parameter values for loss calculation are given. Simulation results verifying the design expressions are shown and the efficiency is calculated.

Figure 5.19 shows the QRDCL block for simulation of the actively clamped quasi resonant DC link, used in the battery charger simulation model in Figure 5.1.

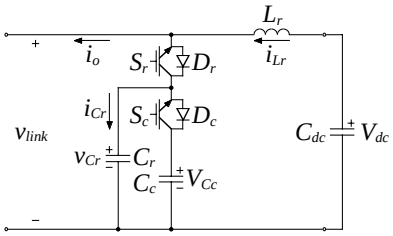


Figure 5.19 The actively clamped quasi resonant DC link used in the simulation, including the DC link capacitor.

Simulation model and parameters

For the operation of the actively clamped quasi resonant DC link, by means of simulation, the similar quantities as for the parallel quasi resonant DC link have to be measured. In an implementation, the trip current level should not be calculated as being an IGBT collector current due to practical problems. Instead, both the trip currents used in the simulation are expressed as resonant inductor currents, i_{Lr}. This implies that this current has to be measured and also that the resonant output current must be estimated from the line and battery side currents and modulator command signals, as discussed in Section 5.4. However, this adds no further complexity to the resonant link control, since this anyway has to be done for proper selection of the instant to initiate the ramp up interval, i.e. the second trip current level and its crossing.

The resonant link voltage v_{link} has to be measured, since the converter half bridges should be shorted by applying appropriate gate signals to all the converter IGBTs when the zero voltage interval is entered. The resonant link IGBT S_r should be turned off when the zero voltage interval is entered.

The clamp capacitor voltage V_{Cc} is measured, since it has to be controlled to obtain the desired clamping voltage for the actively clamped quasi resonant DC link.

The resonant circuit has three passive component values to be selected, L_r, C_r and C_c. The design expressions for this circuit determined in Section 3.4, i.e. (3.240) and (3.244), gives appropriate values for L_r and C_r. The clamp capacitor value is selected from simulations. The passive component values used in the simulations are

$$\begin{cases} L_r = 14.4\ \mu\text{H} \\ C_r = 54.0\ \text{nF} \\ C_c = 94.0\ \mu\text{F} \end{cases} \tag{5.6}$$

Note that the minimum current margins I_{m1} and I_{m2}, needed for safe operation, are assumed to equal 5 A each in the calculation of the passive component values. These minimum current margins are also used in the simulation model.

The resonant inductor is designed according to Table 5.14.

Table 5.14 Resonant link inductor specification used in the simulations.

Inductor	Core	A_L (nH/N^2)	N (turns)	R_{Cu} (mΩ)	R_{th} (°C/W)
L_r	T400-2D	36.0	20	3.9	2.12

The simulation model resonant capacitor C_r actually consists of four parallel connected capacitors, two 12 nF and two 15 nF, with loss parameters selected from the Rifa PHE 428 series, see Section 5.2.

The clamp capacitor is modelled the same way as C_e was for the parallel quasi resonant DC link, i.e. as two parallel connected Icar MSR-D-47-45, see Section 5.4.

The resonant link IGBTs, S_c and S_r, shown in Figure 5.19, actually consist of three parallel connected IGBTs of type IRGPH50K each. The diodes D_c and D_r are modelled by six discrete, parallel connected diodes of type Harris MR10150 each.

Simulated waveforms and losses

For the battery charger utilising the actively clamped quasi resonant DC link, one period of the fundamental grid frequency is simulated in order to calculate the average losses, as for the previously investigated quasi resonant links.

First, the quasi resonant DC link quantities, i.e. voltages and currents, of interest are investigated. Figure 5.20 shows the resonant link waveforms at turn-on of the upper IGBT of the battery side converter at rated current, i.e. maximum increase of the resonant link output current i_o.

In Figure 5.20 it is seen that the duration of the zero voltage interval is longer than was desired at the design stage. This is due to the fact that control actions are made to increase the clamp voltage. The clamp voltage is increased by supplying excess energy to the clamp capacitor at the clamping interval. To do this, the zero voltage interval is maintained somewhat longer than needed by means of short term operation of the resonant circuit. This means that excess energy is stored in the resonant inductor L_r during the zero voltage interval. This energy is then transferred to the clamp capacitor C_c at the clamping interval.

However, this also means that a higher current than expected is supplied to the resonant link capacitor C_r during the ramp up interval, causing the resonant link voltage derivative to be higher than desired, which is also seen in Figure 5.20.

Note that in both Figure 5.20 and Figure 5.21 the resonant link voltage derivative is not explicitly shown but instead the resonant capacitor voltage v_{Cr} derivative. This is done in order to avoid showing the high derivatives, appearing in the resonant link voltage v_{link} at the start of the energy storage interval and at the end of the clamping interval. These high voltage derivatives can not be controlled by proper selection of the resonant link passive components.

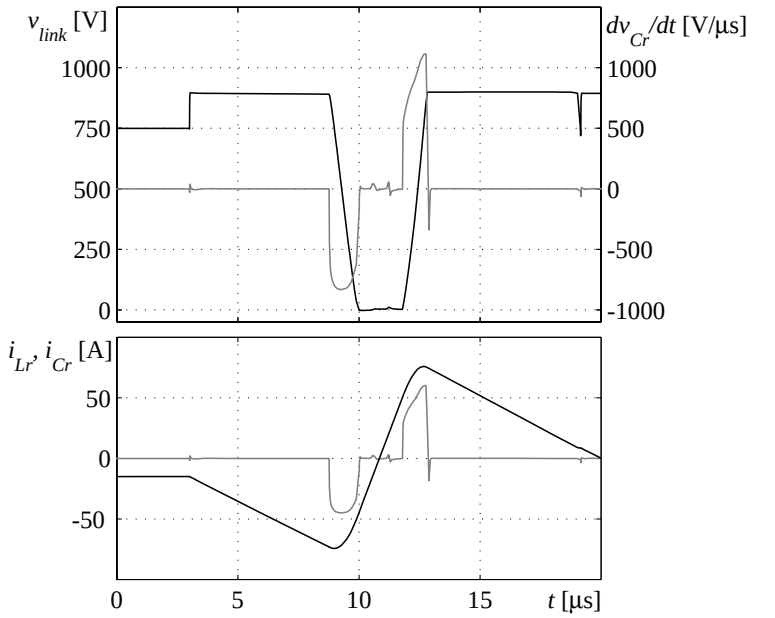


Figure 5.20 Resonant link waveforms at an output current increase corresponding to the rated maximum value. The waveforms shown are resonant link voltage v_{link} (top, black) and the time derivative of the resonant capacitor voltage v_{Cr} (top, grey), and the resonant currents, i_{Lr} (bottom, black) and i_{Cr} (bottom, grey).

The corresponding waveforms at rated resonant link output current decrease, i.e. turn-off of the upper battery side converter IGBT when charging at rated power, are shown in Figure 5.21. The same problems as seen in Figure 5.20 also occurs here. The duration of the zero voltage interval and the resonant link voltage rising edge derivative both exceeds their desired values. The reasons are the same as discussed for turn-on of the upper battery side converter IGBT, even though the poor result is not as obvious as in Figure 5.20.

One way to avoid the high resonant link voltage derivative, caused by clamp voltage control action, is to include the boost current in the

selection of the passive components. In the design expressions given in Chapter 3, this is done by specifying the maximum boost current as a current margin and include it in the design. It is however important to only include this variable boost current when the voltage derivative is calculated and not for the duration of the zero voltage interval. This is due to the fact that the boost current commanded by the clamp voltage controller can be lower than its maximum, thus giving a shorter duration of the zero voltage interval than expected.

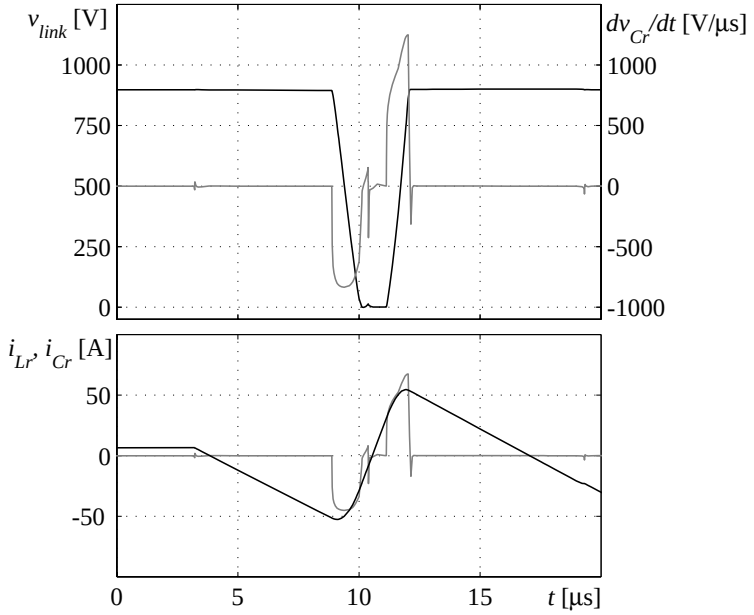


Figure 5.21 Resonant link waveforms at an output current decrease corresponding to the rated maximum value. The waveforms shown are resonant link voltage v_{link} (top, black) and the time derivative of the resonant capacitor voltage v_{Cr} (top, grey), and the resonant currents, i_{Lr} (bottom, black) and i_{Cr} (bottom, grey).

The turn-off waveforms for the resonant circuit IGBTs are left out here, since they are similar to the ones discussed for the parallel quasi resonant DC link circuit. The clamp circuit IGBT S_c turn-off waveform in essence resembles the one given for S_s in Figure 5.16, i.e. a collector current tail bump appears since the IGBT turns off under zero voltage conditions. The resonant circuit IGBT, S_r, turns-off naturally since the resonant inductor current i_{Lr} commutates to the converter freewheeling diodes when the zero voltage interval is entered. Hence, the turn-off waveforms for the IGBT denoted S_r for the actively clamped quasi resonant circuit,

closely resembles the turn-off waveforms given in Figure 5.16 for the parallel quasi resonant circuit IGBT S_r.

Figure 5.22 shows the collector-emitter voltage and the collector current for the upper IGBT of the battery side converter, for the resonant cycles shown in Figure 5.20 and Figure 5.21. Note the converter IGBT collector current tail at turn-off. This implies that also for the battery charger equipped with the actively clamped quasi resonant DC link, the converter losses will be high compared to the cases when the passively clamped quasi resonant DC links are used.

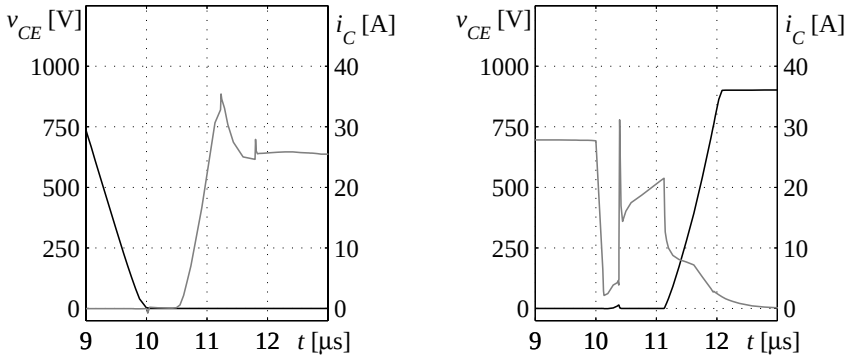


Figure 5.22 Switching waveforms for the upper IGBT of the battery side converter at rated power, turn-on (left) and turn-off (right). The quantities shown are the collector-emitter voltage (black) and collector current (grey).

In Figure 5.23, one of the line side phase currents and the battery current, for one period of the AC side fundamental, are shown for charging at rated power and battery voltage.

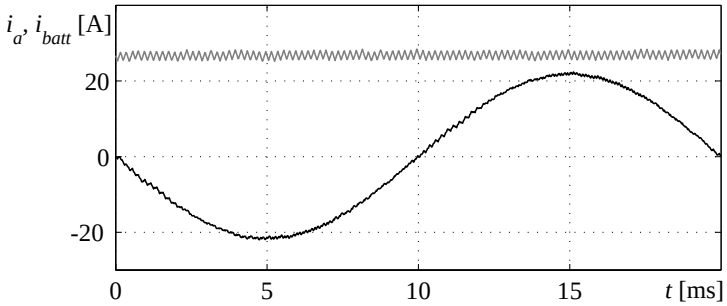


Figure 5.23 Line current in one phase (black) and battery current (grey). Both currents are defined as positive going out of the converters.

Only a small amount of low order harmonics appears in the currents shown in Figure 5.23, even though the actively clamped quasi resonant circuit is not as fast as the parallel, previously investigated.

Efficiency

As for the other quasi resonant DC links investigated, the losses for a battery charger using the actively clamped resonant circuit, are calculated. The calculations are based on simulation data for one period of the fundamental frequency of the AC mains, to give the average losses. Also for this charger the load condition considered is battery charging at rated power. In this case the average power fed to the batteries was 10.027 kW. The losses of the actively clamped quasi resonant DC link are listed in Table 5.15.

Table 5.15 Losses of the actively clamped quasi resonant DC link.

Component	C_c	C_r	L_r	S_r	S_c	D_r	D_c
Losses (W)	0.5	1.4	20.2	21.0	125.0	10.0	7.6

The total losses for each of the blocks are listed in Table 5.16. Note that in this case the output filters dissipates less than half the total losses.

Table 5.16 Losses for the battery charger at rated power.

Component/ Block	Line side		Battery side		DC link capacitor	Resonant circuit
	Converter	Filter	Converter	Filter		
Losses (W)	159.2	303.1	94.0	130.0	14.4	185.9

This gives a total efficiency equal to 91.9 %. The efficiency for the passively clamped quasi resonant circuit including the converter is equal to 95.7 %, according to the simulations.

5.6 Simulation conclusions

One of the investigated quasi resonant DC link battery chargers should be implemented for further analysis. Also, a hard switched battery charger should be implemented to compare the simulated efficiency with the measured. In this section the simulated losses and efficiency for a 10 kW hard switched battery charger is first given, and then the choice of quasi resonant circuit selected for implementation is discussed. The actual design and implementation of both the hard and soft switched battery chargers are presented in Chapter 6.

Losses and efficiency of the hard switched battery charger

The hard switched battery charger is simulated under the same conditions as the quasi resonant DC link chargers are, i.e. battery charging at rated power for one period of the line side fundamental. The losses for the hard switched battery charger at a charging power of 10.044 kW, are given in Table 5.17.

Table 5.17 Losses of the hard switched battery charger at rated power.

Component/ Block	Line side		Battery side		DC link capacitor	Snubber capacitors
	Converter	Filter	Converter	Filter		
Losses (W)	90.0	328.7	101.1	132.7	4.8	≈0

The charging power and the losses listed above gives an overall efficiency for the battery charger of 93.8 %. The converter efficiency is 98.1 %.

Note that for the simulated hard switched battery charger, the gate resistor values are selected 10 times higher than for the quasi resonant chargers, to partly decrease the maximum converter output voltage time derivative. Still, the maximum obtained derivative is as high as 10000 V/μs, in the simulation model. The losses are however only slightly affected by the high gate resistor values used in the simulation, which is probably due to the fact that the dominating part of the switching losses is due to IGBT collector current tailing. Note that the IGBT collector current tail is only slightly affected by the gate resistor value.

Table 5.18 shows the simulated efficiency for the different battery chargers investigated.

Table 5.18 Simulated converter efficiency and total efficiency of the different battery chargers, operating at rated power.

Battery charger	Converter efficiency	Total efficiency
Passively clamped two switch quasi resonant DC link	97.5 %	93.5 %
Passively clamped one switch quasi resonant DC link	97.7 %	94.0 %
Parallel quasi resonant DC link	97.2 %	93.5 %
Actively clamped quasi resonant DC link	95.7 %	91.9 %
Hard Switched	98.1 %	93.8 %

An important conclusion drawn from the simulations of the different battery chargers, is that the maximum converter efficiency is obtained for the hard switched topology, which is shown in Table 5.18. However, resonant converters are in most cases used for higher switching frequencies than the 4.95 kHz used here, which means that the converter switching losses for the hard switched charger would be higher in such a case. Still, several of the quasi resonant DC links investigated do not allow higher switching frequency, without compromising the maximum output voltage derivative, the duration of the zero voltage interval or the output current low order harmonics.

The results of this chapter, by means of simulated efficiency, should be used carefully. This is due to the fact that the battery chargers do not operate at steady state conditions, in the simulations. This is clearly seen in the tables containing the losses of the different battery chargers. In fact, the DC link voltage drops a few volts for all the circuits during the simulations, which is due to the fact that the integral parts of the current controllers, see Appendix B, do not settle for such a short simulation time. One way to circumvent this problem, is to use the calculated losses of a previous simulation to calculate initial conditions for the integral parts. Even though this method was used, it was not iterated the number of times needed for the integral parts to settle, mainly due to the long simulation time required.

However, a DC link capacitor voltage decrease of 2 V corresponds to an average power of less than 200 W, fed from the DC link capacitors to the rest of the battery charger. This power is fed from the grid when steady state conditions are established. This means that this power should be fed through the line side filter and converter, which implies that the losses of these parts would increase. However, the additional power constitutes only a minor part of the total power, fed via the line side. Furthermore, the battery charger and converter input power are calculated by adding the corresponding output power and the losses. This implies that the resonant link power losses are not affected, at least not to a large extent.

Therefore, the simulated efficiency is probably close to the one obtained for steady state conditions. Note that in the case of simulated converter efficiency it is only the line side converter losses that increases, due to the additional power. Still, it should be pointed out that the DC link voltage decrease is not equal in the simulations of the different battery chargers, but it only corresponds to a few volts even in the worst case.

Note that a similar comparison is made in [27]. In [27] the rated power is 5 kW and the DC link voltage is 375 V. Therefore, 600 V IGBTs are used

in this case. In [27] the efficiency of the hard switched battery charger becomes lower than the efficiency of several of the quasi resonant DC link equipped ones, even though the same resonant circuits as here are compared. The reason for this is that the hard switched battery charger is equipped with capacitive turn-off snubbers connected across each transistor, i.e. not hard switched. As discussed in Section 2.1 the capacitive turn-off snubber is not suitable in bridge applications since the IGBT collector current becomes very high at turn-on, which causes the low efficiency reported in [27].

Actually, snubbers are used also for the hard switched battery charger investigated here. However, in this case capacitive overvoltage snubbers, connected across each half bridge, are used. Such snubbers are intended to reduce the semiconductor overvoltage stress, appearing due to circuit stray inductance. This kind of snubber does not affect the semiconductor switching waveforms.

Selection of quasi resonant DC link for implementation

The passively clamped two switch quasi resonant DC link battery charger is selected for implementation. The reasons for selecting this circuit are the quite high efficiency together with the uncomplicated control needed for implementation. Uncomplicated control is important since several quasi resonant DC links relies upon high bandwidth measurements of resonant link voltage and resonant inductor currents, which is hard to achieve. Also, internal time delay of the IGBT drivers further complicates the controller implementation.

Another important reason for selecting the passively clamped two switch quasi resonant DC link battery charger is that also a hard switched version should be implemented. To circumvent differences between individual semiconductors used, it is favourable if the very same converter components can be used for both chargers implemented, by means of efficiency comparison.

However, there are also drawbacks associated with the passively clamped two switch quasi resonant DC link. The main problems occurs in the clamp circuit, where several diodes have to be series connected and a transformer with high magnetic coupling factor has to be designed. Another problem is the large amount of low order harmonics contained in the output currents, caused by the time delay introduced by the long resonant cycle time for this circuit.

6

Implementation

In this chapter, the implementation and evaluation of the passively clamped two switch quasi resonant DC link battery charger, are presented. The ratings and switching frequency of the implemented battery charger are the same as for the ones investigated in Chapter 5. The implementation of the power electronic main circuit is presented in steps discussing each component used. A lot of emphasis is put on minimising the effects due to non-ideal device behaviour. One section describing the modulator used is also given. Finally, the quasi resonant DC link battery charger is tested and its efficiency compared to a hard switched counterpart. To overcome measurement deviations due to parameter variations both for the semiconductors and the passive components, the quasi resonant battery charger is altered to form a hard switched, instead of using two separate circuits for the comparison.

6.1 Power electronic main circuit

The battery charger main circuit is shown in Figure 6.1. The connection points for the clamp transformer, *a'* and *a"*, are marked in Figure 6.1. To perform measurements on the hard switched battery charger, the clamp transformer is disconnected at the connection points, *a'* and *a"*, which instead are connected directly to each other.

Note that the output filters of the implemented battery charger are purely inductive, i.e. LCL-filters are not used for the evaluation. The reason for not using LCL-filters is discussed in the measurement section. The output filters used in the battery charger implementation are not designed especially for the application, and their loss characteristics are unknown. Therefore, loss measurements are made both on the battery charger including filters and on the battery charger itself. In order to determine to what extent the limited bandwidth of the power meter used affects the measurements, it is important to include the passive filters in the measurement of losses.

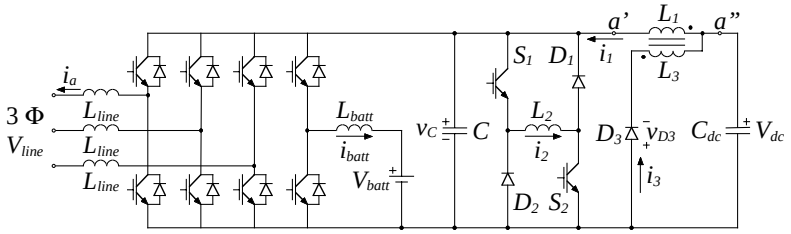


Figure 6.1 The main circuit of the implemented quasi resonant battery charger. To convert the charger to a hard switched, the clamp transformer is disconnected at the points *a'* and *a"*, and these points are connected directly to each other.

The DC link capacitor actually consists of four electrolytic capacitors, two series connected and two in parallel. Data on the DC link capacitor parameters for loss calculation are not available. Neither is the equivalent series inductance, L_{ESL}. The data available on the output filters and the DC link capacitor are listed below.

$$\begin{cases} L_{line} = 15.5 \text{ mH} \\ L_{batt} = 21.7 \text{ mH} \\ C_{dc} = 2.2 \text{ mF} \end{cases} \tag{6.1}$$

To estimate the efficiency of the implemented battery chargers, by means of simulation, the loss parameters used for the output filters and the DC link capacitor are the same as was given in Chapter 5.

Converter semiconductor devices

The converter semiconductors used in the simulations are considered not suitable for the implementation. The main reason is that in the simulations several semiconductors are connected in parallel to meet the constraint (2.1), which complicates the design. Instead IGBT modules consisting of an entire half bridge, i.e. two IGBTs and two freewheeling diodes, are used. The current ratings of these modules are selected in such a way that paralleling is not needed. By using modules, good mechanical and thermal design are also gained.

The modules selected for the battery charger converters are of the type SKM50GB123D manufactured by Semikron [68], which consists of 50 A, 1200V devices. However, at a silicon temperature of 125 °C, which is a suitable operating temperature, the rated current for the module is 40 A. The IGBT module rated current is thus slightly higher than needed for the line side converter of the battery charger, according to (2.1).

Drive circuits suitable for the modules selected are also manufactured by Semikron. For the battery charger the driver SKHI23/12 is chosen [68]. This is a 1200 V dual driver which means that it actually consists of two drivers, one for the upper and one for the lower IGBT of a half bridge. The drivers are equipped with internal gate resistors, whose resistance only can be decreased. However, the built in gate resistor has a resistance of 22 Ω but for the IGBT modules used, 27 Ω is recommended [68]. However, IGBT gate resistors of 22 Ω are used for the implementation. In Chapter 4, the influence of the gate resistor value on the switching waveforms is discussed.

The drive circuit SKHI23/12 internally provides blanking time and is also equipped with an interlock function. The interlock function is in this application turned-off. The logic control signals fed to the driver provides the blanking time needed for the hard switched converters.

Quasi resonant DC link IGBTs

Since the peak resonant inductor current is selected to equal the rated battery current, the same IGBT modules can be used for the resonant link IGBTs S_1 and S_2 and the diodes D_1 and D_2. Note that one module is used for each IGBT and freewheeling diode combination, i.e. S_1/D_2 and S_2/D_1. Thus, one IGBT of each module must never be turned on. The driver SKHI23/12 is used also for the resonant link IGBTs, with gate resistors of 22 Ω.

Clamp circuit diodes

The clamp circuit diode D_3, must withstand a blocking voltage of at least six times the DC link voltage, which appears across the diode during the resonant link zero voltage interval. This means that the clamp circuit diode should be selected to sustain a voltage of 4500 V in this case. Consequently, several diodes have to be series connected. Since the series connected diodes are not likely to exhibit the same properties, an additional margin has to be adopted, by means of blocking voltage. Thus, an even more conservative margin than the one used for the other semiconductors, i.e. (2.1), must be used. In the implemented design, six 1500 V diodes are series connected, implying a voltage margin of 100 %.

Furthermore, since the series connected diodes do not have exactly the same characteristics, a voltage dividing network is adopted. The voltage dividing network used for the implementation is shown in Figure 6.2.

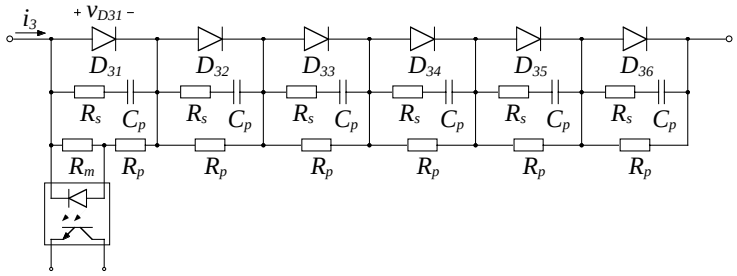


Figure 6.2 The six series connected diodes for realising D_3 together with the voltage dividing network added. An opto-coupler is used to detect clamp action.

The parallel resistors, R_p, are used to divide the total blocking voltage among the series connected diodes during stationary blocking conditions. Otherwise, differences in the reverse leakage current characteristic for the diodes can cause severe reverse voltage imbalance among the six diodes. The parallel capacitors, denoted C_p, are used to divide the total blocking voltage during the turn-off transients. This is needed due to the fact that the series connected diodes possibly exhibits different amounts of reverse recovery charge, Q_{rr}, leading to the fact that one of the diodes will start blocking before the other. Thus, this diode is exposed to the total blocking voltage appearing at the moment. In [63] selection of proper parallel resistor and capacitor values is discussed. As seen in Figure 6.2, another resistor, R_s, is connected in series with each parallel capacitor C_p. This resistor is included in order to dampen oscillations between C_p and the stray inductance of the circuit.

In order to select proper diodes for the clamp circuit, the effect of reverse recovery is investigated. Figure 6.3 shows an equivalent of the clamp circuit with an equivalent parallel capacitor added. Also the stray inductances of the circuit are included.

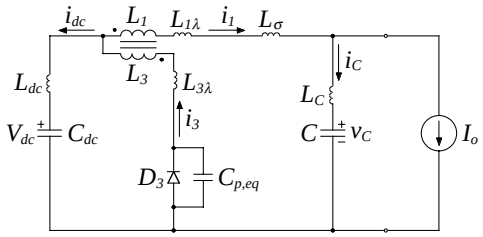


Figure 6.3 Clamp circuit equivalent for investigating influence of clamp diode reverse recovery and circuit stray inductance.

The equivalent parallel capacitor, for six series connected diodes, is given by

$$C_{p,eq} = \frac{1}{6} C_p \tag{6.2}$$

The idea of the following investigation, is to study the effect of the reverse recovery current of D_3. Assume that the investigation starts when the off resonance interval is entered, i.e. immediately after the clamping interval. Note that the stray inductances are neglected in this investigation. The current through the equivalent parallel capacitor is coupled to the clamping transformer giving

$$i_3' = \frac{N_3}{N_1} C_{p,eq} \cdot \frac{dv_C}{dt} \tag{6.3}$$

where N_1 and N_3 are the winding turns number of the clamping transformer. The differential equation for the circuit in Figure 6.3, neglecting the stray inductances, is thus written

$$L_1 \left(C + \left(\frac{N_3}{N_1} \right)^2 \cdot C_{p,eq} \right) \cdot \frac{d^2 v_C}{dt^2} + v_C = V_{dc} \tag{6.4}$$

The general solution to the differential equation is given by

$$v_C(t) = A \cos \omega_{eq}(t - t_4) + B \sin \omega_{eq}(t - t_4) + V_{dc} \tag{6.5}$$

where the characteristic angular frequency is given by

$$\omega_{eq} = \frac{1}{\sqrt{L_1 \left(C + \left(\frac{N_3}{N_1} \right)^2 \cdot C_{p,eq} \right)}} \tag{6.6}$$

It is assumed that the reverse recovery is extremely snappy, i.e. the diode current returns to zero, from its negative peak value, abruptly. This means that the initial resonant link capacitor current will be non zero in this case. If the peak reverse recovery current is denoted I_{rr}, the constants of the differential equation above, is given by

$$\begin{cases} A = (K-1) V_{dc} \\ B = \dfrac{1}{\omega_{eq} C} \left(\dfrac{N_3}{N_1} \right) I_{rr} = \dfrac{1}{C} \sqrt{L_1 \left(C + \left(\dfrac{N_3}{N_1} \right)^2 C_{p,eq} \right)} \cdot \left(\dfrac{N_3}{N_1} \right) I_{rr} \end{cases} \tag{6.7}$$

This means that the minimum resonant link voltage obtained during the off resonance interval becomes

$$v_{C,min} = V_{dc} - \sqrt{A^2 + B^2} \tag{6.8}$$

Hence, the minimum resonant link voltage is lower than calculated in Section 3.1. The problem is that, as the off resonance interval oscillation continues, the resonant link voltage will enter a clamping condition again, though operating in the off resonance interval. This occurs since more energy than previously assumed, is oscillating in the circuit.

As shown above, proper selection of the clamp circuit diodes is an important issue, since even a low reverse recovery current affects the behaviour of the resonant circuit to a large extent. Therefore, three fast diode modules of type Semikron SKKD42F15 [68], consisting of two series connected diodes each, is selected for the implementation. The voltage dividing network components are selected as

$$\begin{cases} R_p = 100 \text{ k}\Omega \\ R_s = 1 \ \Omega \\ C_p = 10 \text{ nF} \end{cases} \tag{6.9}$$

Note that the voltage dividing capacitors in the clamp circuit also affects the other modes of operation, since the total capacitance of the resonant circuit is increased. Consequently, the characteristic angular frequency decrease.

Clamp transformer

The clamp transformer design is also an important issue. First, the importance of keeping the stray inductances of the resonant circuit at a minimum, where the clamp transformer leakage inductances take part, is highlighted. This is done with aid of Figure 6.3. The critical instant to be investigated, is when the resonant circuit traverses from the ramp up interval to the clamping interval. The resonant inductor current i_1, immediately prior to the clamping interval, is expressed as

$$i_1(t_3^-) = I_o + \Delta i_1 \tag{6.10}$$

where Δi_1 corresponds to the excess energy stored in the clamping transformer L_1/L_3. Assuming that the stored magnetic energy does not change during this short interval, the following relationships are established

$$\begin{cases} i_C = i_1 - I_o \\ i_{dc} = i_1 - i_3 \\ i_1 - I_o + i_3 \dfrac{N_3}{N_1} = \Delta i_1 \end{cases} \Rightarrow \begin{cases} \dfrac{di_C}{dt} = C\dfrac{d^2 v_C}{dt^2} = \dfrac{di_1}{dt} \\ \dfrac{di_{dc}}{dt} = \left(1 + \dfrac{N_1}{N_3}\right) C\dfrac{d^2 v_C}{dt^2} \\ \dfrac{di_3}{dt} = -\dfrac{N_1}{N_3} C\dfrac{d^2 v_C}{dt^2} \end{cases} \tag{6.11}$$

The following equations are also valid

$$\begin{cases} V_{dc} - L_{dc}\dfrac{di_{dc}}{dt} - v_1 - \left(L_{1\lambda} + L_\sigma\right)\cdot\dfrac{di_1}{dt} - L_C\dfrac{di_C}{dt} - v_C = 0 \\ V_{dc} - L_{dc}\dfrac{di_{dc}}{dt} - v_1\dfrac{N_3}{N_1} - L_{3\lambda}\dfrac{di_3}{dt} = 0 \end{cases} \tag{6.12}$$

where L_{dc} and L_C are the equivalent series inductances of C_{dc} and C, respectively. The leakage inductance of the clamp transformer windings are denoted $L_{1\lambda}$ and $L_{3\lambda}$. L_σ represents the stray inductance not associated with a particular component, i.e. the stray inductance of the supply rails etc. By combining the previous expressions it is found that

$$L_{stray} C\frac{d^2 v_C}{dt^2} + v_C = \left(1 + \frac{N_1}{N_3}\right) V_{dc} = K V_{dc} \tag{6.13}$$

where the total stray inductance, L_{stray}, is written

$$L_{stray} = \left(1 + \frac{N_1}{N_3}\right)^2 \cdot L_{dc} + L_{1\lambda} + L_\sigma + L_C + \left(\frac{N_1}{N_3}\right)^2 \cdot L_{3\lambda} \tag{6.14}$$

The characteristic angular frequency for this circuit is thus

$$\omega_{stray} = \frac{1}{\sqrt{L_{stray} C}} \tag{6.15}$$

Since the initial capacitor current equals Δi_1, the resonant link peak voltage becomes

$$\hat{v}_C = K V_{dc} + \frac{\Delta i_1}{\omega_{stray} C} \tag{6.16}$$

From the derivation above, the importance of keeping the stray inductance of the circuit low becomes clear. Note that especially the DC link capacitor equivalent series inductance, denoted L_{dc} in the derivation, affects the over voltage experienced. However, this inductance is usually rather low, at least compared to the leakage inductance of the clamp transformer windings denoted $L_{1\lambda}$ and $L_{3\lambda}$.

In order to minimise the clamp transformer leakage inductance, a coaxial winding transformer [29], [33] is adopted for the passively clamped two switch quasi resonant DC link investigated in [7], [8] and [17]. By using a coaxial winding arrangement, the leakage inductance becomes very low and in [33] a magnetic coupling factor of 0.999 is obtained.

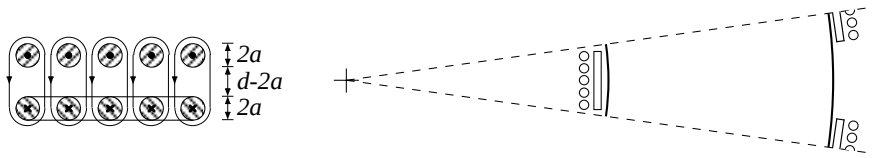
However, the coaxial winding transformer has a large drawback in the fact that it is complicated to manufacture a winding with several turns. This means that designing a transformer for a certain self inductance results in the need of a core having a large cross sectional area. In [8] and [29], several toroidal cores are mounted along an U-shaped coaxial winding, to form the transformer. The primary is the outer, hollow conductor, which in effect is wound less than one turn. The secondary conductor is thus inside the primary, to form a coaxial winding.

Here, a different approach is used for the implementation of the clamp transformer, since it should be designed for a given primary self inductance. The idea is to wind the primary and secondary conductors in parallel paths, which is a well known method to obtain low leakage inductance [63]. In this case, the winding turns ratio should be 1:5 to give a clamp voltage 20 % higher than the DC link voltage. Hence, a split winding technique has to be adopted. The split winding technique for a coaxial transformer is discussed in [8].

For the parallel primary and secondary conductors discussed here, the split winding technique means that the primary and secondary should be wound together upon the transformer core. To accomplish this, $2 \cdot N_3/N_1$ parallel conductors are wound, with a turns number equal to the desired number of primary turns, i.e. N_1 turns in this case. Then, N_3/N_1 conductors are connected in parallel, to form the primary and N_3/N_1 conductors are connected in series, to form the secondary.

For the clamp transformer design, a band conductor is used for the primary and a circular conductor for the secondary, see Figure 6.4. The combination shown in Figure 6.4 is wound upon the iron core, with the number of turns required for the primary. Then the five circular conductors are connected in series to form the secondary. This

corresponds to the split winding technique, since the band conductor can be regarded as consisting of five parallel conductors, which is also implied in Figure 6.4.



(a) (b)

Figure 6.4 The investigated winding arrangement (a), with the band conductor equivalent for the five parallel conductors indicated and (b), 1/22nd of the clamp transformer core with the windings.

According to [10], the leakage inductance for two parallel circular conductors, is calculated from (in the unit H/m)

$$L_\lambda = \frac{\mu_0}{\pi}\left(\frac{1}{4} + \operatorname{arccosh}\left(\frac{d}{2a}\right)\right) \tag{6.17}$$

The split winding technique gives the leakage inductance for the primary, $L_{1\lambda}$, and secondary, $L_{3\lambda}$, as

$$\begin{cases} L_{1\lambda} = \dfrac{N_1}{N_3} L_\lambda N_1 \cdot MLT = \dfrac{\mu_0}{\pi}\left(\dfrac{1}{4} + \operatorname{arccosh}\left(\dfrac{d}{2a}\right)\right) \cdot \dfrac{N_1^2}{N_3} \cdot MLT \\ L_{3\lambda} = \dfrac{N_3}{N_1} L_\lambda N_1 \cdot MLT = \dfrac{\mu_0}{\pi}\left(\dfrac{1}{4} + \operatorname{arccosh}\left(\dfrac{d}{2a}\right)\right) \cdot N_3 \cdot MLT \end{cases} \tag{6.18}$$

where MLT is the mean length per winding turn.

The core used for the implemented clamp transformer is an iron powder core of type Micrometals T650-8/90 [67]. The following specification for the clamp transformer is listed in Table 6.1.

Table 6.1 Clamp transformer specification.

Inductor	Core	A_L (nH/N^2)	N (turns)	A_{Cu} (mm^2)	L (μH)
L_1/L_3	T650-8/90	200	22/110	12.5/2.0	96.8/2420

In Figure 6.4, 1/22nd of the transformer with the winding arrangement used is shown. However, note that additional insulation is used since (N_3-1)/N_3 of the total secondary voltage will appear between two adjacent winding turns, in this case 0.8·5·750 V=3000 V. At such high voltage and

short distance between the conductors, there is a potential risk of partial discharge or corona effects appearing, destroying the insulation. Here, this is solved by using an insulating mica foil between the conductors, see Figure 6.5. Also the core itself is covered with mica foil, wound directly upon it.

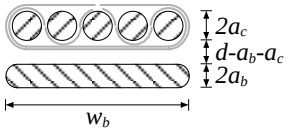


Figure 6.5 The winding arrangement used for the implemented clamp transformer. Note the mica film (grey), which is used to eliminate insulation problems by means of partial discharge.

Resonant inductor

The resonant inductor L_2 used for the implementation is designed almost according to the specification used in the simulation, i.e. Section 5.2. However, since the self inductance of the clamp transformer primary, i.e. L_1, is lower in the implementation, the inductance of L_2 is also lowered in such a way that the ratio L_2/L_1 used in the simulation, is preserved also for the implementation. The specification for the resonant inductor L_2 is given in Table 6.2.

Table 6.2 Resonant inductor specification.

Inductor	Core	A_L (nH/N^2)	N (turns)	A_{Cu} (mm^2)	L (μH)
L_2	T300-2	11.4	68	4.5	52.7

The inductor was intentionally designed to be wound with Litz wire [44], consisting of at least 12 parallel strands. Consequently, a copper fill factor k_{Cu} equal to 0.2 was assumed at the design stage. However, it was not possible to manufacture the inductor with this type of conductor. Instead only two parallel wires were used. This results in the fact that the iron powder core is somewhat oversized due to the increase in copper fill factor, by using fewer parallel conductors. Skin effect [44] of the copper conductor current can also become a problem since the AC resistance increases with increasing frequency.

Resonant link capacitor

The resonant link capacitor C, consists of six discrete capacitors connected in parallel, three 10 nF and three 12 nF, to give a total capacitance of 66 nF. The reason for not using three parallel 22 nF as in the simulation of

Section 5.2, is because the converter should also be operated under hard switched conditions. It is advantageous to distribute the capacitance among the IGBT-modules since they serve as overvoltage snubbers in the hard switched case. The capacitors used for the implemented quasi resonant DC link, to form the resonant link capacitor, are from the Rifa PHE 428 series [64], see Section 5.2.

6.2 Quasi resonant DC link controller

In this section, the quasi resonant DC link controller is described. The controller is used to operate the resonant link IGBTs in a proper way, and to delay the modulator control signals fed to the converter drive circuits until zero link voltage is established. These tasks seems, at a first glance, rather simple to implement. However, several important issues have to be considered. First of all, error states of the resonant link must be detected. The right control actions must then be taken to solve the problem. The second issue is that the IGBT drive circuits have an internal time delay of about 1 μs, which also has to be considered.

In order to obtain safe operation of the quasi resonant DC link, two signals are measured. First, clamp action is detected by the opto-coupler shown in Figure 6.2. This is needed due to the fact that a resonant cycle must not be initiated before the previous is completely finished. If the resonant link IGBTs, S_1 and S_2, are turned on when the circuit is in the clamping state, too much resonant energy is stored in the circuit. As a consequence, the peak resonant inductor current i_2 will become considerably higher than expected, which means that S_1 and S_2 experience higher current stress than expected.

The opto-coupler in the circuit for clamp action detection is used to provide galvanic isolation between the main circuit and the control electronics. This is especially important in this case, because of the location in the clamp circuit where a voltage of several kV appears. The opto-coupler input is connected across a resistor, R_m, equal to 2 kΩ.

Also the current i_2 is measured for operational reasons. As implied above, a high peak value of this current might result in resonant link IGBT failure. Therefore, the current i_2 is measured in order to detect errors resulting in a high peak value, occurring due to other problems than the previously discussed. The current i_2 is measured with a LEM current transducer of type LA50P, which has a rated current of 50 A, but can measure currents up to 70 A. The main advantages gained by using a LEM current transducer are the high bandwidth and galvanic isolation.

The need for galvanic isolation is discussed above. A high bandwidth is not necessary for control of the quasi resonant circuit, since the measured current is only compared to a pre-set value to detect over current. However, to analyse the circuit, the current should be measured anyway and therefore the high bandwidth is favourable.

The state machine for resonant link control is shown in Figure 6.6. The resonant link controller is implemented in a programmable logic device, PLD, which in fact consists of two PAL22V10 integrated circuits. One of these integrated circuits is used to implement an asynchronous state machine which keeps track of the resonant cycle, see Figure 6.6. In the other integrated circuit, a timer function to control the duration of each interval is implemented.

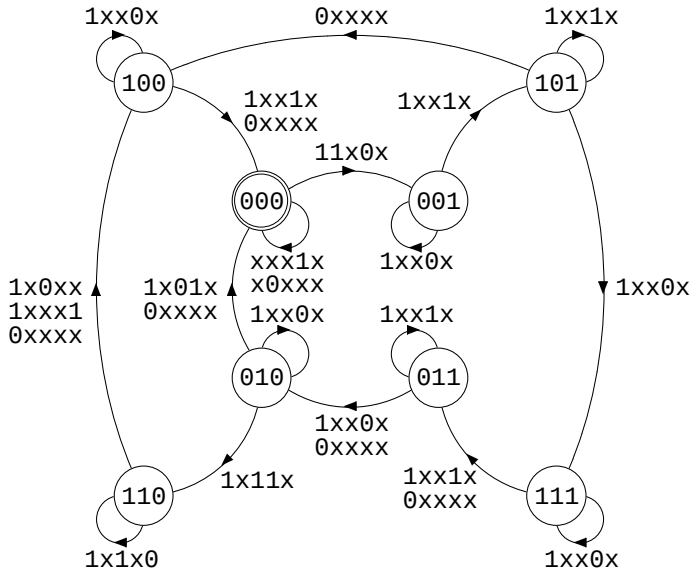


Figure 6.6 State graph showing the implemented quasi resonant DC link controller. The state machine is implemented in PAL circuits.

In Figure 6.6, the input sequences resulting in the state transitions are shown next to each graph symbolising the possible transitions. The input sequence is formed by the following digital signals

```
Input_sequence = [Enable,Soft_start,Clamp,Timer,Timer_clamp]
```

The input signal `Enable` is set as long as no error occurs, i.e. as long as over current is not detected. `Soft_start` is set when the carrier wave modulator commands a change of any of the converter switch states. This

is implemented as an exclusive or function between the actual and commanded switch state for the switch states of each converter half bridge. The `Clamp` signal is set during clamp action. Note that the opto-coupler shown in Figure 6.2 is actually inverting, which means that the signal `Clamp` is directly given. The `Timer` and `Timer_clamp` signals are intended for synchronisation of the state machine. The states shown in Figure 6.6, correspond to the different modes of operation of the quasi resonant circuit. As seen there are eight logic states where two of them are needed due to the IGBT drive circuit delay. These two states are referred to as intermediate or transition states. The states are described in Table 6.3.

Table 6.3 Description of the states of the quasi resonant controller and modulator.

State	Description
`000`	Idle condition, corresponds to off resonance
`001`	Ramp down. Resonant link IGBTs turned on.
`101`	Ramp down intermediate state. The new switch state is applied to the drivers.
`111`	Zero voltage interval.
`011`	Zero voltage intermediate state. The resonant link driver control signal is set low.
`010`	Resonant link voltage ramp up interval.
`110`	Clamping interval.
`100`	Clamping intermediate interval needed to obtain a hazard free realisation.

As seen in Figure 6.6, the `Timer` signal is very important for the controller operation. Note that for each state whose transitions are triggered by the `Timer` signal, the logic state is maintained for a certain time set for the particular state. For each such state, the time set should correspond to the duration of the resonant link mode in question. Therefore, the times set have to be tuned, even though the simulated waveforms gives the approximate duration of each interval.

Note that since the `Timer` signal is involved in almost all the state transitions of the entire quasi resonant modulator and controller, the state machine might as well be implemented as a synchronous state machine. However, the PAL22V10 integrated circuits only have one clock signal, which is used to update the converter switch state, i.e. used as a clock signal fed to the latches needed to delay the drive circuit input signals to wait for the zero voltage interval. This clock or update signal is trigged during the resonant link voltage ramp down interval, as soon as the ramp down intermediate state is entered.

The logic signal controlling the resonant link IGBT drivers, is simply the last bit of the three bit pattern used to symbolise the logic states.

6.3 Measurements

In this section the measured results are presented and compared to the simulated. Waveforms of the quasi resonant DC link quantities are shown, and discussed. The converter efficiency is measured for both the quasi resonant and the hard switched battery chargers, and compared to simulation results.

The tests are made at a lower converter DC link voltage than designed for, due to overvoltage problems arising from the stray inductance of the power electronic main circuit. The DC link voltage used for the measurements therefore equals 650 V. This means that the rated maximum current step which the quasi resonant DC link is designed for, is lowered by the ratio (650/750), i.e. to approximately 23.1 A. Consequently, the rated battery current is decreased to the same level. In effect, the rated output power of the battery charger is decreased by the ratio $(650/750)^2$, to become 7.5 kW. The large reduction in output power is due to the fact that the rated battery voltage equals half the DC link voltage. This is of minor importance since such a high DC voltage is not available, at least not for the current level required, in the laboratory. Therefore, the efficiency measurements are performed at rated battery side output current and a DC voltage of 240 V. For practical reasons, the DC voltage is generated by a rotating converter instead of electro-chemical batteries.

Waveforms

The resonant link waveforms shown in this section are measured with a Tektronix TDS 640A four channel digitising oscilloscope in all cases but one, which will be pointed out. The resonant currents i_1 and i_3 are measured by a LEM RR3330-SD Rogowski current transducer, whose output amplifier has a quite narrow bandwidth which is seen in the measured signals, later on. Also note that a Rogowski current transducer can not measure DC currents, which means that no attention should be paid to the DC level of the currents i_1 and i_3 shown in the figures of this section.

In the first part of this section, the attention is focused on test of the resonant link operation and parameter estimation. The measurements

shown at this stage are made at a DC link voltage close to 375 V and at idle conditions with the battery charger output disconnected.

In Figure 6.7, first a resonant cycle is shown and then an off resonance interval of long duration follows.

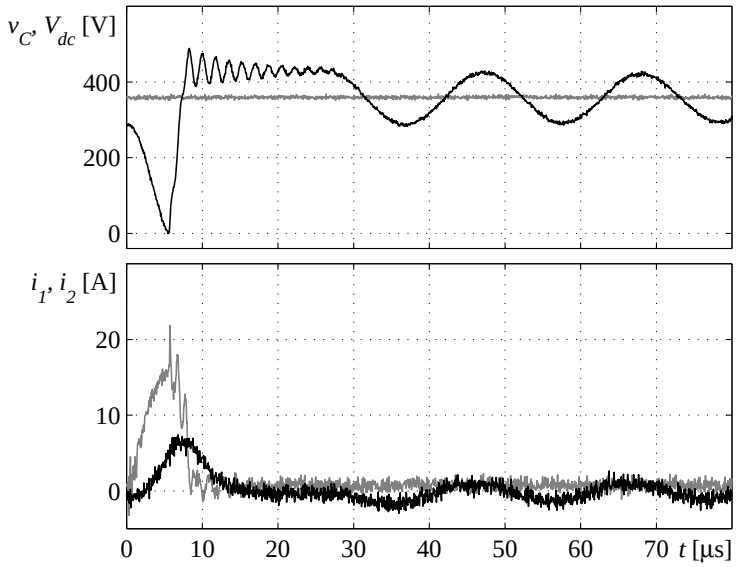


Figure 6.7 Off resonance oscillation at reduced DC link voltage. The waveforms shown are v_C (upper, black), V_{dc} (upper, grey), i_1 (lower, black) and i_2 (lower, grey).

During off resonance operation, the resonant link voltage is still oscillating due to resonance between L_1 and C, which is discussed in Chapter 3. Note the magnitude of the oscillating voltage which is between 0.8 and 1.2 times the DC link voltage, which also is concluded from Chapter 3. Also note the ringing seen in both the resonant link voltage v_C and the resonant current i_2, when the resonant link enters the clamping interval, in Figure 6.7.

In Figure 6.8, the clamp circuit current i_3 and the forward voltage v_{D31} across one of the six clamp circuit diodes, see Figure 6.2, are shown. For convenience, also the resonant link voltage is shown. The poor bandwidth of the Rogowski current transducer is clearly seen in Figure 6.8. From Figure 6.8, it is also clear that the Rogowski current transducer can not reproduce the accurate DC level of the measured current. A Rogowski coil can not be used to measure a DC current, since it in fact is equivalent to an air wound transformer.

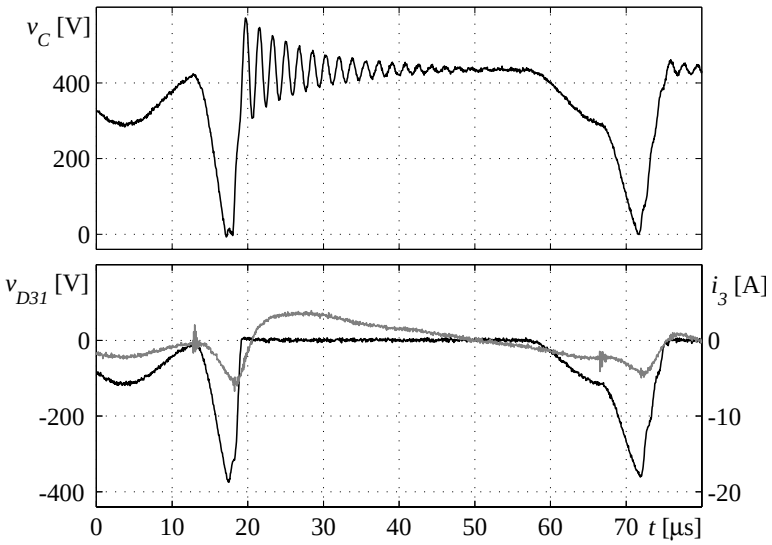


Figure 6.8 Clamp circuit waveforms. The upper part shows the resonant link voltage. The lower part shows the diode forward voltage, v_{D31}, of one of the six series connected clamp circuit diodes (black) and the clamp transformer secondary current i_3 (grey). Since the current is measured with a Rogowski current transducer, the DC level is not accurately shown.

The results shown in Figure 6.7 and Figure 6.8 are used to estimate the resonant circuit actual passive component values by means of inductance and capacitance. The time derivative of i_3 in Figure 6.8, together with the measured DC link voltage gives the self inductance of the clamp transformer secondary, i.e. L_3. The resonant link voltage during the clamping interval and the DC link voltage gives the clamping factor K, which means that also L_1 is estimated. Then the off resonance oscillation period time is measured, which together with L_1 gives the total equivalent capacitance of the circuit.

The passive component value which is hardest to estimate is definitely L_2. Here, L_2 is estimated from the second resonant cycle shown in Figure 6.8, by measuring the time to complete the resonant link voltage ramp down interval. However, as seen in Figure 6.8, the resonant circuit is not started at rest, implying that the actual initial conditions must be used instead of the ones derived for this mode in Chapter 3. On the other hand, this is not a severe problem, since the cycle starts close the resonant link voltage minimum for the off resonance interval. Thus, the resonant capacitor current i_C is regarded as being equal to zero. By iterating equation (3.5) with these initial conditions, the inductance of L_2 is estimated.

According to the measurements discussed above, the following passive component values are estimated

$$\begin{cases} L_1 = 97.5\ \mu\text{H} \\ L_2 = 54.6\ \mu\text{H} \\ L_3 = 2.32\ \text{mH} \\ C + \left(N_3/N_1\right)^2 \cdot C_{p,eq} = 112\ \text{nF} \end{cases} \tag{6.19}$$

Also the oscillation period time at the start of the clamping interval, shown in the resonant link voltage measurement of Figure 6.8, is measured. This oscillation time together with the passive component values previously calculated, gives the total stray inductance L_{stray} according to equation (6.15). This gives

$$L_{stray} = 1.11\ \mu\text{H} \tag{6.20}$$

assuming that the equivalent series inductance of the DC link capacitor L_{dc} equals 30 nH and that all other stray inductances equals zero except the clamp transformer leakage inductances. If the latter are considered being equal seen from the primary or secondary it is found that

$$L_{1\lambda} = 533\ \text{nH} \tag{6.21}$$

This corresponds to a magnetic coupling factor equal to 0.995, which is fairly high. However, it is not high enough for the application which is reflected in the fact that the quasi resonant battery charger is operated at a maximum DC link voltage of 650 V, whereas it was designed for 750 V.

Another interesting feature investigated at low DC link voltage is the effect of clamp circuit diode reverse recovery. The fairly shallow slope of i_3 during the clamping interval, indicates that the reverse recovery current of the clamp circuit diodes is likely to be low even if rectifier diodes are used. Therefore, six rectifier diodes of type Semikron SKKD46/16 [68] were tested in the clamp circuit. The measured resonant link voltage for this case is shown in Figure 6.9. Note that this measurement is made with a different oscilloscope, Philips PM 3384A, which has one fourth of the bandwidth of the oscilloscope used for the rest of the measurements.

Although, the time derivative of the clamp circuit current i_3 is low, the reverse recovery problem discussed previously in this chapter shows up. Note that clamping occurs also in the off resonance interval.

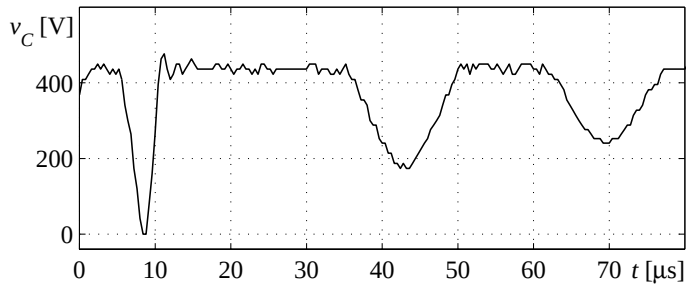


Figure 6.9 Resonant link voltage, when rectifier diodes are used in the clamp circuit. Note the large magnitude of the off resonance oscillation and the fact that clamp action occurs during this interval.

By use of equation (6.7), it is found that the reverse recovery current I_{rr} is equal to 0.75 A for the case shown in Figure 6.9. Since the resonant circuit behaviour shown in Figure 6.9 is not acceptable, the fast diode SKKD42F15 is used for the clamp circuit instead of the rectifier diode.

One important conclusion to be drawn from the measurements above and the discussion previously in this chapter, is that the voltage sharing capacitors needed for realisation of the clamp circuit diode, D_3, do affect the resonant link waveforms. This is reflected in the fact that the duration of both the resonant link ramp down and ramp up interval becomes longer than for the case simulated in Chapter 5. This alone increases the total cycle time. Moreover, the duration of the clamping interval also becomes longer due to the fact that the voltage time areas of these two intervals together with the zero voltage interval should equal the one of the clamping interval, on the average [7]. The increase of the total cycle time results in the fact that the switching instants for the implemented battery charger are further delayed.

There are also advantages gained by the increased equivalent capacitance. The resonant link voltage derivative becomes lower than expected which is advantageous in itself. Also, the need for accurate timing becomes less pronounced due to the fact that the voltage is low for a longer time since the resonant link voltage slopes are more shallow. Note that the overvoltage due to circuit stray inductance is not affected by the additional capacitance, since $C_{p,eq}$ is shorted by D_3 during the clamping interval.

The rest of the measurements are made at a DC link voltage level of 650 V. The battery side output current reference value is equal to 23 A, unless otherwise specified. In Figure 6.10, one resonant cycle for the case when clamping do not occur is shown.

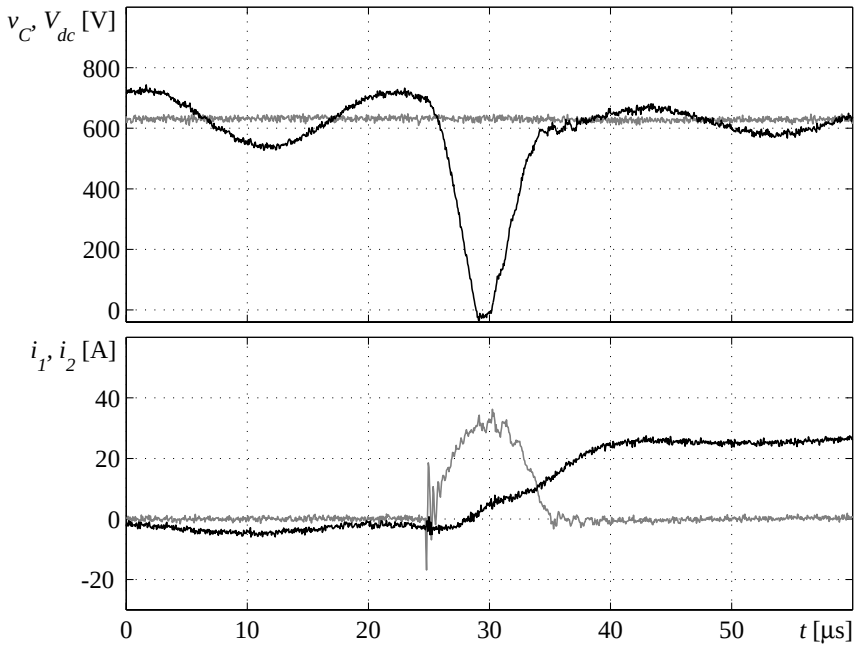


Figure 6.10 Resonant link waveforms for one cycle in the case when clamping do not occur. The upper part shows resonant link voltage v_C (black) and the DC link voltage V_{dc} (grey). In the lower part, the resonant currents i_1 (black) and i_2 (grey), are shown.

In Figure 6.10, the upper battery side converter IGBT is turned on at rated current (for the DC link voltage used). In Figure 6.11 both positive and negative resonant DC link output current steps are shown. Note that the current steps for two of the resonant cycles shown in Figure 6.11, are larger than the rated ones. These large output current changes occurs due to the fact that several half bridges are switched during the very same resonant cycle.

The passive component values are selected based on a resonant DC link output current change equal to the rated battery side converter output current, according to Section 3.1. There it is also stated that for a resonant link output current increase larger than the rated, the resonant link voltage will start to decrease when i_2 has decreased to zero during the resonant link voltage ramp up interval. This occurs due to the fact that i_1 has not reached the level corresponding to the new converter switch state. However, this is not seen in Figure 6.11, although the positive output current step of the first resonant cycle shown is about 30 A. The reason why this does not occur, is due to the time control used for the resonant circuit.

The resonant link IGBTs are kept on for a constant time, and the length of the ramp down interval used in the controller must cover the worst case. This means that in some cases the zero resonant link voltage is maintained for longer than 1 μs which is used in the selection of the resonant link passive components. The longer duration of the zero voltage interval thus implies that more energy than expected is stored in the circuit when the clamping interval is entered.

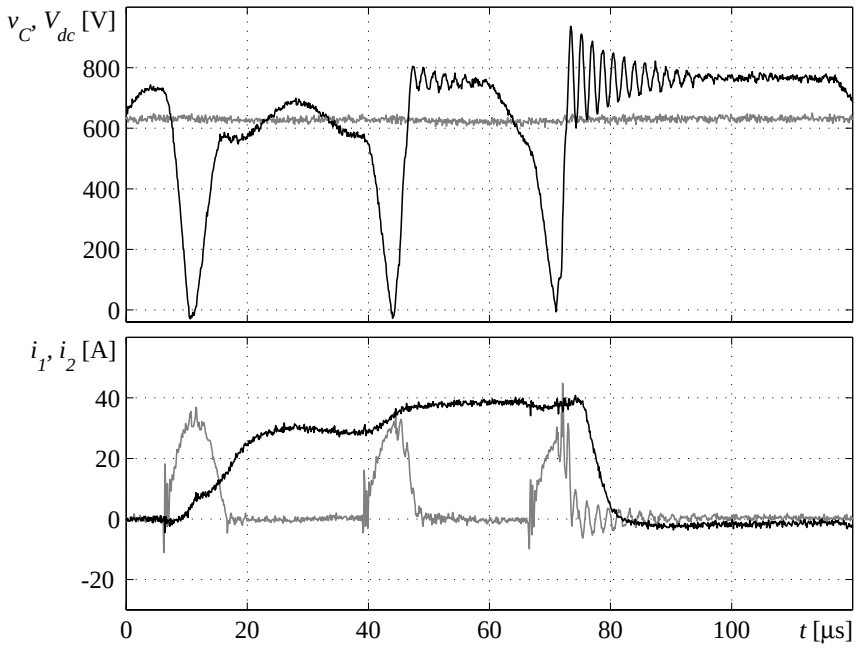


Figure 6.11 Resonant link waveforms for large positive and negative current steps. Note that the output current decrease during the last resonant cycle is larger than the rated maximum. The upper part shows resonant link voltage v_C (black) and the DC link voltage V_{dc} (grey). In the lower part, the resonant currents i_1 (black) and i_2 (grey), are shown.

In Figure 6.12, the resonant link waveforms are shown for a time interval corresponding to one period of the modulation carrier.

As seen in Figure 6.11 and Figure 6.12, the resonant inductor current i_2 has a higher peak magnitude than expected from the design expression. The high peak value of i_2 results from the increase of the equivalent resonant link capacitor due to the capacitive voltage dividing network used in the clamp circuit. Also, note that the peak value of i_2 is dependent on the level of the resonant link voltage v_C and the capacitor current i_C, at the start of the resonant cycle.

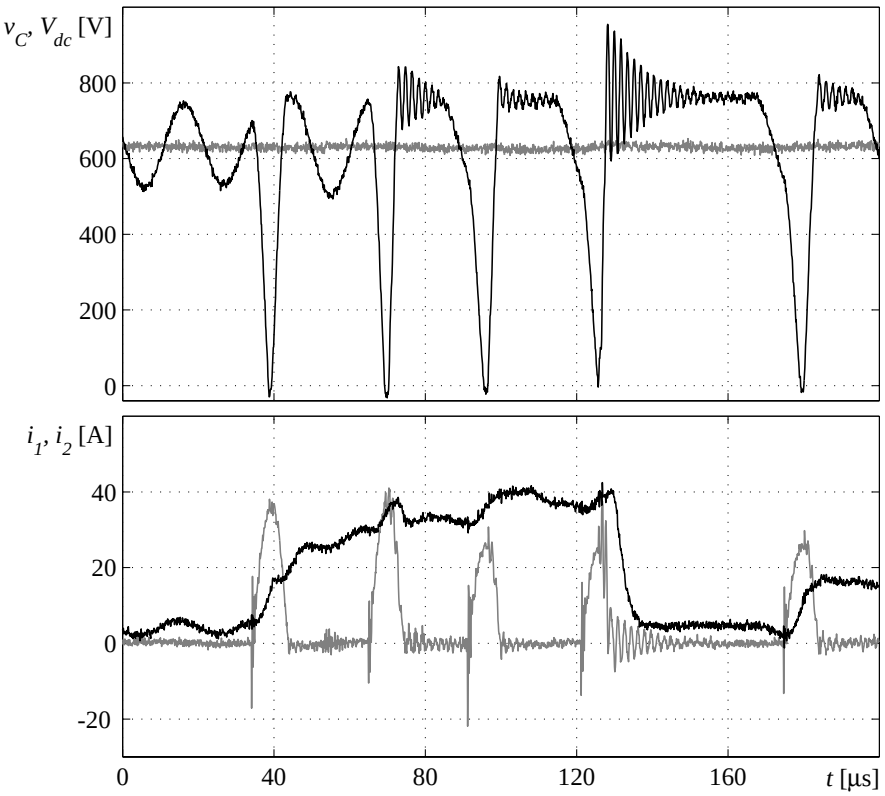


Figure 6.12 Resonant link waveforms for a time interval corresponding to the modulation carrier time period. This means that ideally eight distinct resonant cycles should take place but in the case shown several switchings are made during some of the resonant cycles. The upper part shows resonant link voltage v_C (black) and the DC link voltage V_{dc} (grey). In the lower part, the resonant currents i_1 (black) and i_2 (grey), are shown.

Figure 6.12 shows the previously discussed problem associated with a too high amount of resonant energy stored when the clamping interval is entered. This both gives a higher over voltage due to the stray inductance of the circuit according to (6.16) and a longer duration of the clamping interval according to (3.38).

In Figure 6.12, only five resonant cycles take place, whereas ideally eight should be performed. This implies that more than one of the four converter half bridges are switched simultaneously for some of the resonant cycles. During a clamping interval, several switching transitions might be held to await the next zero voltage interval. Therefore, the modulator commands are delayed a varying time, depending on the duration of the clamping interval.

The varying delay time, imposed on the modulator command signals, results in low order harmonics appearing in the output currents, see Figure 6.13.

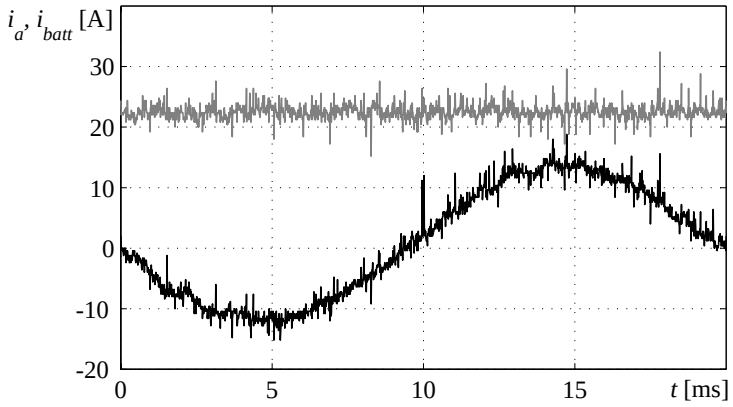


Figure 6.13 One of the line side phase currents (black) and the battery current (grey), in the case of purely inductive output filters at rated current when the DC link voltage equals 650 V.

In Figure 6.13 the input current for one of the AC side phases and the battery side output current, in the case of purely inductive output filters, are shown. Though present, the low order harmonics are not such a large problem in this case. In Figure 6.14, one of the AC side input currents are shown for the outer inductor in the case of a LCL-filter at idle conditions with the battery side disconnected. As shown, a high content of low order harmonics, appears. The high harmonic content results from the fact that the impedance of the LCL-filter is considerably lower than for the L-filter, since the filters are designed to have the same attenuation at switching frequency. The result shown in Figure 6.14 is of course not acceptable, and therefore L-filters are used for all the measurements.

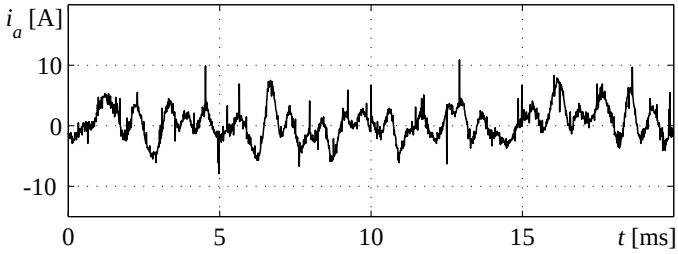


Figure 6.14 One of the line side phase currents in the case of LCL-filter, at idle conditions. Note the magnitude of the low order harmonics. The high harmonic content is due to modulation errors resulting from the fact that the converter control signals are delayed by the resonant link operation.

Efficiency

In order to measure the losses, a power meter is connected to the test set-up. To measure the output power from a voltage source power converter is a complicated task, due to the switched nature of the output voltages, which makes high bandwidth measurements necessary. Therefore, a four channel Norma D 6100 wide band power analyser is used for the measurements, which has a bandwidth of 400 kHz. However, an even higher bandwidth is desirable for the output voltage derivatives appearing in this case. To verify the converter input and output power measurements, the power meter is also connected outside the filters to measure the total power losses of the battery charger. The result of these measurements is shown in Table 6.4.

Table 6.4 Measured battery charger efficiency.

Battery charger	Without output filter losses			Including output filter losses		
	P_{in} [W]	P_{out} [W]	Efficiency	P_{in} [W]	P_{out} [W]	Efficiency
Hard switched	5765	5581	96.8 %	6051	5623	92.9 %
Quasi resonant	5955	5595	94.0 %	6263	5632	89.9 %

A series of measurements are made on each charger in Table 6.4. The variations in efficiency between individual measurements are approximately ±0.5 % to the average efficiency. The results shown in Table 6.4 are individual measurements close to the average of the series, for each case. Note that the variation of ±0.5 % in addition to the bandwidth limitations of the power meter, indicates that the efficiency only can be measured with two significant numbers.

As seen in Table 6.4, the efficiency of the hard switched battery charger seems to be approximately 3 percent units higher than the quasi resonant battery charger efficiency. The inductive filters are responsible of decreasing the efficiency by 4 percent units.

To compare the measured results with simulations, models have to be developed for the semiconductor devices used in the implementation. The simulation software used, SABER™, supports characterisation of semiconductors based on vendor data sheets. However, the behavioural models obtained are not as accurate as the physical models used in the simulations of Chapter 5. The simulated results, at a load condition corresponding to the measurements, are shown in Table 6.5.

Table 6.5 Simulated battery charger efficiency.

Battery charger	Without output filter losses			Including output filter losses		
	P_{in} [W]	P_{out} [W]	Efficiency	P_{in} [W]	P_{out} [W]	Efficiency
Hard switched	5878	5639	95.9 %	5978	5546	92.8 %
Quasi resonant	6025	5661	94.0 %	6122	5567	90.9 %

In Table 6.5, only the leftmost part is of interest since the inductive filters used in the laboratory set-up is not the same as the simulated. In fact, for the measurements the filter inductors are wound on 0.3 mm laminated cores, whereas in the simulation iron powder cores are considered. The reason for not simulating the inductors used in the test set-up, is that the only data available is their inductance.

The simulated converter efficiency for the hard switched battery charger is considerably lower than the measured. However, the efficiency of the battery charger equipped with the quasi resonant DC link shows good agreement between measurements and simulations. The reason for this is the poor semiconductor models used. Especially the switching transients are difficult to model correctly with a behavioural model, since they depend on a lot of factors. For example, both turn-on and turn-off energy dissipation are junction temperature dependent but the model used do not use temperature as an input. Therefore, the simulation model must be characterised for the correct operating temperature to give the correct turn-on and turn-off energies.

The data sheets for the semiconductors used, specifies these energies only at a junction temperature of 125 °C, whereas the heat sink used for the implemented battery charger was kept close to room temperature, i.e. 25 °C, implying that the junction temperature is considerably lower than 125 °C. The on-state, or conduction, losses on the other hand are not as temperature dependent as the switching losses.

The losses of the hard switched converter originates from both switching transients and current conduction. The conduction losses are almost temperature independent but the switching losses increases with increasing temperature. Since the actual junction temperature probably is lower than 125 °C, which the simulation models are based on, the losses are over estimated. For the quasi resonant converter implemented, the conduction losses are dominating, see Section 5.2. Since these are not temperature dependent, at the same extent as the switching losses, the simulated and measured converter efficiencies show better agreement in this case.

7

Conclusions

Quasi resonant DC link converters for a battery charger application are investigated in this thesis. The main topic investigated, regards passive component selection to meet certain performance criteria. Four quasi resonant DC links are designed and then simulated. One of the quasi resonant DC links is implemented in the battery charger application considered, for further investigation. This chapter concludes the results obtained, by means of simulations and measurements. Also some topics for future work on resonant converters are given.

7.1 Results

The design expressions derived in Chapter 3, are used to determine suitable passive component values to meet certain performance criteria. The performance criteria selected for the investigation are the maximum voltage derivative and the maximum duration of the zero voltage interval. However, the most important issue covered by the developed design expressions is to guarantee the operation of the quasi resonant DC link at the worst case load conditions.

In Chapter 5, the four different quasi resonant DC links investigated are simulated. To give a fair comparison, the simulated quasi resonant DC links are designed to meet the same maximum voltage derivative and maximum duration of the zero voltage interval. The simulations shows good agreement with the expressions derived in Chapter 3, by means of design criteria. The energy efficiencies are calculated based on the simulations. From these calculations it is found that the output filters dissipate approximately half the total losses of the battery charger. Also, it is found that the quasi resonant battery chargers do not have lower losses than the hard switched.

One of the quasi resonant DC link battery chargers investigated, is designed and built for 10 kW nominal power. Important aspects regarding the implementation are discussed in Chapter 6. The resonant link waveforms are shown and discussed. Also, the losses of the entire battery

charger and the quasi resonant DC link converter losses are measured. The efficiency of a hard switched battery charger is also measured for comparison. Both the quasi resonant and the hard switched battery chargers are simulated with semiconductor models based on data sheet information. The simulated and measured efficiency do not show full agreement and the reasons for this are discussed.

Both simulations and measurements indicate that the efficiency of the battery charger do not increase by the use of a quasi resonant DC link compared to the hard switched case. The main reason is that the switching frequency is only 5 kHz for the investigated battery charger. At such a low switching frequency, the efficiency is already high for a hard switched converter. In order to fully utilise resonant converter technology the switching frequency should be higher than it is in this study. However, it is also seen from both simulations and measurements that several of the investigated quasi resonant DC links are not suitable for operation at a high switching frequency. Already for the low switching frequency used, the switching instants commanded by the modulator are severely delayed resulting in low order harmonics appearing in the converter output currents. To partly overcome this problem, the restriction on the converter output voltage derivative can be loosen or the clamping factor can be somewhat increased. However, both these actions increase the semiconductor stress.

7.2 Future work

For further investigations of quasi resonant DC link converters two topics are of particular interest, modulation strategies and semiconductors developed for soft switching applications. There is a lot of work done and ongoing, on these topics. For example, for two of the circuits investigated here, by means of passive component selection, there are publications on modulation issues [17], [40]. In [26] semiconductors suitable for soft switching is, to some extent, discussed. The work presented in [54] closely relates to Chapter 3 and Chapter 5. In [54], the resonant link voltage derivative of the quasi resonant DC link converter presented in [11] and [31], is varied to minimise the losses. Still, the results obtained by such investigations are dependent on the type of semiconductors used.

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A

Modulation

In this appendix converter modulation is considered. First, carrier based pulse width modulation (PWM) is introduced. This kind of modulation strategy is often used for hard switched converters, and it is often stated that it is suitable also for quasi resonant DC link converters. However, resonant DC link converters cannot use this kind of modulation strategy, since these converters are only allowed to switch at the zero voltage intervals of the resonant link voltage. This implies that the switching frequency is determined by the resonant link oscillation frequency. The method used for this kind of converters is termed discrete pulse modulation (DPM). Here, only the operation of one such modulation strategy is discussed. Features like differences in output spectrum and so on are discussed in the literature [23], [44], [62], [63], but are left out in this text.

A.1 Carrier based PWM

Carrier based PWM is well discussed in the literature, for example in [23], [44], [62], [63]. Here, carrier based PWM is only discussed to give a more complete description of the control system and its interface to the power electronic main circuit.

The controllers, used in both the simulation and the implementation of the battery charger, generate voltage reference values. These reference values are fed to the modulator where they are transformed into pulses determining whether the upper or lower transistor of each half bridge should be on. This implies that one voltage reference value must be generated for each half bridge, to form the pulse pattern for each half bridge output potential.

In order to generate this pulse pattern, the PWM strategy adopted uses a carrier wave. The carrier wave can have different shapes, for example triangular or saw-tooth shaped. Both for the simulations of the different battery charger topologies and for the implementation, triangular carrier

PWM is used. Anyway, saw-tooth carrier PWM are used for the quasi resonant DC link converters reported in [17], [40], [41].

The switching instants for a particular half bridge are determined by the crossings between the carrier wave and the voltage reference value for the half bridge considered. For an AC converter the voltage reference value is time varying with a frequency determined by the desired output frequency. Of course, the carrier frequency must be several times higher than the frequency of the voltage reference value for the modulation to work properly. The ratio between these two frequencies is referred to as the pulse number, or modulation index.

In order to obtain the proper average output voltage for a certain reference value, the carrier wave amplitude has to be a function of the DC link voltage. Note that the DC link voltage limits the maximum output voltage possible to supply to the load.

To some extent, the converter topology also determines the parameters of the carrier wave. For example one single half bridge (the battery side converter considered in the thesis) can have an average output voltage ideally ranging from zero up to the DC link voltage level. This implies that the carrier wave should vary between these values. On the other hand, a three phase VSC (for example the line side converter considered in this thesis) has both negative and positive instantaneous output voltages, implying that the carrier wave in this case varies between a value corresponding to minus half the DC link voltage to plus half the DC link voltage. All three phases can use the same carrier wave to determine the switching instants in this case.

Note that in both cases above, the peak to peak value of the carrier wave is proportional to the DC link voltage. Also, note that in the three phase converter case, it is not necessary for the carrier to vary between a negative and a positive value, since a constant value can instead be added to each voltage reference value. A constant value added in this manner, corresponds to a zero sequence component which can not be supplied by such a converter anyway [4].

Saw-tooth carrier PWM

As the name implies, the carrier wave in this case is saw-tooth shaped. This means that the carrier will traverse from its minimum value to its maximum (or vice versa) abruptly. When this occurs, the crossing between carrier wave and reference value will occur simultaneously for all phases using this carrier. One example of saw-tooth carrier modulation

of a three phase converter is shown in Figure A.1. Note that the pulse number is considered as very high which means that the voltage references appears as constant for the short time interval shown.

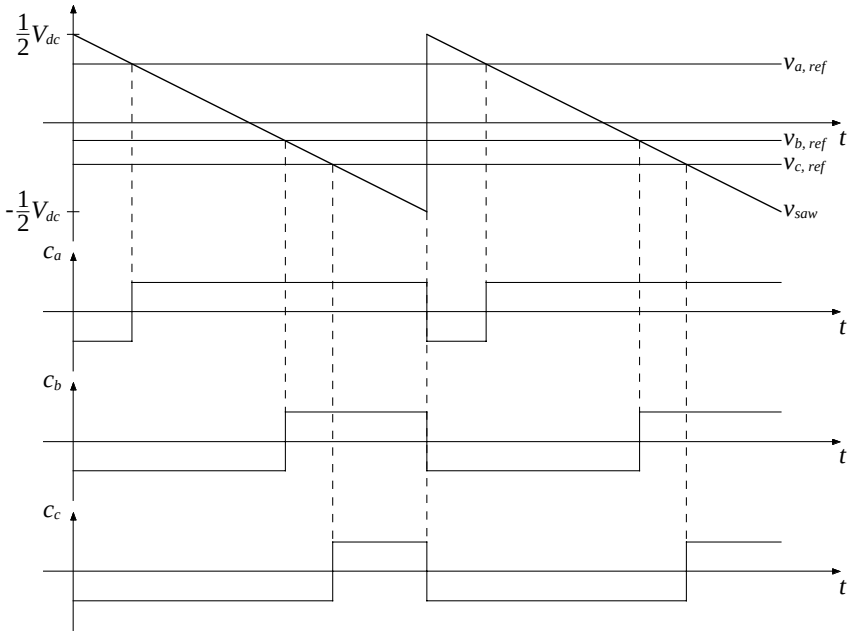


Figure A.1 Saw-tooth carrier PWM of a three phase converter.

In Figure A.1, the reference levels for each phase, $v_{a,ref}$, $v_{b,ref}$ and $v_{c,ref}$, are shown together with the saw-tooth carrier wave v_{saw}. Also the corresponding pulse patterns for each phase, c_a, c_b and c_c, are shown. The interpretation of these pulse patterns is that for each half bridge, a high level corresponds to upper switch (transistor or diode) conducting and a low level means that the lower switch is conducting.

Triangular carrier PWM

Triangular carrier PWM uses a triangular wave as carrier. The main difference in operation compared to the previously discussed saw-tooth carrier PWM, is that in this case simultaneous switching only occurs when two reference values are equal at the carrier crossing. Figure A.2 shows the resulting pulse pattern when triangular carrier PWM is used for a three phase converter. Similar to the previous case, the pulse number is considered as being very high.

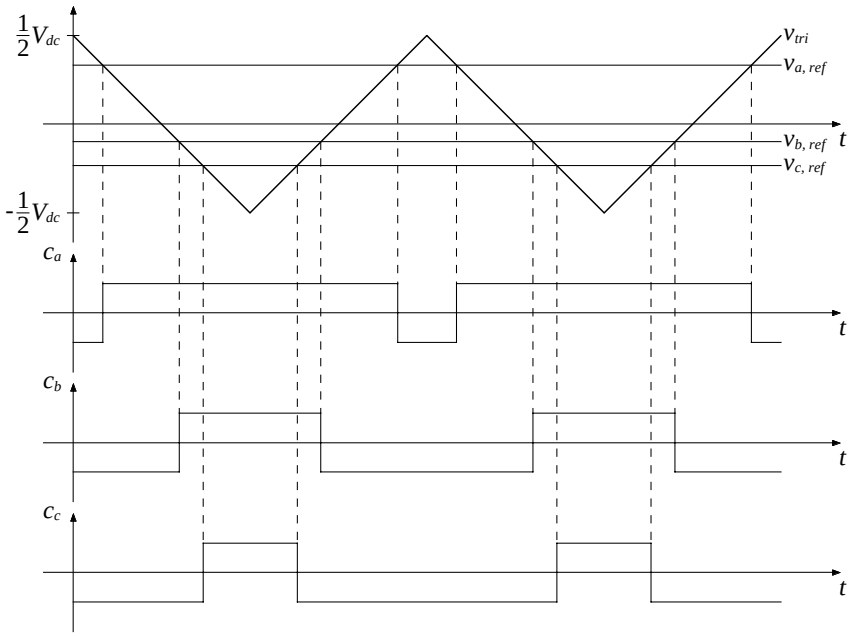


Figure A.2 Triangular carrier PWM of a three phase converter.

The interpretation of the quantities given in Figure A.2 is the same as the one given for saw-tooth carrier PWM, except that the carrier is called v_{tri} in this case.

A.2 Discrete pulse modulation

Discrete pulse modulation is similar to hysteresis control [23]. In hysteresis control the idea is to feed the reference value and the actual value to a comparator with a dead band. The comparator output determines the switch state to be set for each half bridge. In this way the actual value is kept within a hysteresis band located around the reference value.

Voltage regulated sigma delta modulator

The voltage regulated sigma delta modulator (ΣΔM), is the by far most popular modulator used for resonant DC link converters, mainly due to the fact that the modulation is load independent and exhibits relatively good spectral performance [18]. This type of modulator acts upon the error between the measured output voltage and its reference level. The error is fed to an integrator. The output of the integrator is input to a comparator, with hysteresis band equal to zero.

Since this modulator is used for resonant DC link converters, the switching instants commanded by the comparator are delayed until a resonant link voltage equal to zero is obtained. This can be achieved by latching the command signal from the comparator, and the use of another comparator to generate the clock signal to the latch when zero voltage occurs. Figure A.3 shows a schematic of the ΣΔ-modulator for one bridge leg. Here, *K* is the gain of the integrator and D symbolises the D-latch. The signal *zv* fed to the D-latch, is the clock signal which triggers the D-latch when zero voltage is detected.

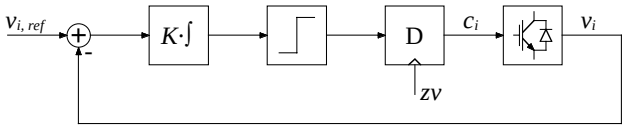


Figure A.3 Schematic picture of the ΣΔ-modulator for one half bridge.

There are a lot of interesting features regarding ΣΔ-modulation, some of them can be found in [13], [18].

B

Control

In this section the controllers used in the simulation model are described. First the battery side current controller is discussed and then the vector current controller used for the line side converter. Finally the DC link voltage controller is discussed. For details on the controller used for the implemented battery charger, see [4].

B.1 Battery side current controller

The simulation model battery or DC side current controller is implemented as a PI controller, with feed forward of the battery voltage. All the controllers discussed in this appendix are based on sampled quantities, i.e. time discrete. Hence, the discrete time battery side PI current controller is written

$$v_{batt}^{*}(k+1) = K \cdot \left(\left(i_{batt}^{*}(k) - i_{batt}(k) \right) + \frac{1}{T_i} \cdot \sum_{n=0}^{k-1} \left(i_{batt}^{*}(n) - i_{batt}(n) \right) \right) + v_{batt}(k) \tag{B.1}$$

where v_{batt} and i_{batt} are the battery voltage and current, respectively. The corresponding reference values are marked with a star (*). The gain of the proportional part is selected in order to obtain dead beat action, i.e. for a step change in the output current reference level, the actual output current should reach this value at the next sampling instant. The following gain, K, and integrator time constant, T_i, are used for the simulation model battery side current controller

$$\begin{cases} K = \dfrac{L}{T_s} + \dfrac{R}{2} \\ T_i = \dfrac{1}{2} + \dfrac{L}{RT_s} \end{cases} \tag{B.2}$$

where L and R are the load inductance and resistance, respectively. The sampling time is denoted T_s.

B.2 AC side vector current controller

The vector controller is based on the synchronously rotating reference frame *dq*-system. This implies that that the three phase quantities (*abc*) have to be transformed into the stationary reference ($\alpha\beta$) frame (two phase quantities) and then further transformed into rotating reference (*dq*) frame (two phase quantities).

The controller acts upon the *dq*-quantities, and also gives reference values expressed in the rotating frame. Therefore, the reference values must be transferred back into three phase quantities before they are passed on to the modulator. However, before the reference values are fed to the modulator they are symmetrised in order to utilise the converter DC link voltage in a more efficient way.

Vector transformations

As stated above, the three phase quantities are transformed into two phase quantities, i.e. from *abc* to $\alpha\beta$-quantities. This means that a vector $\vec{s}$ in the stationary $\alpha\beta$ -frame is expressed as

$$\vec{s}^{\,\alpha\beta} = \sqrt{\frac{2}{3}} \cdot \left(s_a + s_b e^{j(2\pi/3)} + s_c e^{j(4\pi/3)} \right) = s_\alpha + j s_\beta \tag{B.3}$$

For a symmetric three phase quantities, this is simplified to

$$\begin{cases} s_\alpha = \sqrt{\frac{3}{2}} \cdot s_a \\ s_\beta = \frac{1}{\sqrt{2}} \cdot \left(s_b - s_c \right) \end{cases} \tag{B.4}$$

This is further transferred into the rotating *dq*-frame, see Figure B.1, through the transformation

$$\vec{s}^{\,dq} = \vec{s}^{\,\alpha\beta} e^{-j\theta} = s_d + j s_q \tag{B.5}$$

which means that

$$\begin{cases} s_d = s_\alpha \cos\theta + s_\beta \sin\theta \\ s_q = -s_\alpha \sin\theta + s_\beta \cos\theta \end{cases} \tag{B.6}$$

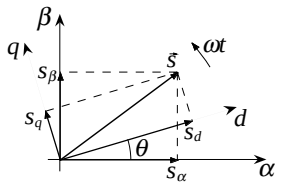


Figure B.1 The stationary and rotating reference frames.

Note that this means that the fundamental components of the three phase quantities are expressed as DC quantities in the rotating *dq*-frame. For a grid connected converter, the *dq*-system is oriented to the integral of the grid voltage vector. This implies that the direction of the grid voltage vector and the *q*-axis coincide. Hence, an easy way to calculate the transformation angle, θ, is from

$$\begin{cases} \sin\theta = -\dfrac{e_\alpha}{\sqrt{e_\alpha^2 + e_\beta^2}} \\ \cos\theta = \dfrac{e_\beta}{\sqrt{e_\alpha^2 + e_\beta^2}} \end{cases} \tag{B.7}$$

Note that this method is not suitable for implementation where disturbances, transducer offset and harmonics might interfere with the fundamental.

Vector controller

Current controllers for the *d* and *q* components are implemented in a similar way as the DC side current controller. However, in this case there are also cross coupling terms which appears as feed forward terms. Hence,

$$\begin{aligned} v_d^*(k+1) = K \cdot \left(\left(i_d^*(k) - i_d(k) \right) + \frac{1}{T_i} \cdot \sum_{n=0}^{k-1} \left(i_d^*(n) - i_d(n) \right) \right) - \\ -K_c \cdot \left(i_q^*(k) + i_q(k) \right) + e_d(k) \end{aligned} \tag{B.8}$$

$$v_q^*(k+1) = K \cdot \left(\left(i_q^*(k) - i_q(k) \right) + \frac{1}{T_i} \cdot \sum_{n=0}^{k-1} \left(i_q^*(n) - i_q(n) \right) \right) + \\ + K_c \cdot \left(i_d^*(k) + i_d(k) \right) + e_q(k) \tag{B.9}$$

where e denotes the power grid voltage and K_c is the cross-coupling gain. The gains and the integrator time constant, for dead beat current control, is in this case given by

$$\begin{cases} K = \dfrac{L}{T_s} + \dfrac{R}{2} \\ K_c = \dfrac{2\pi f L}{2} \\ T_i = \dfrac{1}{2} + \dfrac{L}{RT_s} \end{cases} \tag{B.10}$$

where f is the power grid fundamental. In the simulations the following set points or reference values are used for the AC side current controller

$$\begin{cases} i_d^*(k) = 0 \\ i_q^*(k) = -\left(\dfrac{v_{batt}(k)}{e_q(k)} \cdot i_{batt}(k) + \dfrac{v_{dc}(k)}{e_q(k)} \cdot i_{dc}^*(k) \right) \end{cases} \tag{B.11}$$

where DC link capacitor current reference is determined from the DC link voltage controller, discussed later on.

Symmetrisation

The dq-frame voltage reference values are transferred into $\alpha\beta$ -quantities and further into three phase quantities. In order to fully utilise the DC link voltage available, the three phase reference voltages are altered in such a way that the maximum and minimum instantaneous voltage reference values have the same magnitude, i.e. that their distance from the zero level are equal. This is achieved by calculating

$$v_z(k) = \frac{1}{2} \left(\max\left(v_a^*(k), v_b^*(k), v_c^*(k) \right) + \min\left(v_a^*(k), v_b^*(k), v_c^*(k) \right) \right) \tag{B.12}$$

The new reference values are given by

$$\begin{cases} v_{az}^{*}(k) = v_{a}^{*}(k) - v_{z}(k) \\ v_{bz}^{*}(k) = v_{b}^{*}(k) - v_{z}(k) \\ v_{cz}^{*}(k) = v_{c}^{*}(k) - v_{z}(k) \end{cases} \quad \text{(B.13)}$$

Therefore, this is called symmetrisation.

B.3 DC link voltage controller

In order to maintain the DC link voltage at the desired level, it has to be controlled. The deviation between the actual DC link voltage and its reference value, is multiplied with a gain giving a current reference according to

$$i_{dc}^{*}(k+1) = K_{dc}\frac{C_{dc}}{4T_{s}}\left(v_{dc}^{*}(k) - v_{dc}(k)\right) \quad \text{(B.14)}$$

In order to limit the current demanded by the DC link voltage controller, the constant included in the gain is selected as

$$K_{dc} = 0.01 \quad \text{(B.15)}$$

The DC link current reference value calculated above is added to the *q*-axis current reference. However, the low value of the gain, K_{dc}, in effect means that the DC-link voltage controller is turned off, at least for the short simulation time employed (20 ms). Instead, approximate initial current controller integral parts are calculated from the battery charger losses of previous simulations, to accommodate for the DC link voltage variations. This is done due to the fact that for the short simulation time used, the integral parts will not assume steady state conditions.

C

Differential equations

In this appendix a unified approach to use the differential equations of a resonant circuit in order to characterise its behaviour is presented. The obtained results can be used to calculate peak values, constraints on component values etc. An application example where the method is applied to the resonant DC link converter, is also given.

C.1 Method

A typical solution to the differential equations arising from a resonant circuit is

$$\begin{cases} u(\alpha) = A\cos(\alpha) + B\sin(\alpha) + D = E \\ v(\alpha) = -AC\sin(\alpha) + BC\cos(\alpha) = F \end{cases} \tag{C.1}$$

For a ZVS resonant circuit, u can be regarded as the voltage across the resonant capacitor and v as the corresponding capacitor current. A and B are determined by the initial values, for the particular mode of the resonant cycle. D is due to the stationary solution of the differential equation. E and F are the values of u and v, respectively at instant α. For a resonant circuit the resonance frequency, as well as the time, are part of α.

Since the capacitor current is the product of the capacitance and the time derivative of the capacitor voltage, the factor C in (C.1) is the product of the capacitance and the time derivative of α, in this case.

The equation system (C.1) above is substituted into

$$\begin{cases} \sin(\alpha) = \dfrac{BC(E-D) - AF}{\left(A^2 + B^2\right)C} \\ \cos(\alpha) = \dfrac{AC(E-D) + BF}{\left(A^2 + B^2\right)C} \end{cases} \tag{C.2}$$

This expression, together with the trigonometric identity

$$\sin^2(\alpha) + \cos^2(\alpha) = 1 \tag{C.3}$$

gives constraints on what simultaneous values of *u* and *v*, i.e. *E* and *F*, that are possible, according to

$$(E - D)^2 + \left(\frac{F}{C}\right)^2 = A^2 + B^2 \tag{C.4}$$

By using the obtained constraint above, one unknown final value of one mode of the resonant cycle can be calculated upon knowledge of the initial values and the other final value of the particular mode. By repeating this several times, an entire resonant cycle can be characterised. Furthermore, the necessary initial values needed to assure a certain final value can be calculated.

C.2 Application to the resonant DC link converter

The resonant DC link converter introduced in section 2.3 is selected as an example to show the application of the method previously described. Since only the behaviour of the resonant circuit is of interest here, the simplified converter circuit can be used, see Figure 2.16.

Usually, the resonant cycle is only piecewise linear, which means that it has to be subdivided into intervals where a certain set of differential equations and initial conditions are valid. These intervals are referred to as modes of operation. As the first mode of operation (mode 1), a natural choice is the link voltage ramp down interval, i.e. the part of the resonant cycle where the resonant link voltage has a negative derivative with respect to time.

For the resonant DC link, this mode of operation is characterised by the differential equations

$$\begin{cases} L_r \dfrac{di_{Lr}}{dt} + v_{Cr} = V_{dc} \\ i_{Cr} = C_r \dfrac{dv_{Cr}}{dt} \\ i_{Lr} = i_{Cr} + i_o \end{cases} \tag{C.5}$$

By assuming that the output current is constant during this mode, i.e.

$$i_o = I_{o1} \tag{C.6}$$

this system of ordinary differential equations can be rewritten as one second order differential equation

$$\frac{d^2 v_{Cr}}{dt^2} + \frac{1}{L_r C_r} v_{Cr} = \frac{1}{L_r C_r} V_{dc} \tag{C.7}$$

This differential equation has the solution

$$v_{Cr}(t) = A\cos\omega_r(t-t_0) + B\sin\omega_r(t-t_0) + V_{dc} \tag{C.8}$$

Here, A and B are constants depending on the initial values of the capacitor voltage and current, respectively. The characteristic angular frequency of the resonance circuit, ω_r, is given by

$$\omega_r = \frac{1}{\sqrt{L_r C_r}} \tag{C.9}$$

The capacitor current is expressed by

$$i_{Cr}(t) = -\omega_r C_r A\sin\omega_r(t-t_0) + \omega_r C_r B\cos\omega_r(t-t_0) \tag{C.10}$$

Assuming a continuously oscillating resonant circuit, i.e. without damping, gives the initial conditions for this mode

$$\begin{cases} v_{Cr}(t_0) = A + V_{dc} = 2V_{dc} \\ i_{Cr}(t_0) = \omega_r C_r B = 0 \end{cases} \tag{C.11}$$

The constants A and B are determined by the initial conditions, which means that the resonant link capacitor voltage and current are given by

$$\begin{cases} v_{Cr}(t) = V_{dc}\left(1+\cos\omega_r(t-t_0)\right) \\ i_{Cr}(t) = -\omega_r C_r V_{dc}\sin\omega_r(t-t_0) \end{cases} \tag{C.12}$$

Mode 1 is finished when zero resonant link voltage is obtained, which gives

$$\begin{cases} v_{Cr}(t_1) = 0 \\ i_{Cr}(t_1) = 0 \end{cases} \tag{C.13}$$

These values serves as initial conditions for the next mode of operation. It should be clear that in this case they are easy to calculate without the use of the previously shown method.

As soon as the zero voltage interval is entered a new converter switch state is set, if desired.

The zero voltage interval is somewhat special for this type of resonant link converter, in the sense that its duration can equal zero. This is due to the fact that a decrease in the output current, i_o, according to the new switch state of the converter implies that the resonant inductor L_r has excess energy stored, resulting in a positive, non-zero resonant link capacitor current occurring immediately after the output current change.

If, on the other hand the output current is increased, the link voltage is clamped to zero by the freewheeling diodes of the converter. At the same time, the inductor current is increased since the entire DC link voltage is applied across L_r. Mathematically this is expressed by the differential equation

$$L_r \frac{di_{Lr}}{dt} = V_{dc} \tag{C.14}$$

which have the solution

$$i_{Lr}(t) = i_{Lr}(t_1) + \frac{V_{dc}}{L_r}(t - t_1) = I_{o1} + \frac{V_{dc}}{L_r}(t - t_1) \tag{C.15}$$

The zero voltage clamping due to the freewheeling diodes is inhibited as soon as the resonant inductor current, i_{Lr}, reaches the level of the output current I_{o2}. This means that the resonant link voltage ramp up interval (mode 3) starts when

$$i_{Lr}(t_2) = I_{o2} \tag{C.16}$$

When analysing this circuit it is important to remember that the last expression is only valid if the output current is increased. Otherwise the link voltage ramp up interval starts immediately, i.e. when

$$i_{Lr}(t_2) = I_{o1} \tag{C.17}$$

One of the problems when analysing this circuit arises from this fact, since this results in different initial conditions for the resonant link capacitor current, depending on the output current change.

For mode 3, the differential equations of mode 1 are still valid, however with a new set of initial conditions.

The initial conditions in this case are dependent on whether the output current from the resonant circuit, i_o, has increased or decreased due to the new switch state of the converter. If the output current has increased, a zero voltage interval has been present prior to mode 3 and the initial capacitor current will equal zero. If the output current has decreased, the initial capacitor current will be non-zero and positive. For the latter case, it was previously stated that the duration of the zero voltage interval (mode 2) will be very short.

However, in both these cases the initial capacitor voltage equals zero, thus

$$v_{Cr}(t_2) = A + V_{dc} = 0 \tag{C.18}$$

Mathematically the first case is expressed as

$$i_{Lr}(t_2) = I_{o2} \tag{C.19}$$

$$i_{Cr}(t_2) = \omega_r C_r B = 0 \tag{C.20}$$

which gives

$$\begin{cases} v_{Cr}(t) = V_{dc}\left(1 - \cos\omega_r (t - t_2)\right) \\ i_{Cr}(t) = \omega_r C_r V_{dc} \sin\omega_r (t - t_2) \end{cases} \tag{C.21}$$

The maximum resonant link voltage is reached when the capacitor current equals zero, i.e.

$$i_{Cr}(t_3) = 0 \tag{C.22}$$

which gives

$$v_{Cr}(t_3) = 2V_{dc} \tag{C.23}$$

Here, the resonant cycle is completed for the first case. The second case is mathematically expressed as

$$i_{Lr}(t_2) = I_{o1} > I_{o2} \tag{C.24}$$

$$i_{Cr}(t_2) = \omega_r C_r B = I_{o1} - I_{o2} \tag{C.25}$$

This gives the solution

$$\begin{cases} v_{Cr}(t) = V_{dc}\left(1-\cos\omega_r(t-t_2)\right) + \dfrac{I_{o1}-I_{o2}}{\omega_r C_r}\sin\omega_r(t-t_2) \\ i_{Cr}(t) = \omega_r C_r V_{dc}\sin\omega_r(t-t_2) + \left(I_{o1}-I_{o2}\right)\cos\omega_r(t-t_2) \end{cases} \quad \text{(C.26)}$$

Also in this case the maximum resonant link voltage appears when the capacitor current equals zero. By using the described method, i.e. equation (C.4), the maximum voltage in this case is described by

$$v_{Cr}(t_3) = V_{dc} + \sqrt{V_{dc}^2 + \left(\frac{I_{o1}-I_{o2}}{\omega_r C_r}\right)^2} \quad \text{(C.27)}$$

This expression can be simplified to

$$v_{Cr}(t_3) = V_{dc} + \sqrt{V_{dc}^2 + \frac{L_r}{C_r}\left(I_{o1}-I_{o2}\right)^2} \quad \text{(C.28)}$$

In this case the maximum resonant link voltage becomes higher than twice the DC link voltage. This means that the previously assumed initial state for the resonant link voltage ramp down interval (mode 1) is not valid in this case. However, as seen in Figure 2.17, the initial conditions becomes valid after only one additional resonant cycle.

The VPC strategy

Another example is found by applying the method to the voltage peak control (VPC) strategy for the resonant DC link converter found in [46], [47]. The idea of this strategy is to perform the change of the switch state at such a resonant link voltage level that the maximum capacitor voltage always becomes close to twice the DC link voltage. This implies that some of the switching transitions are made at a resonant link voltage somewhat higher than zero.

However, since the VPC strategy is intended for the resonant DC link converter, the differential equations and their solutions found previously are still valid but with different initial conditions.

Consider the case when the output current i_o is supposed to decrease. Instead of allowing the capacitor voltage to reach zero, the change of converter switch state takes place at

$$v_{Cr}(t_1) = v_{Cr0} \quad \text{(C.29)}$$

The corresponding capacitor current, prior to the change of switch state, is depicted as

$$i_{Cr}(t_1^-) = i_{Cr0} \leq 0 \tag{C.30}$$

Equation (C.4) states that the relationship between v_{Cr0} and i_{Cr0} is given by

$$\left(\frac{i_{Cr0}}{\omega_r C_r}\right)^2 + \left(v_{Cr0} - V_{dc}\right)^2 = V_{dc}^2 \tag{C.31}$$

This is rewritten to

$$i_{Cr0}^2 = \left(\omega_r C_r\right)^2 \cdot \left(2V_{dc}v_{Cr0} - v_{Cr0}^2\right) \tag{C.32}$$

Since the capacitor is discharged at the resonant link voltage ramp down interval the solution is given by

$$i_{Cr0} = -\left(\omega_r C_r\right) \cdot \sqrt{2V_{dc}v_{Cr0} - v_{Cr0}^2} \tag{C.33}$$

The inductor current at this instant becomes equal to

$$i_{Lr0} = I_{o1} + i_{Cr0} \tag{C.34}$$

Since only the case when the output current, i_o, increases due to the change of converter switch state is considered, the ramp up interval (mode 3) starts directly. The initial resonant link capacitor voltage is

$$v_{Cr}(t_1) = A + V_{dc} = v_{Cr0} \tag{C.35}$$

The initial capacitor current for the resonant link capacitor voltage ramp up interval becomes

$$\begin{aligned} i_{Cr}(t_1^+) = \omega_r C_r B = i_{Lr0} - I_{o2} = I_{o1} - I_{o2} + i_{Cr0} = \\ = I_{o1} - I_{o2} - \left(\omega_r C_r\right) \cdot \sqrt{2V_{dc}v_{Cr0} - v_{Cr0}^2} \end{aligned} \tag{C.36}$$

The aim of the VPC strategy is to fulfil (note t_1=t_2)

$$\begin{cases} v_{Cr}(t_3) = 2V_{dc} \\ i_{Cr}(t_3) = 0 \end{cases} \tag{C.37}$$

If this is inserted into equation (C.4), the expression below is obtained

$$\left(\frac{0}{\omega_r C_r}\right)^2 + \left(2V_{dc} - V_{dc}\right)^2 = \left(v_{Cr0} - V_{dc}\right)^2 + \\ + \left(\frac{1}{\omega_r C_r}\right)^2 \cdot \left(I_{o1} - I_{o2} - \left(\omega_r C_r\right) \cdot \sqrt{2V_{dc} v_{Cr0} - v_{Cr0}^2}\right)^2 \tag{C.38}$$

This expression is rewritten to

$$2V_{dc} v_{Cr0} - v_{Cr0}^2 = \left(\left(\frac{I_{o1} - I_{o2}}{\omega_r C_r}\right) - \sqrt{2V_{dc} v_{Cr0} - v_{Cr0}^2}\right)^2 \tag{C.39}$$

By assuming

$$v_{Cr0} \leq V_{dc} \tag{C.40}$$

the expression is further simplified

$$\sqrt{2V_{dc} v_{Cr0} - v_{Cr0}^2} = \left(\frac{I_{o1} - I_{o2}}{\omega_r C_r}\right) - \sqrt{2V_{dc} v_{Cr0} - v_{Cr0}^2} \tag{C.41}$$

This is equal to

$$2\sqrt{2V_{dc} v_{Cr0} - v_{Cr0}^2} = \left(\frac{I_{o1} - I_{o2}}{\omega_r C_r}\right) \tag{C.42}$$

If both sides are squared, this expression becomes equal to

$$2V_{dc} v_{Cr0} - v_{Cr0}^2 = \frac{1}{2^2} \cdot \left(\frac{I_{o1} - I_{o2}}{\omega_r C_r}\right)^2 \tag{C.43}$$

which is rewritten to

$$v_{Cr0}^2 - 2V_{dc} v_{Cr0} + \frac{1}{4} \cdot \left(\frac{I_{o1} - I_{o2}}{\omega_r C_r}\right)^2 = 0 \tag{C.44}$$

According to the constraint (C.40), the only solution to this second order equation is

$$v_{Cr0} = V_{dc} - \sqrt{V_{dc}^2 - \frac{1}{4}\cdot\left(\frac{I_{o1}-I_{o2}}{\omega_r C_r}\right)^2} = \\ = V_{dc} - \sqrt{V_{dc}^2 - \frac{1}{4}\cdot\frac{L_r}{C_r}\left(I_{o1}-I_{o2}\right)^2} \tag{C.45}$$

In [46], [47] the corresponding expression is written as

$$v_{Cr0} = V_{dc}\left(1-\cos\left(\arcsin\left(\frac{Z_r\left(I_{o2}-I_{o1}\right)}{2V_{dc}}\right)\right)\right) \tag{C.46}$$

where

$$Z_r = \sqrt{\frac{L_r}{C_r}} \tag{C.47}$$

Here, the symbol names are fitted to the ones used previously in this section, which are not the same as the ones used in [46], [47].

Note that the VPC strategy is only used if the resonant link output current decreases due to the change in converter switch state, i.e. if $I_{o1}>I_{o2}$. Otherwise, the maximum resonant link voltage do not exceed twice the DC link voltage anyway.

C.3 Integration of the voltage equation

For some of the resonant DC link circuits the differential equations becomes linearly dependent. This implies that there will be one term in the inductor current expression which is linearly dependent in time. The reason for this is that the solution contains an integration of the capacitor voltage which has one constant term.

Assuming that the expression to be integrated, is written

$$u(t) = A\cos\omega_r(t-t_0) + B\sin\omega_r(t-t_0) + D \tag{C.48}$$

If the derivative of v with respect to time equals u, i.e. if

$$\frac{dv}{dt} = u \tag{C.49}$$

then v is found by integration of (C.48), thus

$$v(t) - v(t_0) = \int_{t_0}^{t} u(\tau) d\tau =$$

$$= \int_{t_0}^{t} \left(A \cos \omega_r (\tau - t_0) + B \sin \omega_r (\tau - t_0) \right) d\tau = \qquad \text{(C.50)}$$

$$= \frac{A}{\omega_r} \cdot \sin \omega_r (t - t_0) - \frac{B}{\omega_r} \cos \omega_r (t - t_0) + \frac{D}{\omega_r} \omega_r (t - t_0) + \frac{B}{\omega_r}$$

D

Inductor design

In this appendix, inductor design is reviewed. The design method used, is basically the same as the one described in [42]. Nevertheless, some of the steps are also found in [44].

D.1 Inductance

First, the inductance of a gapped iron core inductor, see Figure D.1, is derived.

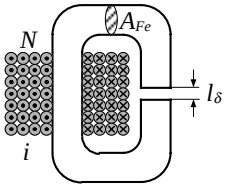


Figure D.1 Basic gapped iron core inductor.

According to [10], the inductance L is defined as

$$L = \frac{d\psi}{di} \tag{D.1}$$

where ψ is the flux linkage resulting from the current i. For a linear media, i.e. disregarding magnetic saturation and hysteresis in the case of an iron core, this is equivalent to

$$L = \frac{\psi}{i} \tag{D.2}$$

For the gapped iron core of Figure D.1, Ampère's circuital law gives

$$N \cdot i = H_{Fe} \cdot l_{Fe} + H_\delta \cdot l_\delta \tag{D.3}$$

Here, N denotes the number of winding turns, H_{Fe} and H_δ the magnetic field intensity in the iron core and air gap, respectively. The magnetic

flux mean path length is denoted l_{Fe} in the iron and l_δ in the air gap. The magnetic flux densities, B_{Fe} and B_δ, is defined from

$$\begin{cases} B_{Fe} = \mu_0 \mu_{Fe} H_{Fe} \\ B_\delta = \mu_0 H_\delta \end{cases} \tag{D.4}$$

where μ_0 is the permeability of air and μ_{Fe} is the relative permeability of the iron core material. Substitution into Ampère's circuital law gives

$$N \cdot i = \frac{B_{Fe}}{\mu_0 \mu_{Fe}} \cdot l_{Fe} + \frac{B_\delta}{\mu_0} \cdot l_\delta \tag{D.5}$$

Assuming uniform flux densities, the flux linkage is expressed as

$$\psi = N B_{Fe} A_{Fe} = N B_\delta A_\delta \tag{D.6}$$

where A_{Fe} and A_δ are the cross-sectional areas of the iron core and the air gap, respectively. Substituting the flux linkage into Ampère's circuital law gives

$$N \cdot i = \frac{\psi}{\mu_0 N} \cdot \left(\frac{l_{Fe}}{\mu_{Fe} A_{Fe}} + \frac{l_\delta}{A_\delta} \right) \tag{D.7}$$

Fringing flux in the vicinity of the air gap is neglected, which is equivalent to

$$B_\delta = B_{Fe} = B \Leftrightarrow A_\delta = A_{Fe} \tag{D.8}$$

This gives

$$N \cdot i = \frac{\psi}{\mu_0 A_{Fe} N} \cdot \left(\frac{l_{Fe}}{\mu_{Fe}} + l_\delta \right) \tag{D.9}$$

Rearranging this, gives an expression for the inductance according to

$$L = \frac{\psi}{i} = \frac{\mu_0 A_{Fe} N^2}{\frac{l_{Fe}}{\mu_{Fe}} + l_\delta} \tag{D.10}$$

In most cases the relative permeability of the iron core is high and the air gap long, i.e.

$$l_\delta >> \frac{l_{Fe}}{\mu_{Fe}} \tag{D.11}$$

which implies that the inductance is approximately given by

$$L = \frac{\mu_0 A_{Fe} N^2}{l_\delta} \tag{D.12}$$

D.2 Inductor core size selection

One of the first steps in the design of an inductor, is to select an appropriate core size. The problem of selecting the core size arises from the fact the geometrical properties of a core are composed in a wide variety of ways. It is thus desirable to select the core size in a formalised way, by assigning a general quantity to a core that is not depending on its actual geometrical shape, i.e. the ratio between the geometrical measures of the core. A common way to accomplish is by selecting the core based upon the desired area product. Here, this method is reviewed from [44].

The peak flux linkage is expressed as

$$\hat{\psi} = L\hat{i}_m = NA_{Fe}\hat{B}_m \tag{D.13}$$

where i_m is the magnetising current. The winding window A_w of a core is in the case of a single inductor coil expressed as

$$A_w = \frac{NA_{Cu}}{k_{Cu}} \tag{D.14}$$

where A_{Cu} is the winding copper conductor cross-sectional area and k_{Cu} is the copper fill factor, expressing how tightly wound the inductor coil is. The copper conductor RMS current I_{Cu} is expressed as

$$I_{Cu} = A_{Cu} J_{Cu} \tag{D.15}$$

where J_{Cu} is the corresponding current density. Substitution into equation (D.13) gives

$$L\hat{i}_m = k_{Cu} \frac{J_{Cu}}{I_{Cu}} \hat{B}_m A_w A_{Fe} \tag{D.16}$$

The area product, *AP*, of a core is defined according to

$$AP = A_w A_{Fe} \tag{D.17}$$

Substitution into (D.16) and rearranging the terms gives

$$AP = \frac{L\,\hat{i}_m I_{Cu}}{k_{Cu}\hat{B}_m J_{Cu}} \tag{D.18}$$

For an inductor, the copper conductor current and the magnetising currents are equal from a design point of view, i.e.

$$i_m(t) = i_{Cu}(t) \tag{D.19}$$

Thus, in this case the area product is written

$$AP = \frac{L\,\hat{i}_{Cu} I_{Cu}}{k_{Cu}\hat{B} J_{Cu}} \tag{D.20}$$

The last result is also found in [44]. If several inductor coils are wound upon a single core, like for a regenerative snubber [63], the expression (D.18) has to be slightly modified. This is done by assuming equal current density of each of the inductor coils. This means that the winding window area A_w is equally divided among the winding coils. Thus, the winding window area available for one coil is written

$$A_{w1} = \frac{A_w}{N_w} = \frac{N A_{Cu}}{N_w k_{Cu}} \tag{D.21}$$

where N_w is the number of windings, i.e. the number inductors, wound upon the core. Note that, similar to the case of a transformer, the inductance and both the magnetising and copper conductor currents must be referred to the same coil. The AP value for a core with several inductor coils thus becomes

$$AP = N_w \frac{L_k\,\hat{i}_{m,k} I_{Cu,k}}{k_{Cu}\hat{B}_m J_{Cu}} \tag{D.22}$$

where the inductance and currents are referred to coil k.

This is used for core selection of the clamping transformers used in the simulations of Chapter 5. Note that for the implementation of a clamping transformer, the magnetic coupling factor must also be taken into consideration. As discussed in Chapter 6, designing for a specified coupling factor is a by far stronger constraint than selecting core size based on the AP value. Thus, the method above can not readily be used for design of a clamping transformer.

D.3 Inductor design example

In this section one way of designing a certain type of inductors is given through an example. The inductor designed is actually used in the line side LCL-filter of the battery charger presented in [3]. The design is based on a tape wound C-core. An advantage of tape wound cores is that a high stacking factor is obtained even though a thin steel tape (0.025-0.3 mm) is used.

The specification of the inductor is given in Table D.1.

Table D.1 Inductor specification.

L	0.3 mH
I_{RMS} @ 1 kHz	120 A
I_{PEAK} @ 5 kHz	10 A
I_{PEAK} @ 10 kHz	5 A

Thus, the total RMS current is approximately given by the 1 kHz component, i.e.

$$I_{Cu} \approx 120 \text{ A} \tag{D.23}$$

By using four parallel conductors of rectangular cross-section, 3×5 mm, a RMS current density equal to 2 A/mm^2 is obtained. The absolute maximum magnetising, and thus copper conductor, current is calculated according to

$$\hat{i}_{Cu} = 120\sqrt{2} + 10 + 5 \text{ A} = 185 \text{ A} \tag{D.24}$$

To select core size, an initial guess of a suitable peak magnetic flux density has to be done. Here

$$\hat{B} = 0.35 \text{ T} \tag{D.25}$$

is selected. Also, a reasonable guess on the copper fill factor k_{Cu} must be made. A common value is 0.4. If this is used it is found that

$$AP = \frac{L\,\hat{i}_{Cu} I_{Cu}}{k_{Cu} \hat{B} J_{Cu}} = 2379 \text{ cm}^4 \tag{D.26}$$

The C-core TELMAG Su 150b, have geometrical properties according to Figure D.2 and Table D.2.

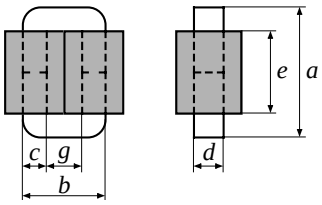


Figure D.2 Inductor based on a C-core. The winding (grey) is split into two parallel connected windings.

Table D.2 Geometry of the core Su 150b.

a	255.6 mm
b	150.2 mm
c	49.4 mm
d	76.2 mm
e	154.0 mm
g	50.0 mm

By including the stacking factor of the core with 0.1 mm tape, the iron core area is found

$$A_{Fe} = 0.968 \cdot 33.9 \text{ cm}^2 = 32.8 \text{ cm}^2 \tag{D.27}$$

The winding window area is approximated as

$$A_w \approx 15.4 \cdot 5.0 \text{ cm}^2 = 77.0 \text{ cm}^2 \tag{D.28}$$

Hence, the area product for this core becomes

$$AP = A_w A_{Fe} = 2527 \text{ cm}^4 \tag{D.29}$$

An initial guess, i.e. without air gap, of the number of winding turns required, is given by equation (D.13). Thus

$$N = \frac{L \hat{i}_{Cu}}{A_{Fe} \hat{B}} = 48 \text{ turns} \tag{D.30}$$

From equation (D.12), the total air gap length is calculated.

$$l_\delta = \frac{\mu_0 A_{Fe} N^2}{L} = 32 \text{ mm} = 2 \cdot 16 \text{ mm} \tag{D.31}$$

According to [42], the fringing flux factor, k_{FF}, is calculated as

$$k_{FF} = 1 + \frac{l_\delta}{\sqrt{A_{Fe}}} \cdot \ln\left(\frac{2e}{l_\delta}\right) = 2.265 \tag{D.32}$$

The fringing flux factor is then used to adjust the number of winding turns, to compensate for the fringing flux introduced in the vicinity of the air gap.

$$N = \sqrt{\frac{l_\delta L}{\mu_0 A_{Fe} k_{FF}}} = 32 \text{ turns} \tag{D.33}$$

The reduced turns ratio implies that the peak magnetic flux density becomes higher than expected. According to (D.13) it is given by

$$\hat{B} = \frac{L \hat{i}_{Cu}}{A_{Fe} N} = 0.53 \text{ T} \tag{D.34}$$

The peak flux density is calculated for each frequency component and then the iron core loss for each component is found from the manufacturer data sheets, which for 0.1 mm tape gives

$$\begin{cases} \hat{B}_{1\text{ kHz}} = 0.486 \text{ T} \\ \hat{B}_{5\text{ kHz}} = 0.029 \text{ T} \\ \hat{B}_{10\text{ kHz}} = 0.014 \text{ T} \end{cases} \Rightarrow \begin{cases} P_{Fe,1\text{ kHz}} = 141 \text{ W} \\ P_{Fe,5\text{ kHz}} = 10 \text{ W} \\ P_{Fe,10\text{ kHz}} = 6 \text{ W} \end{cases} \tag{D.35}$$

If minor loops are neglected, the total iron core loss is found directly summing the loss associated with each current component, i.e.

$$P_{Fe} = \sum_i P_{Fe,i} = 157 \text{ W} \tag{D.36}$$

Another iron core loss component, air gap loss due to fringing flux components being perpendicular to the tape surface, introduces additional eddy current losses. In [42], the air gap losses are calculated from the empirically derived expression

$$P_{\delta,i} = 388\, d\, l_\delta\, f_i \hat{B}_i^2 \tag{D.37}$$

The corresponding air gap losses, for the different current components, is found to be

$$\begin{cases} P_{\delta,1\text{ kHz}} = 212\text{ W} \\ P_{\delta,5\text{ kHz}} = 4\text{ W} \\ P_{\delta,10\text{ kHz}} = 2\text{ W} \end{cases} \tag{D.38}$$

Again, the total air gap losses are found by summing the components

$$P_\delta = \sum_i P_{\delta,i} = 218\text{ W} \tag{D.39}$$

which seems to be fairly high. To calculate the losses in the winding, referred to as copper losses, the mean length per turn, *MLT*, is calculated. For a C-core with a winding geometry according to Figure D.2, i.e. two coils, *MLT* is given by

$$MLT = 2c + 2d + 2g = 351\text{ mm} \tag{D.40}$$

The total winding resistance of the inductor is calculated at a winding temperature of 90 °C. At this temperature the resistivity of copper, ρ_{Cu}, equals $2.156 \cdot 10^{-2}$ Ωmm^2/m. The winding resistance is thus

$$R_{Cu} = \rho_{Cu} \frac{N \cdot MLT}{A_{Cu}} = 4.04\text{ m}\Omega \tag{D.41}$$

The copper losses is calculated from

$$P_{Cu} = R_{Cu} I_{Cu}^2 = 58\text{ W} \tag{D.42}$$

In order to estimate the temperature rise of the winding, its surface area is calculated according to

$$A_{T,Cu} = 4e(c+g) + 2e(d+g) + 4g(c+g) + 2dg = 0.1276\text{ m}^2 \tag{D.43}$$

Also, the iron core surface area is calculated

$$A_{T,Fe} = 4bc + 2bd + 4cf = 0.0676\text{ m}^2 \tag{D.44}$$

The total thermal flux density through the copper winding, is calculated as

$$\Psi_{T,Cu} = \frac{1}{A_{T,Cu}} \left(\frac{e}{b+e} P_{Fe} + P_\delta + P_{Cu} \right) = 2782\text{ W/m}^2 \tag{D.45}$$

In the same manner, the thermal flux through the iron core surface not covered by the copper winding, is calculated

$$\Psi_{T,Fe} = \frac{1}{A_{T,Cu}}\left(\frac{b}{b+e}P_{Fe}\right) = 1154 \text{ W/m}^2 \tag{D.46}$$

According to the literature, for example [42], [44], heat transfer is due to two physical processes, radiation and convection. Radiation follows the expression

$$\Psi_{T,rad} = 5.70 \cdot 10^{-8}\,\varepsilon\left(T_s^4 - T_a^4\right) \tag{D.47}$$

where ε is the emissivity of the surface, and T_s and T_a are the surface and ambient temperatures, respectively. Heat transfer by convection is according to [42], expressed as

$$\Psi_{T,conv} = 2.17\,F\left(T_s - T_a\right)^{\eta}\sqrt{p} \tag{D.48}$$

where F is an air friction factor, η is a factor depending on the shape and orientation of the surface and p is the relative pressure. Note that other text books presents different methods for calculating the convection heat transfer. The total heat transfer is given by the sum of the radiation and convection components, i.e.

$$\Psi_T = \Psi_{T,rad} + \Psi_{T,conv} \tag{D.49}$$

However, since the heat transfer by convection is complicated to model, heat transfer is instead calculated from experience. In [42] it is stated that the heat transfer is usually 55 % radiation and 45 % convection, which means that the total heat transfer can be approximated directly from the radiation component. The temperature rise at an ambient temperature of 40 °C, using this approximation, is shown in Figure D.3. In Figure D.3, another approximation is also shown where the temperature rise is calculated according to

$$T_s = T_a + \frac{\Psi_T}{\alpha_0 + k_\alpha T_a} \tag{D.50}$$

where the two constants are selected as α_0=12 W/m^2·°C and k_α=0.1 W/m^2·°C^2. As seen in Figure D.3, both methods give similar results.

If equation (D.50) is used, the temperature rise of the copper winding surface becomes

$$T_{s,Cu} - T_a = 174 \text{ }^\circ\text{C} \tag{D.51}$$

which is by far too high. The temperature rise of the iron core surface becomes

$$T_{s,Fe} - T_a = 72\ ^\circ\text{C} \tag{D.52}$$

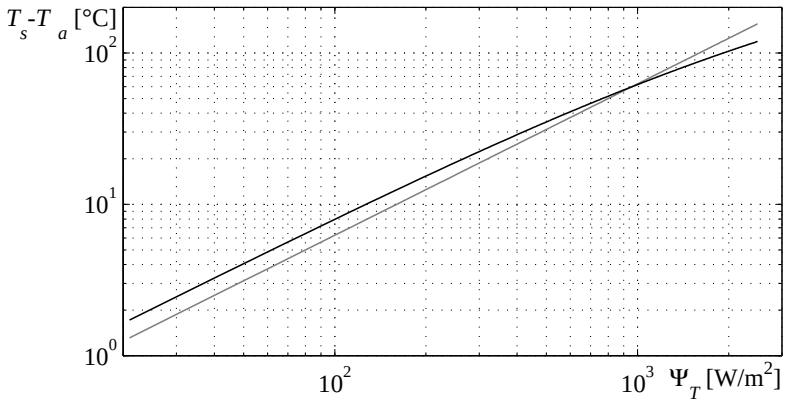


Figure D.3 Calculated temperature rise at an ambient temperature of 40 °C, based on radiated heat (black) and an approximate method (grey).

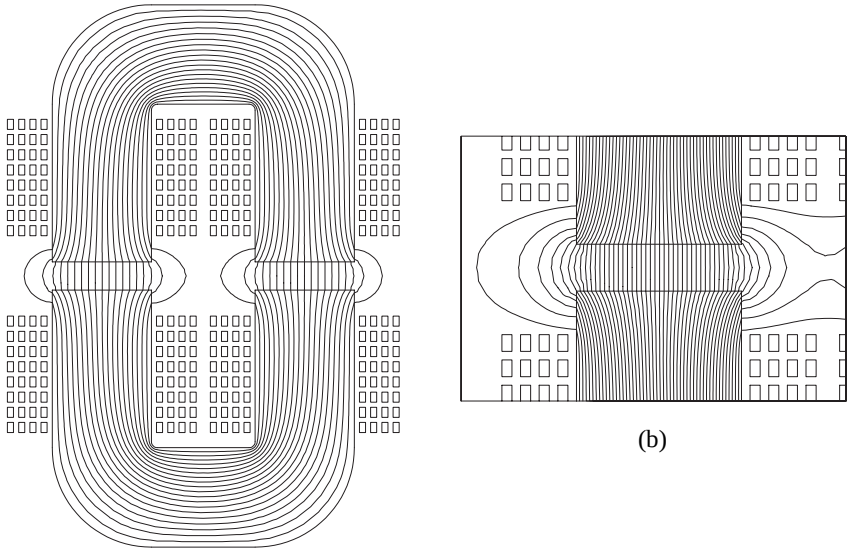
The calculated temperature rise of the copper winding surface is high, mainly due to the air gap losses. Often, the air gap losses are not included in the temperature calculation, which in this case gives

$$\Psi_{T,Cu} = \frac{1}{A_{T,Cu}}\left(\frac{e}{b+e}P_{Fe} + P_{Cu}\right) = 1074\ \text{W/m}^2 \tag{D.53}$$

$$T_{s,Cu} - T_a = 67\ ^\circ\text{C} \tag{D.54}$$

Another question to be asked, is how good the empirical air gap loss model is. However, when the inductor was implemented and tested, the copper winding surface close to the air gap was by far too hot, i.e. more than 130 °C.

To partially overcome this problem, the winding was split close to the air gap, in order to give a more efficient cooling of the iron core in the vicinity of the air gap, see Figure D.4. Another advantage gained by splitting the winding, is that the eddy currents induced in the copper winding, are reduced. To some extent this solved the problem, but fan cooling was also needed.



(a) (b)

Figure D.4 Magnetic flux lines (a) of the entire inductor, and (b) of the region around one of the air gaps.