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Abstract

In railway traffics the low friction between wheel and rail causes long braking distances, normally much longer than the driver's sight distance, i.e. if the driver starts the braking when a problem is discovered on the track it may be too late to brake the train. Therefore safe railway traffic can not only rely on the driver, there must also be a signalling or even a automatic surveyor system, which supervises the positions of different trains along the track and organise the traffic. Such a system uses train detection systems to check if a certain section of the track is occupied or not. Train detection systems can be disturbed by harmonics generated by the vehicle's drive system. Therefore it is necessary to be able to predict the line interference generated by a vehicle.

In this work, fast algorithms for calculation of harmonic from a traction drive system, based on three phase induction motors, are presented. The generation from both machine converters and line converters can be calculated. Both ideal and non-ideal commutations are taken into account.

The non-ideal commutations causes asymmetries, which can be compensated for. Following compensation methods are investigated in this work:

- Dead time compensation. The compensation method feeds back the differential between the integral of the inverter output voltage, or rather the output flux, and the voltage time area reference.
- Position asymmetry compensation. The compensation method is based on feed back of the DC-component in the machine inverter phase currents.
- Compensation of a remaining dc bias in Hall-effect current transducers. In the method, the fundamental current content in the DC-link current is fed back to the control system.

The compensation methods are found to be effective in most operating conditions.

Acknowledgements

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Contents

1 Introduction

In railway traffics the low friction between wheel and rail causes long braking distances, normally much longer than the driver's sight distance, i.e. if the driver starts the braking when he discovers a problem on the track it is too late to brake the train. The conclusions will be that the railway traffic can not only rely on the driver for the traffic safety, there must also be a signalling or even a automatic surveyor system, which can supervise the positions of different trains along the track and organise the traffic. Such a system exists, denoted "signalling system", but it can be interfered by the emission of harmonics from electrical traction drive systems.

This work presents solutions to some of the problems of guaranteeing safe railway traffic with electric trains when variable frequency AC-motor drive systems are introduced. Such drive systems generate undesired frequency components in the supply line, which can disturb the railway signalling system. The aim for the safety design is to guarantee that the interference does not cause a fatal disturbance. The signalling system as well as the traction system shares the rails for information and energy transfer:

Energy. The rails act as the current return path back to the substation for the power current. In a double rail system the current has the same directions in both rails and should be equally distributed between the two rails, i.e. the current is in common mode. In a single rail system only one rail is used as the current return path.

Information. To avoid collisions the signalling system uses train detection systems to indicate if a section of the track is occupied by a train. The standard train detection system, called a track circuit, is formed of one transmitter, the two rails and at least one receiver. The transmitter sends an electric signal in one rail to the receiver and the current returns to the transmitter in the other rail. The signalling current is in differential mode.

1.1 History

The track circuit was invented in the USA at the end of the last century, when all traffic was based on steam locomotives, and there was no risk of interference. With the introduction of electric traction the problems started. Originally this problem was solved by letting the train detection system use a certain frequency which was not generated by the vehicle drive system. This was possible in the days when AC track circuits were used on DC supplied lines where the traction motors were controlled by series resistor, and when DC track

circuits were used on AC-supplied lines where series motors were fed with a constant frequency adjustable voltage from a transformer. With chopper controlled drive systems it was still possible to handle the situation by letting the chopper frequency differ from the track circuit frequency.

However, with the introduction of variable frequency drive system, based on induction motors, the frequency spectrum, produced by the drive system, became more or less continuous. Interference with the same frequency as the train detection system frequency is occasionally generated.

1.2 Definitions and an overview of a DC supplied drive system

DC supplied lines are normally used in suburban traffic, but also for high-speed passenger trains and in locomotives, operating on main line in densely populated areas. The onboard electrical equipment is simpler compared to trains on AC-lines. On DC supplied lines the line voltage is normally low, 750 V, 1.5 kV or 3 kV. The line current will be correspondingly high, and the voltage drop along the line demands short distances between substations, but as the distance between the feeding substations in suburban traffic is short this is not a big problem.

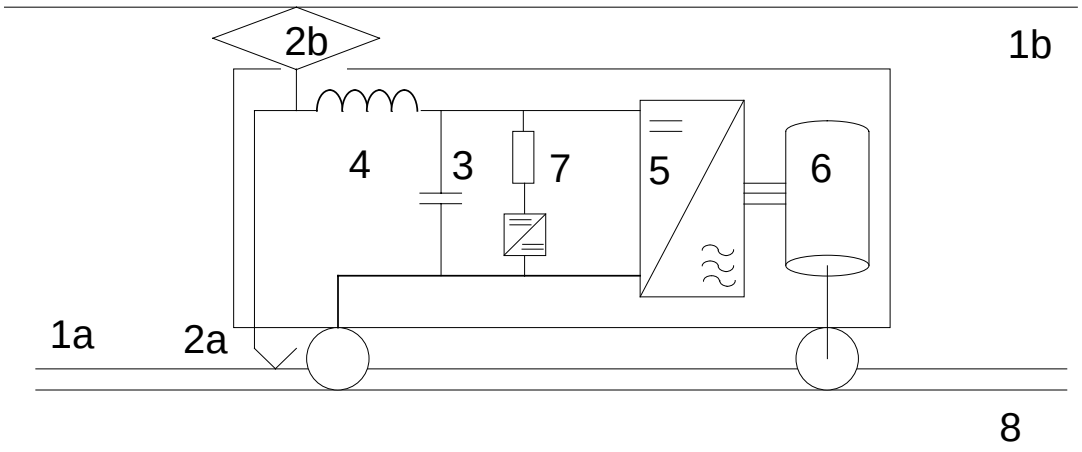

Figure 1-1 *A DC supplied AC-motor drive system with a brake chopper phase.*

The main power handling parts of a DC supplied AC-drive system in a railway vehicle are depicted in figure 1-1.

1. The power line is either (a) a third rail situated at ground level, or (b) an overhead catenary. The advantage of a third rail system is its low

resistance due to the large cross section area, compared to the resistance in an overhead catenary with a small cross section area. The low resistance allows long distances between feeding substations. Third rail systems are normally used in combination with heavy traffic like subways and main line trains, where the supply voltage is below 1 kVDC (typically 750 VDC). An overhead catenary is used for tram systems, since it is impossible to use a ground level third rail, as the tram traffic often is mixed with other traffic. At voltages above 1 kVDC, like 1,5 or 3 kVDC, overhead catenaries are always used to supply any kind of DC-railway traffic.

2. In third rail systems current shoes (2a) are used as the current collector, pantographs (2b) are used in systems with overhead catenaries.

3. The voltage source DC-link where the capacitor stabilises the DC-voltage feeding the machine converter.

4. The line inductor forms together with the DC-link capacitor a line filter, which reduces line interference.

5. The three-phase machine converter produces the desired motor voltage at the desired motor speed. As the motor speed and the motor torque varies during the train operation, the motor voltage and the motor frequency will also vary. This is the reason why the drive system generates a more or less continuous spectrum of line interference. The inverter does not produce a pure sinusoidal output voltage, but the voltage is PWM-modulated, and the generated interference originates from both the variable fundamental frequency and from the modulator switching frequency. Due to imperfections in the power converters, low frequency harmonics on the motor side will be reflected in the DC-link.

6. The modulated voltage does not only give rise to line interference, it also produces undesired torque pulsation, sound and vibrations in the three phase squirrel cage induction motor and in the mechanical gear. Also for this reason, it is desired to reduce the harmonic content.

7. When the drive system operates in braking mode, the power shall normally be generated back to the line, but if this is unreceptive, the braking power is converted to heat in the brake resistor(s). The brake chopper operates also in pulse width modulation mode and will generate line interference, but with constant frequency.

8. The current, including harmonics, leaves the vehicle via the wheels and returns to the feeding substation in the rails, where interference can occur with the track circuit frequency.

1.3 Definitions and an overview of an AC supplied drive system

AC-supplied lines are used in high-speed passenger trains and in locomotives, operating on main line. By means of transformers in substation an on board the train, the line voltage can be high, 15 kV and 25 kV are standard levels in Europe. The line current will be correspondingly low, and the voltage drop along the line will therefore be low, and the distance between substations can be long.

The main power handling parts of an AC supplied train with an AC drive system are shown in figure 1-2.

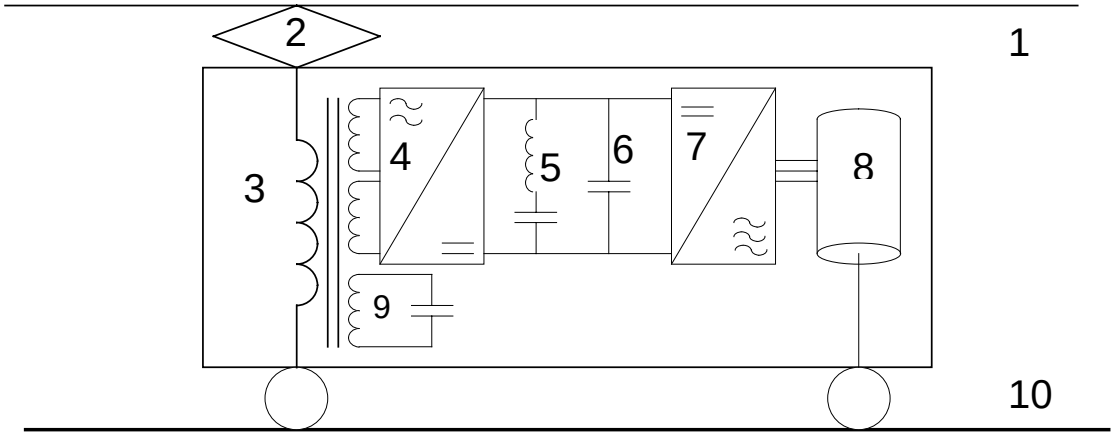

Figure 1-2 *An AC supplied AC-motor drive system.*

1. In AC-supplied systems, the power line is always an overhead catenary, due to the high voltage.

2. The current collector is a pantograph.

3. The main transformer

4. The line converter is a four quadrant (”4qs”) converter, with two bridges, which can consume and regenerate power at unity power factor. The line converter rectifies the line voltage to a DC-voltage in the DC-link. Since the line frequency is constant, the line converter does not generate a variable spectrum except for the machine converter produced DC-link

voltage ripple, which will be modulated to the line by the line converter. From this point of view, the line converter can be compared to a chopper drive system, where the switching frequency can be selected to give a harmless influence.

5. The second harmonic link is a shunt branch. The function of the line converter is to rectify the line voltage and generate a DC-voltage, simultaneously a current component with twice the line frequency will be generated. The second harmonic link is a low-impedance path at twice the line frequency, and therefore the second harmonic ripple in the DC-link will be low. The second harmonic link must be carefully tuned.

6. The voltage source DC-link.

7. The three phase machine converter produces the desired motor voltage at the desired motor frequency. As the motor speed and the motor torque varies during the train operation, the motor voltage and the motor frequency will change. The inverter does not produce a pure sinusoidal output voltage, instead the voltage is PWM-modulated. The generated interference originates from both the variable fundamental frequency and from the modulator switching frequency. In a DC supplied drive system, the continuous spectrum from the machine converter results in a continuous spectrum of line interference. In an AC-supplied drive system, the continuous spectrum will not reach the line, instead it will cause a continuous spectrum of DC-link voltage ripple, that the line converter modulates to a line side spectrum, with variable sidebands around the line converter switching frequency harmonics. Due to imperfections in the power electronics, low frequency harmonics will be produced into the line.

8. The modulated voltage does not only give rise to line interference, it also produces undesired torque pulsation, sound and vibrations in the three phase induction motor and in the mechanical gear. Also for this reason, it is desired to reduce the harmonic content.

9. The line filter reduces the line converter interference.

10. The current return path via the wheels and the running rails. In AC-supplied lines the running rails are only partly used as the current return. With some arrangements the return current is removed from the rails to a cable situated in the mast tops, but some of the generated line interference will still be found in the running rails, where it can interfere with track circuits.

1.4 The challenge

In modern AC motor driven trains, the spectrum from the machine converter is variable and the frequency of the harmonics depends on the actual vehicle speed. The spectrum from the line converter has varying amplitude, but as long as the frequencies are constant it is possible to avoid critical frequencies by choosing certain switching frequencies.

The continuous spectrum from the machine converter is the major problem in the low frequency area due to the switching pattern, restrictions like minimum pulse length. Besides the fact that the switching itself being non ideal, the actual switching will be delayed due to semiconductor component imperfections and due to snubbers, which makes the prediction more difficult. Therefore, this thesis is concentrated on machine converters and its non-ideal switching.

It is of fundamental importance that the line current spectra generated from the train does not interfere with the train detection system. The traction system has to be designed in order to avoid exciting critical frequencies for the train detection system, or the train detection system has to be designed in such a way that it is not sensitive for the spectra generated by the train.

Parts of the signalling system can be very old, and it has been designed without considering all the problems that new technique do cause. The signalling system, new or old, is also a part of the infrastructure. As Europe is becoming one region, trains will pass border between countries and therefore new traction drive systems must fulfil the demands of several signalling systems. The investments to install a new signalling system are normally very high. Therefore, the signalling system will not be changed when a new traction system is introduced.

One challenge is to be able to predict the emission from a drive system already at the design stage. Traditionally, it has been regarded that current in the rail or in the earth causes interference with the signalling system. However, as the switching in modern semiconductor based converters has become faster, other coupling mechanisms, e.g., inductive coupling, must be taken into account. Another challenge is the mitigation of those harmonics that are liable to disturb the train detection system. If the mitigation has to be done by passive filters, these have a tendency to become physically large. Thus, software based methods to obtain the same result ar of outmost importance.

1.5 The goal of the work

It is necessary to be able to predict the electromagnetic emission from the drive system already at the design stage in order to ensure that the generated level from a manufactured and commissioned vehicle will be lower than the detection level of the train detection system.

In the design stage of the drive system it is presumed that the induction motor is fed with a voltage which is based on an ideal modulation pattern, but due to imperfections in the modulator and in the power semiconductors undesired harmonics will be generated.

- The *first goal* is to construct and establish mathematical tools, which can be used to predict the emission of electrical interference from an electrical train, which has a traction drive system based on three phase induction motors. The algorithms shall also calculate the non-ideal effects as commutation delay, asymmetries etc., which always are present in a real converter.
- The *second goal* is to develop compensation methods by which it will be possible to reduce the generation of the undesired harmonics, which are generated due to the non-ideal effects in a real converter. The work is restricted to the motor inverter.

1.6 Main contribution

The contribution from the author to this thesis is divided in two areas:

- The calculation program Ascalp, see chapter 4, which is used for fast calculations of generations of harmonics from a drive system based on three phase induction motors. In DC supplied drive systems, the generation from the machine converter, including brake chopper phases, is calculated. In AC supplied drive system the harmonics from both the line converter and the machine converter are calculated. In the latter case also the cross-modulation, where the machine converter DC-link ripple by the line converter can be taken into account.

- Three compensation methods, which reduces the machine converter generated harmonics caused by non ideal commutations. One compensation method reduces the harmonic with six times the fundamental frequency that is caused by the so called dead time. Another method reduces the harmonics, that are caused by asymmetries.

1.7 The contents of the thesis

This paragraph is an overview of the content of the thesis. The first part is a description of today's signalling and traction equipment.

Chapter 2 is a description of existing signalling system. Especially the function and the interference mechanisms of different kinds of track circuits are described.

Chapter 3 is a description of traction drive systems based on three phase induction motors. Also a description of the drive system control is included.

Chapter 4 is mainly a description of the drive system as the source of line interference generation. In this chapter the calculation program Ascalp is described, which is used for calculation of the harmonic generation. In chapter 4 also the non-ideal commutation effects in the in the converter is classified.

In chapter 5, finally, compensation principles are presented, which can be used for correction of some of the non-ideal effects.

2 The Signalling System

As mentioned in the beginning of Chapter 1, a supervising system must be used in railway traffic. The supervising system controls that permission is given to one train to run on a certain part of a track section if, today automatic, it is ensured that the section is not occupied.

In the early days of railway traffic supervision was done by means of token. Each section of the track, normally the part between two stations, had its own, and only one, token, .i.e. a physical object used as evidence. A train was only allowed to run on a certain track section, when the train driver possessed the token. The token was given to him at the departure station and he left it at the arrival station, where he received a new token for the next track section. The token-based system works well when every second train runs in opposite direction. However when two trains after each other run in the same direction, the token must be brought back from the arrival station to the departure station by some other means.

When electricity was introduced in the society the problem was solved in an electrical way. In the station at each end of a track section a limited number of tokens were stored in a token instrument, one in each station. Both token instruments were connected electrically. When a token was taken from either of the two instruments, both became locked by electric means and it was not possible to take another token until the first token was returned to any of the instruments. In this way a number of trains can run in the same direction without any need for trains running in opposite direction. ([3] page 60).

When telephones and telegraphs were introduced, and today even radio, the ”token” could be brought as a message, but to do this the token had to be converted from a physical to a logical thing. Instead the risk of duplication of the token arose. To avoid that two trains simultaneously got a token for the same track part, the rules and regulations of token handling became very rigorous.

However, even with rigorous rules, there was always an uncertainty if the track section really was not occupied when a train was given permission to run.

A need of a train detection system, that could check if the track really was free became more and more obvious. In today’s complex railway traffic in and around big cities, the train detection system is a fundamental part of the computerised supervision and interlocking system.

Most train detection systems are based on track circuits, and therefore track circuits form the basis of modern signalling ([1] page 182), but have also become the most important victim of low frequency interference from the drive system.

The aim of all railway signalling systems is to prevent head-on and end-on collisions, prevent derailments and to allow trains to travel at maximum speed allowed for the line and for the vehicle. To achieve this, information about restrictions etc. is given to the driver by visual means, track side coloured lights or semaphore arms. Information can also be presented to the driver's cab by a display, often in combination with an audible signal and recently also as ATC ([2] page 5). The information from the train detection system is transferred to the supervising traffic control, where the track interlocking is done.

A signalling system has the following key elements ([2] page 5):

- A train detection system based on track circuits or axle counters
- Control of points and crossings (a point is where a track is split in two tracks or two tracks are merged into one single track)
- Interlocking of points and signals
- Indication to the driver by line side signals or cab signalling
- Enforcement of signal controls on the train with train stops or ATP (automatic train protection)
- Braking characteristics of the trains on the line

2.1 The track circuits

The main purpose for the track circuit is to prove that there are no other rail vehicles in a track section. When this is done, points may be operated and signals may be cleared for a train to move safely into the section. The second purpose for the track circuit is to detect the presence of a train within a certain section of the track. When this is being done the route ahead of the train will be locked in order to ensure the safe transit of the train ([1] page 182). The track circuit makes it possible to indicate on the train traffic surveyor's control panel the detailed position of a train along the track in order to keep the surveyor knowing where different trains are. The track circuits consists of a transmitter, a receiver and the two rails. The transmitter sends a signal to the receiver at the other end of the track section and the running rails are used as conductor to connect the transmitter to the receiver. If there is a train in the track section the signal will be short circuited by the wheel sets in the train and no signal reaches

the receiver. The track circuit is isolated from adjacent track circuits by means of insulated rail joints, that prevents the signal from interfering other track circuits. The insulated rail joints must not prevent the traction current (the power current) from returning to the sub station. There are three ways to achieve this:

In **single rail system** one rail, ”the traction rail”, is used for traction current. This rail has no insulated rail joints. The other rail, ”the signal rail”, is divided into insulated sections. A track circuit is formed of one of these sections and the corresponding part of the traction rail. Single rails system is used on tracks with such traffic, where the traction current has a small magnitude, i.e. traffic with low weight vehicles, the number of vehicles is low or where high voltage supply is used. The voltage drop in the running rail is therefore low, despite that only one rail is used as the traction current return. Single rail track circuits are normally not allowed at crossings, due to the current shunt in the surrounding earth. The ballast resistance is low due to salt etc. ([7] page 2).

In **double rail system** the traction current has high magnitude and is equally distributed between the two rails, the traction current is a common mode current. The signal current has different directions in the two rails and is therefore a differential mode current. Both running rails have insulated rail joints, see figure 2-1. Between adjacent track circuits an impedance bond is connected, which has a low impedance for common mode traction current and a high impedance for the differential mode signal current. The impedance bond allows the traction current to pass on to the feeding supply substation, but prevents the signal from reaching adjacent track circuits and from shunting the receiver. This system is used on the tracks with heavy traffic, where both running rail must be used as traction current return, in order to keep the voltage drop low.

Track circuit systems on continuously welded rails shall preferable not use insulated rail joints, and therefore jointless track circuits are used. In these kind of track circuits the signal current is prevented from passing to adjacent track circuits by means of a short circuit between the rails, normally a tuned LC series link. Adjacent track circuits use different frequencies and therefore each track circuit uses its own tuned link. At the short circuit a train can not be indicated, because a short circuiting wheel axles have no meaning there. Instead adjacent track circuits overlap, see figure 2-23.

Safety.

Fail safe. The signalling system must be designed to be fail safe. Any component or subsystem failure must lead to a default safety state which

ensures safety in all circumstances ([2] page 5), i.e. the track side signals shall turn to red. Electronic design and components must comply with the following: ([1] page 198): ”Components must be chosen to avoid any possibility of self oscillation, and all transistors and other active components must be continually switching, and failure, whether an short circuit or open circuit, must cause the relay to drop.”

Right side failure means that a not occupied track circuit is indicated as occupied. This situation is not dangerous but leads to traffic disturbance.

Wrong side failure means that an occupied track circuit is indicated as not occupied and it is of course a very dangerous situation. The design of a signalling system is to prevent a wrong side failure to happen. Coding is one traditional way to immunise a track circuit, i.e. to decrease the probability for a wrong side failure. Examples are the phase shift in an AC power frequency vane relay track circuit sections, or the switching between two frequencies in frequency shift key (FSK) track circuit sections. The problem of coding is that it reduces the probability for a wrong side failure to almost nothing, but the probability for a right side failure is increased, at least as long as the electric interference is unchanging, and this will lead to disturbed traffic.

Restrictive side. Stop is normally coded as no signal, and if the signal disappears because of an error, the train will automatically be stopped.

Response time. A track circuit can respond to transients, caused by sudden change in torque reference, by bouncing current collectors etc., because transients contain a wide band of frequencies. The most effective way to immunise the track circuit receiver against transients, is to make the response time as long as is possible concerning the interlocking and control system. A track circuit shall be ”fast to drop, slow to pick up”, i.e. it shall turn to red quickly but turn to green slowly.

2.2 Principal aspects of track circuit action

The track circuit is not occupied.

In the basic function the transmitter sends the signal to the receiver, and if the receiver receives the signal the track circuit is regarded to be not occupied, and another train is allowed to enter the track circuit. The green light is turned on if the train traffic surveyor allows traffic in the actual section and in the actual direction, see figure 2-1.

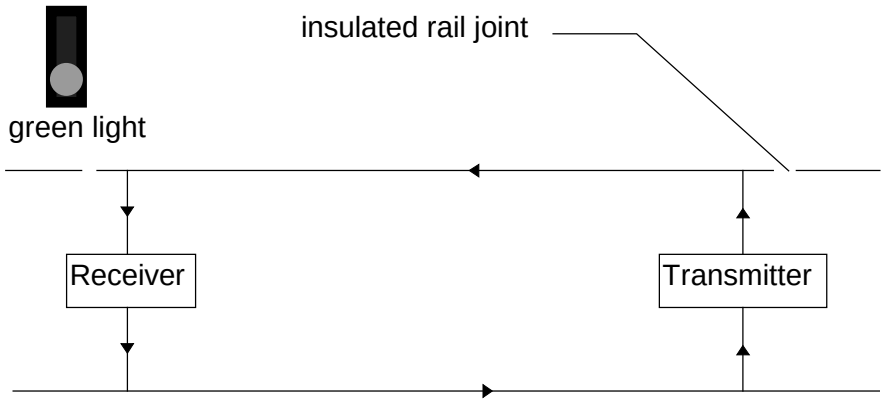

Figure 2-1. *An unoccupied track circuit.*

The track circuit is occupied.

When a train occupies the track circuit, the current signal will be short circuited by the train's wheel axles and the current will not reach the receiver, and the track circuit is regarded as occupied and another train is not allowed to enter the track section. The red light is turned on. See figure 2-2. An advantage with track circuits is that even a "dead" vehicle will be indicated, as long as it has the capability to short circuit the rails.

During work on the track, when an accident has occurred or at other occasions when a train is not allowed to enter a certain track section, a short circuit between the two rails can be done by means of a wire.

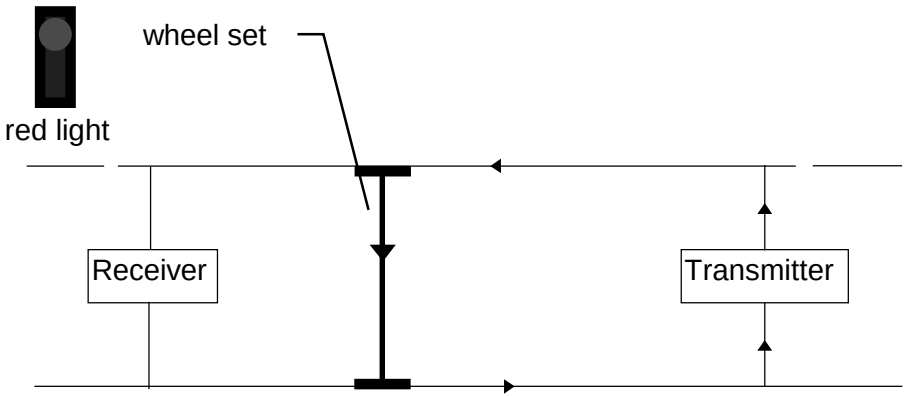

Figure 2-2. *An occupied track circuit*

Fail safe.

If there is a current interruption in the supply to the transmitter, to the receiver or in the track circuit the train detection system will not work, but as no current

signal reaches the receiver, the track circuit will automatically be regarded as occupied. The red light is turned on, see figure 2-3.

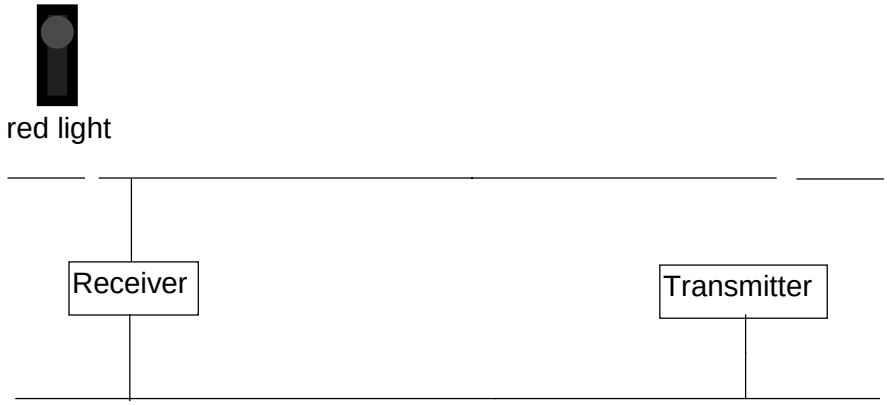

Figure 2-3. *A track circuit with the transmitter disconnected.*

Broken rail.

If one rail is badly broken, there is a derailment risk, and therefore a train is not allowed to run on that part of the track. Fortunately a broken rail is also a circuit interruption. As no current signal will reach the receiver, the track part will automatically be regarded as occupied. The red light is turned on. See figure 2-4.

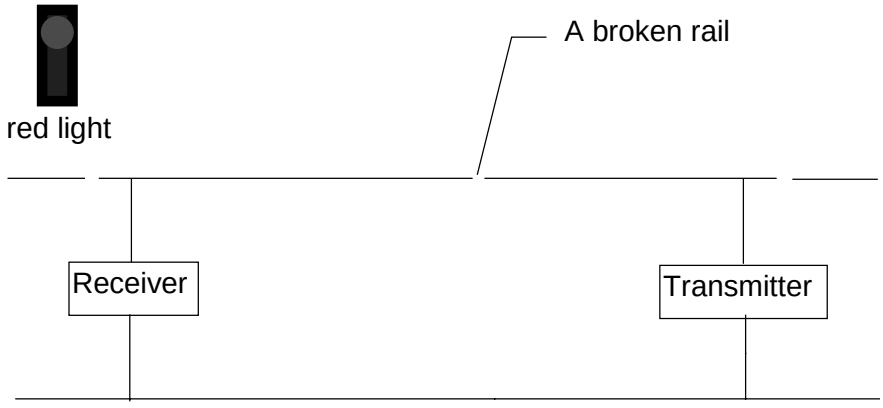

Figure 2-4. *A track circuit with a broken running rail.*

Disadvantage with poor rail isolation.

If the rails are not carefully isolated from earth shunts, some part of the current signal will be shunted to the other running rail via wet and dirty sleepers. If the track circuit is long enough all current signals will be shunted and no current is

left for the receiver. The track circuit will be indicated as occupied. The red light is turned on. See figure 2-5.

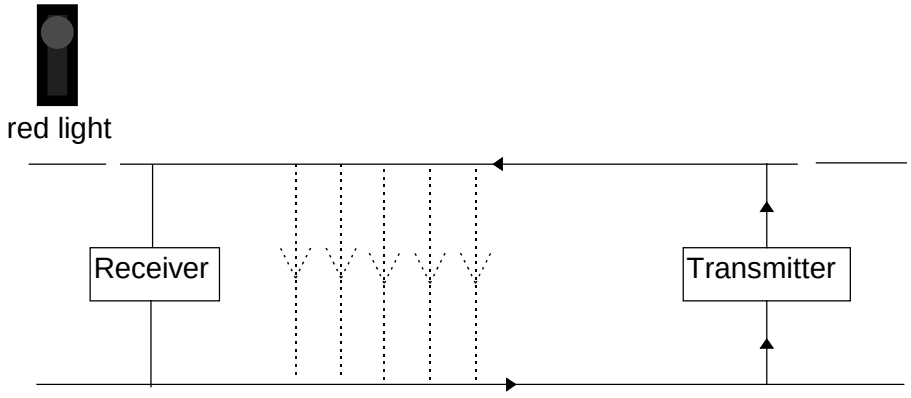

Figure 2-5. *A track circuit with bad isolation from earth.*

2.3 Track circuit interference mechanisms

In a machine converter fed AC-motor drive system the variable output frequency forms a problem. The design of the machine converter modulation pattern has the restriction to avoid generation of output frequencies which will appear in the line current as frequencies equal to and interfering with the track circuit frequencies. The machine converter is often combined with a brake resistor chopper. The brake chopper produces a constant frequency, which can be chosen to differ from the track circuit signalling frequency. The brake chopper frequency can however cross modulate the machine converter DC-link ripple frequencies and can give rise to unexpected interference frequencies.

Interference with the traction current return path in the running rails.

In double rail track circuit systems the traction current shall ideally be distributed equally between the two rails, the current is a common mode current. The track circuit receiver is not sensitive to common mode current in the rails and shall therefore not be sensitive to harmonics in the traction current. In single rail track circuits systems, the traction current return is by definition in differential mode, but the track circuit system shall be designed for this. However during abnormal situation like a broken impedance bond in double rail system or a broken rail in a single rail system a higher amount of traction current will pass the receiver and can then interfere with the track relay in a not

occupied track section. The light will turn to red, a right side failure. See figure 2-6.

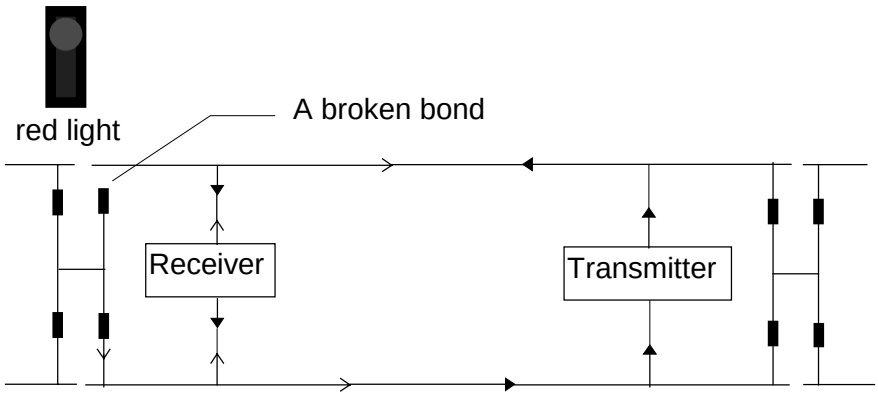

Figure 2-6. *A track circuit that is interfered by a fraction of a traction current from a adjacent track section which passes the track receiver where it cancels the track circuit current in a not occupied track section.*

Another situation, and much more serious, is shown in figure 2-7. The track section is occupied and the light should be red, but due to the broken bond a fraction of the traction current is forced to pass the receiver. In this case the frequency and phase content of the traction current is assumed to be such that it can trip the track circuit receiver. As the receiver responds to the signal, the light is turned to green, *a wrong side failure.*

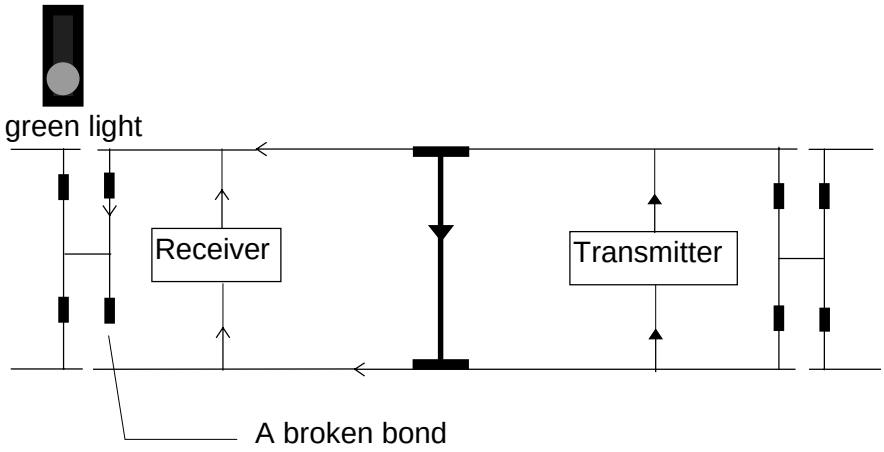

Figure 2-7. *A track circuit that is interfered by a fraction of the traction current that passes the track relay in an occupied track section*

Interference from earth current.

When tracks are not isolated from earth the current return from tracks in the vicinity can also be found in stray earth currents, which can pass the track circuit receiver in another track and interfere with track relay. Similar situations as those described in figures 2-6 and 2-7 can happen, either a not occupied track can be indicated as occupied or an occupied can be indicated as not occupied. An example of a wrong side failure is shown in figure 2-8.

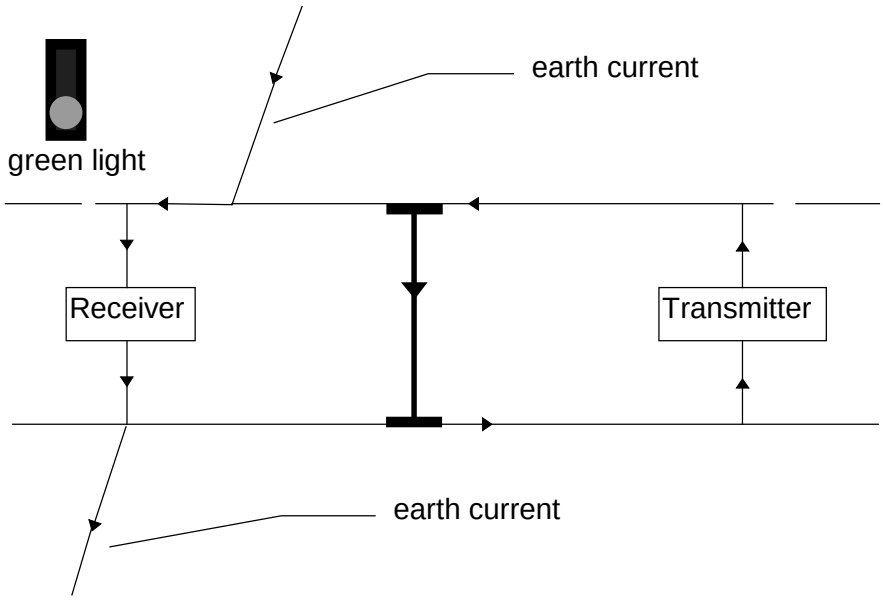

Figure 2-8. *A stray earth current with the correct frequency content passes the track circuit receiver*

Interference from a differential mode current induced by the third rail current.

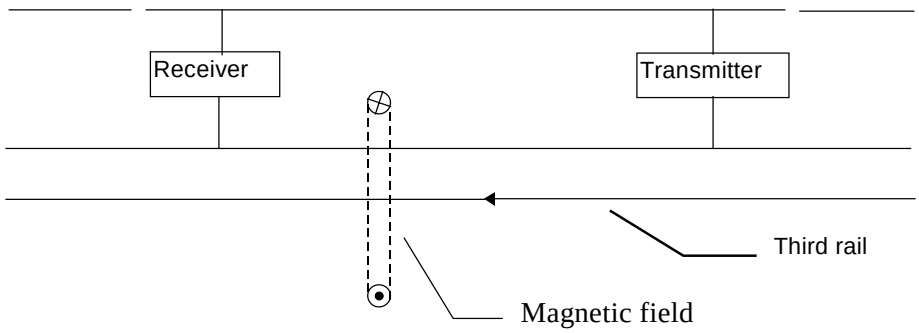

Figure 2-9. *Interference from a third rail or from an overhead power line to the track circuit.*

The traction current in the third rail, in the catenary or in an overhead power line will induce differential mode current in the track circuit, see figure 2-9. If the harmonic content in the traction current is high or the track circuit trip level is low, the track circuit can be disturbed.

Interference from a differential mode current induced by magnetic components on board the train.

Magnetic devices on board the train can induce a differential mode interference current in the track circuit, especially when they are mounted in the vehicle under-frame. The inductive coupling depends on the orientation of the magnetic axis of the component. The worst orientation is a vertical orientation where the magnetic field effectively is coupled to the track circuit, see figure 2-10.

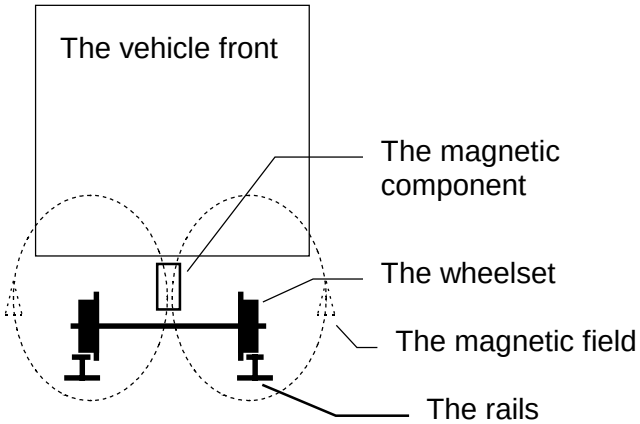

Figure 2-10. *Inductive interference from components with a vertical magnetic axis.*

An orientation of the magnetic component where the magnetic field can go down and return within the same track circuit will be a correct installation and no interference current will be induced..

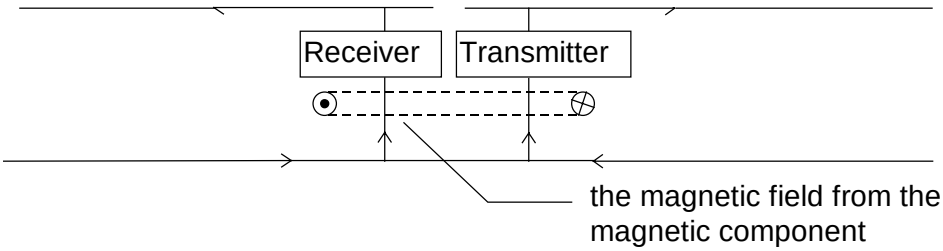

Figure 2-11. *A magnetic field which normally is safe can at the boundary interfere with two track circuits.*

The best orientation seems to be with the magnetic axis along the track. With this orientation the component can be installed anywhere in the underframe. But this orientation has one disadvantage; at the track circuit boundary the magnetic field can go down in one track circuit and return in the adjacent track circuit, and interference currents will be induced in both track circuits, see figure 2-11. Finally, the best orientation is obviously with the magnetic axis horizontal and perpendicular to the track direction. If this orientation shall be effective, the magnetic component must be installed above the midpoint between the two running rails, see figure 2-12.

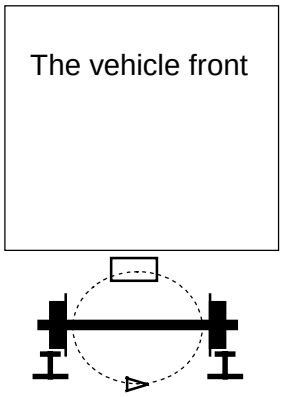

Figure 2-12. *Inductive interference from components with the magnetic axle horizontal and perpendicular to the track direction.*

2.4 Track circuits in reality

Track circuits signal frequencies vary from DC to some tens of kHz. In Sweden the number of different kinds are limited. On the AC supplied main lines DC track circuits are used, and SL, Stockholm Underground, uses 75 Hz AC track circuits. On the other hand, in UK almost any kind of track circuit can be found.

In this thesis four different kinds will be described: DC track circuits, power frequency AC track circuit, audio frequency AC track circuits and high voltage impulse track circuits.

DC track circuit.

DC track circuits are the simplest and least costly track circuits and should therefore be the first choice, as long as the track is not DC supplied ([8] page B1). The first track circuits, invented over a hundred years ago, used dry cells as electric energy supply. This system worked well in combination with steam locomotive technology. With the introduction of electrical traction this system

was easily disturbed. At this point the never ending story of traction current interference with track circuits started.

DC track circuits shall only be used on AC supplied lines, not on DC supplied lines. It is always a bad combination to have the same frequency in the track circuits as in the traction supply.

On AC supplied lines the voltage is high and consequently the current is low. Therefore a single rail system can normally be used. The track circuit is fed via a rectifier and an inductor is smoothing the current. A variable resistor is used to adopt the current level. The receiver is protected from interference AC current by means of a filter, see figure 2-13 ([1] page 196).

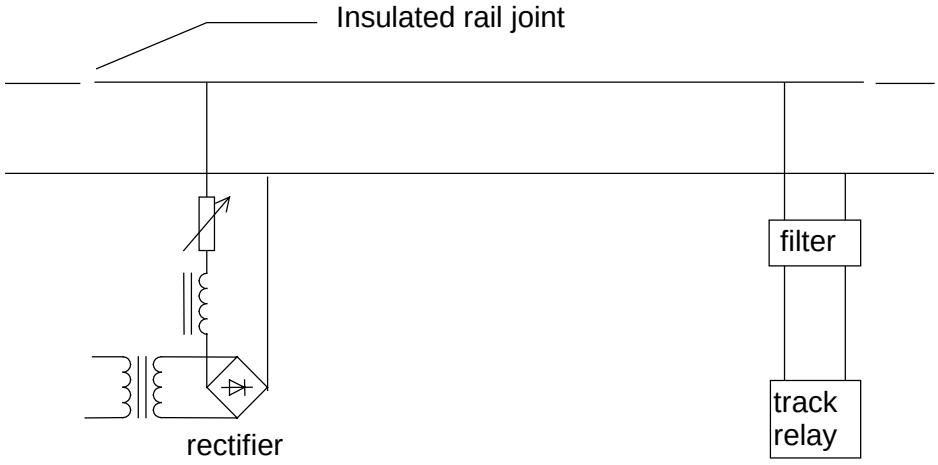

Figure 2-13. *A DC track circuit.*

The first DC track circuits with dry cells supply, had low signal levels in order to reduce the wear and number of batteries ([8] page B2). Low signal levels are one reason why they were not immune to disturbance. Modern DC track circuits are supplied from the public grid via rectifiers.

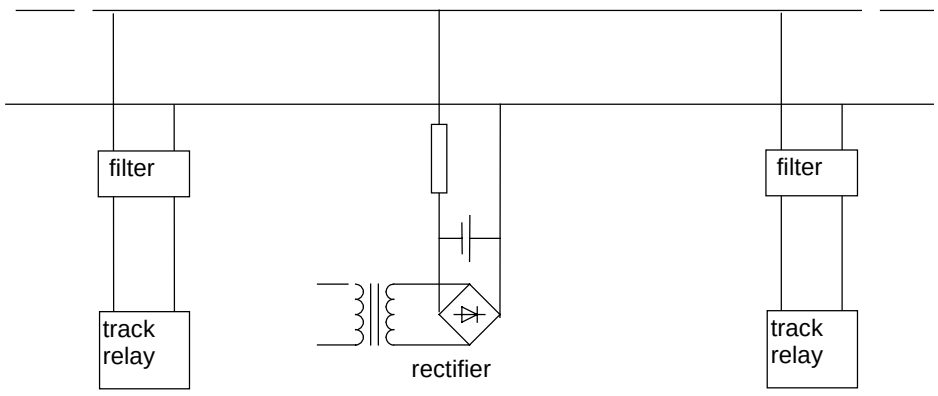

Figure 2-14. *A DC track circuit in areas with high geomagnetic currents.*

The Swedish National Railway Administration (”Banverket”) uses DC track circuits on the main lines. Batteries are integrated as a UPS-supply. Track circuits longer than 200 m have relays at both ends as protection against heavy geomagnetic currents ([2] page 128), see figure 2-14.

DC track circuits are only well suited in combination with AC supply. However as the AC supply itself can energise the track circuit relay, it can also be a source of interference, see figure 2-15 and figure 2-16.

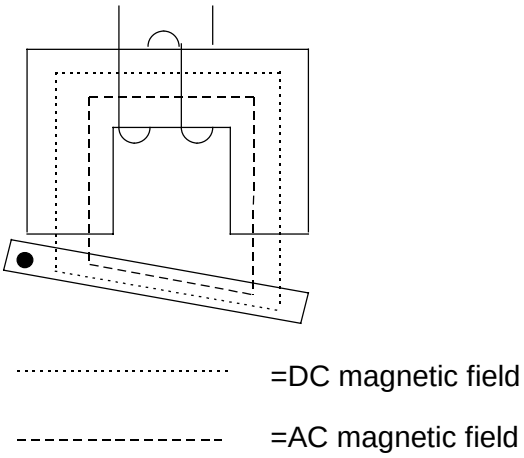

Figure 2-15. *Normal DC track relay action.*

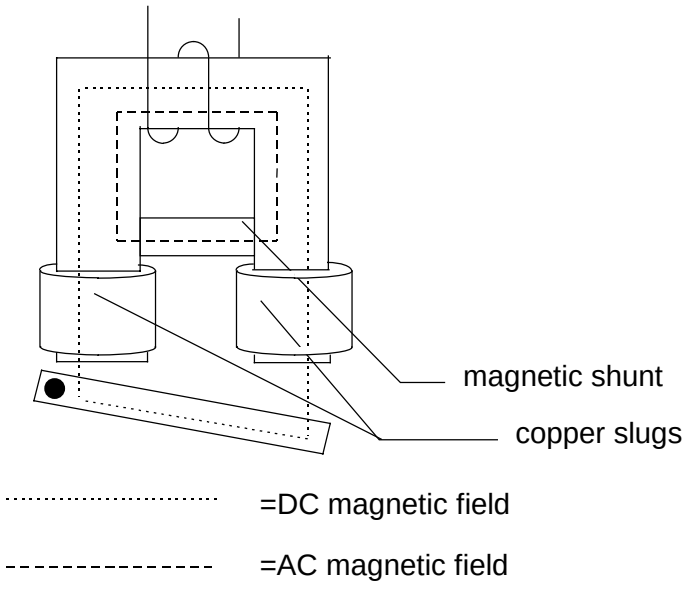

Figure 2-16. *An AC-immunised DC track relay.*

To immunise the DC track circuit, the magnetic circuit is changed. A magnetic shunt and two copper rings, ”slugs”, are put in the iron core. As an AC magnetic flux tries to penetrate the copper rings, a current is induced in them

and they become quite impermeable to the AC magnetic flux, which instead will pass the magnetic shunt. Only the DC magnetic flux can penetrate the rings and trip the track relay. ([1] page 194), see figure 2-16.

Important interference sources for DC track circuits are asymmetric commutations in the line converter, transformer inrush and pantograph-catenary arcing, which cause saturation in the main transformer. All three sources generate DC components, with duration long enough to trip the track circuit, [24] and [25].

Buried metal objects in the vicinity of the track can together with the soil form simple galvanic cells, which can cause corrosion to the object. To avoid this a cathodic protection system with opposite potential must normally be applied to the object. An earth current from the protection system can flow via the rails and interfere with the DC track circuit ([8] page B8). Also reinforced concrete sleepers can form a galvanic cell. The voltage is not high enough to compete with short circuiting wheel axles, but can keep a disconnected DC track circuit energised for several minutes ([8] page B10). These examples show the problem with low DC track circuit signals, and the solution is that the track should be isolated from ground, or if it has to be grounded, it shall only be grounded at one point within each track circuit.

Double element vane relay AC track circuits.

Initially, AC supplied track circuits were developed for use in DC supplied lines. They were fed from the public mains 50 Hz. However, with another frequency, for instance 83.3 Hz, AC track circuits can also be used on lines supplied with 50 Hz or $16^2/_3$ Hz. 83.3 Hz track circuits can also be used on DC supplied tracks if the DC supply contains too much 50 Hz harmonics, due to rectifier components asymmetries or if there is a high amount of 50 Hz vagabonding current.

In the double element vane relay a contact is closed when the vane is turned. The torque, needed to move the vane, is produced by eddy currents induced in the vane by the fluxes from two signals, called ”local” and ”control”. The phase shift between these signals shall be 90 degrees. If the two signal frequencies are unequal the torque will have a beat frequency and the relay will not operate. The relay will therefore only respond correctly to ”control” current of the same frequency as the ”local” current, and with the correct phase shift. The local signal voltage is typically 110 VAC, the control signal only 1-3 VAC. ([7] page 4). The electromagnetic amplifying action of the double element vane relay is both elegant and fail-safe. See figure 2-17 ([1] page 202-207).

Special measures are necessary in 50 Hz traction areas to prevent the supply to the local coil of the relay being disturbed by 50 Hz current. The ”local” supply for relays can demand specified relay rooms, can be screened or can use 50 Hz earth leakage current detection equipment.

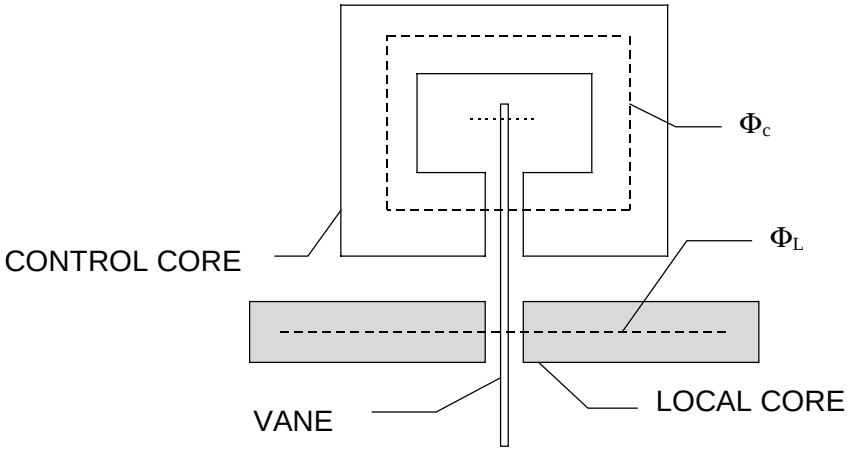

Figure 2-17. *A double element vane relay AC track circuits.*

The control signal shall be connected to the running rail via a capacitor or an inductor in order to get the 90 degrees phase shift, see figure 2-18.

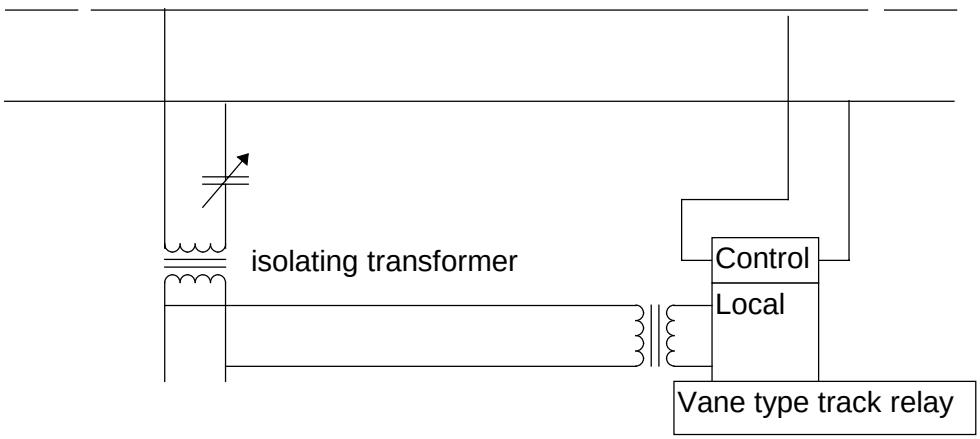

Figure 2-18. *Single rail double element vane relay track circuit.*

The capacitor is preferred in order to avoid transformer saturation due to DC current. The capacitor must be of an adjustable type in order to get the correct phase shift with varying rail and ballast impedance.

In double rail double element vane relay track circuit systems, adjacent track circuits are connected with impedance bonds, see figure 2-19. The impedance

bond iron core shall have an air gap to avoid saturation when a DCsupply traction current is not equally distributed between the two rails. Otherwise the impedance bond will act as a short circuit between the rails.

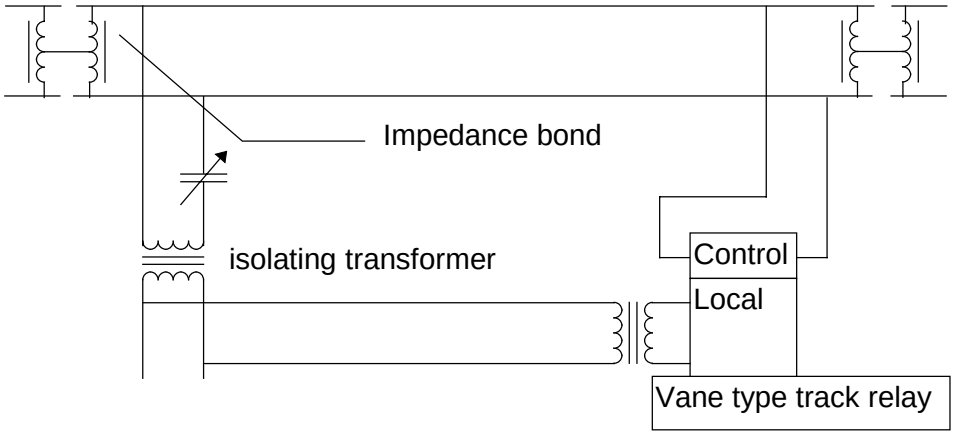

Figure 2-19. *Double rail double element vane relay track circuit with impedance bonds.*

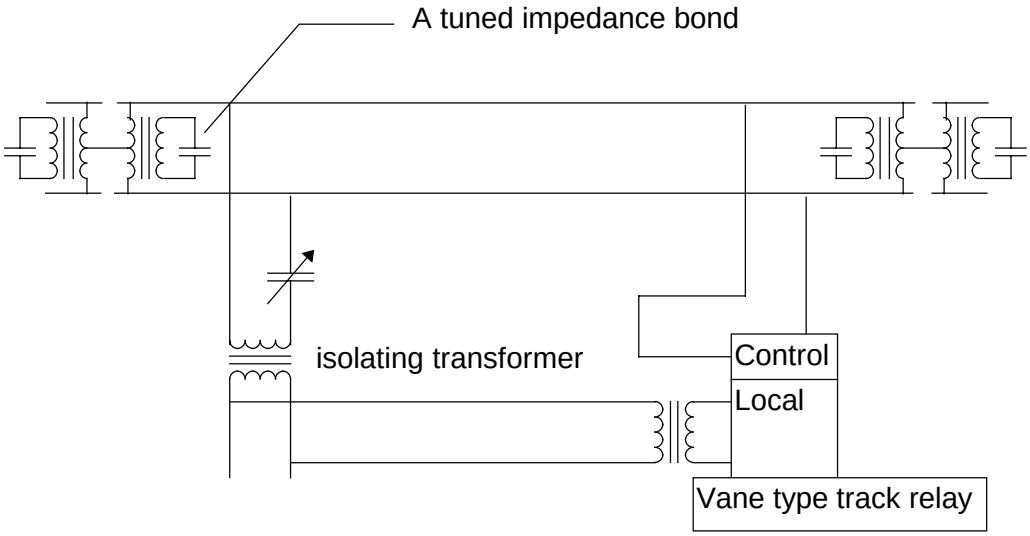

Figure 2-20. *A tuned impedance bond.*

The impedance characteristics of the track circuit can be improved by tuning the impedance bond. With a capacitor connected in parallel to the impedance bond, the impedance between the two rails can be made resistive, and the total impedance can be raised allowing longer track circuits, see figure 2-20.

With an auto coupled impedance bond the track circuit can be fed with higher voltage, and the track sections can be made longer, see figure 2-21.

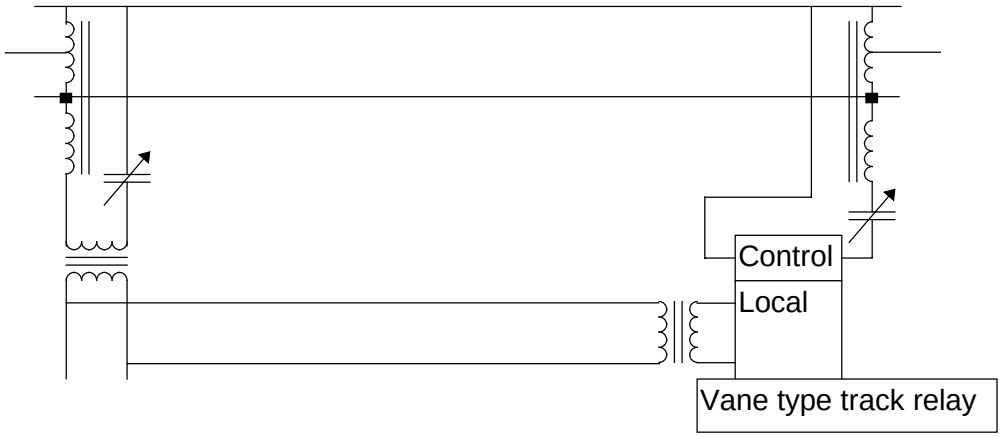

Figure 2-21. *A double element vane relay track circuit with auto coupled impedance bond.*

Tuned reed track circuit

Tuned reed track circuit can be used on both DC and AC supplied tracks and also on non-electric tracks where long track circuits (tunnels for instance) are required. Generally they can be used on the same kind of tracks where double element vane relay track circuits are used, see figure 2-22. ([1] page 213). A reed track circuit is characterised by a pair of mechanically tuned reed filters, one reed filter in the transmitter and one reed filter tuned to the same frequency in the receiver. A coil mechanically excites the reeds, and the reed filter can be tuned to a considerable precision and they have a high Q-value. The transmitter has an oscillator and a feed amplifier, with the reed filter in the feed back loop. The output from the amplifier is fed to the track via a LC-filter. One purpose for the LC filter is to prevent traction surges and other interference from back feeding the transmitter that could cause saturation and/or damage.

The receiver has an LC-filter in series with the reed filter and a relay amplifier, which operates a DC-relay. The reed frequency band can lie as close to each other as 3 Hz. The typical reed frequency bands for 50 Hz traction supply are 363, 366, 369, 372, 375 and 378 Hz ([23]). The use of different frequency band for adjacent track circuits gives freedom from faulty operation due to insulated joint failure. In fact reed track circuits can be used as a jointless track circuit on continuously welded tracks.

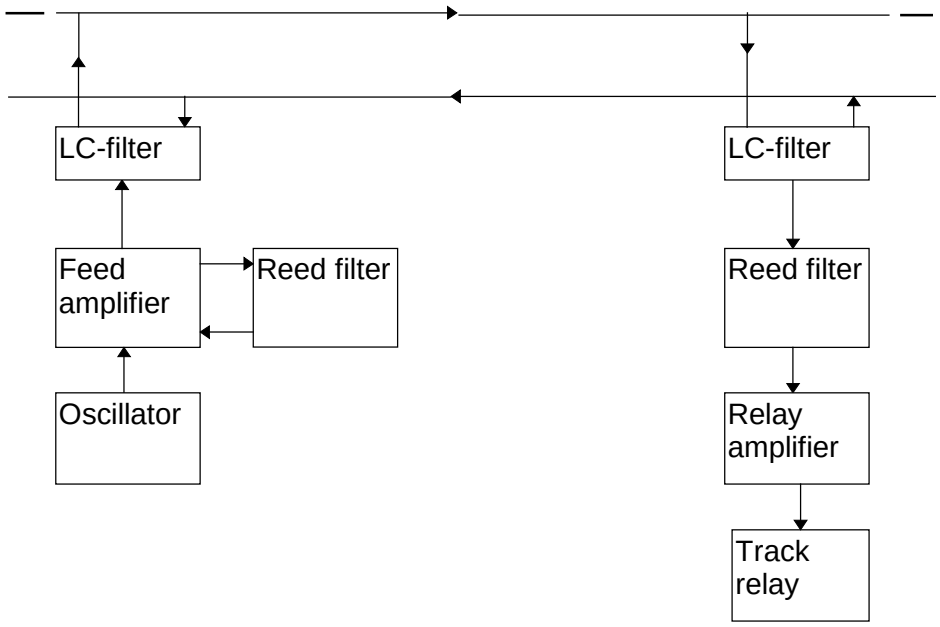

Figure 2-22. *A tuned reed track circuit.*

Jointless track circuits.

When continuously welded rails are used, it is impossible to use insulated rail joints. Instead jointless track circuits shall be used, which can be of either voltage or current operated type. They are normally operated in the audio frequency band.

This technique involves an oscillator and amplifier at the feed end. The frequency signal must be filtered and amplified at the receiver end before it can operate the track relay. By the use of suitable fine tuned filters, either electrically or mechanically tuned, crosstalk is avoided. Adjacent and parallel tracks should use different frequencies. ([1] page 215)

In track circuits with insulated rail joints the end of a track circuits is defined by the insulated joint. In jointless track circuits, a short circuit between the two rails will instead act as a definition of the track circuit boundary. This is of course a contradiction. How can a short circuit be used, when the presence of a train is indicated by the short circuiting wheel axles? However if the boundary short circuit is situated a certain distance from the receiver, it is still possible to send enough current through the receiver to make the track relay to pick-up. As long as the short circuiting wheel axles are not too close to the boundary short circuit a train’s presence can be indicated. However when the train gets close to the boundary, the wheel axle’s short circuit has little impact on the receiver current and the train’s presence can not be indicated.

To solve this problem two adjacent track circuits, A and B in figure 2-23, have different frequencies and the track circuits overlap. B's track circuit starts before A's track circuits finishes, i.e., when the wheel axles, still within A's track circuit, are close to A's boundary short circuit, their presence cannot be detected by A's track circuit. Instead its presence will be detected by B's track circuit. The boundary short circuit can not be a real short circuit, instead it is realised as a series LC-filter, tuned to the track circuit frequency, i.e., at the track circuit boundary two such LC-filters are present, one for track circuit A and one for track circuit B. See figure 2-23 where the voltage operated Aster "Type U" track circuit is depicted. This track circuit is a typical example of an audio frequency jointless track circuit ([1] page 219).

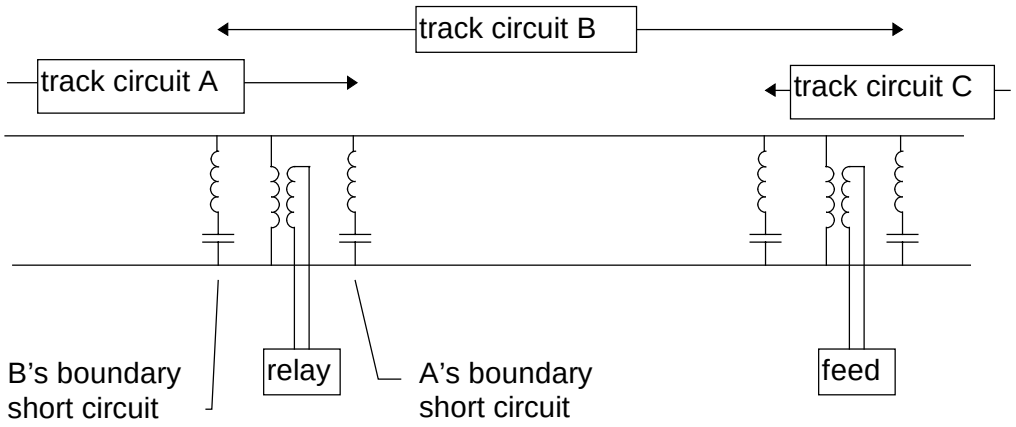

Figure 2-23. *Aster "Type U" jointless track circuits.*

Type TI21 Track Circuit is designed to be used on both AC and DC supplied tracks and also on non electrified lines([9] page B2). It can be used on both jointless and joint track. It is a voltage operated track circuit, similar principle as the Aster 'U' track circuit, but with some improvements. The equipment has great immunity to high values of interference signals. ([2] page 135).

The principle operation of the track circuit is to operate with FSK, "frequency shift key". The audio frequency carrier signal shifts between two frequencies, 34 Hz apart, and the modulation frequency is 4.8 Hz. The reason for two frequencies is to immunise the track circuit against interference. Both signals must have correct modulation frequency and both must be detected by the receiver. Otherwise it is regarded to be an interference and the track side signal turns to red.

The frequency difference 34 Hz is chosen for one reason: If the lower of the two frequencies is interfered by one modulated 50 Hz harmonic, the next higher 50

Hz harmonic shall not be able to interfere with the higher of the two frequencies. The TI21 track circuit system uses 8 different carrier frequencies, each modulated +/-17 Hz. Adjacent track circuits on the same track uses two different carrier frequencies. However also tracks running side by side must use different carrier frequencies due to earth currents. Thus a single track needs two, a double track needs four and four tracks need eight carrier frequencies([9] page B2).

The TI21 transmitter consists of a 4.8 Hz multivibrator, which modulates the carrier frequency oscillator. The modulated signal is amplified and fed to the track via a transformer, for matching and isolation purpose, and a filter. In the TI21 receiver, the signal first passes a transformer. By means of filters, the signal is then split into two parallel branches for each FSK frequency. The signals in the two branches are demodulated to two anti phase square wave signals. Both must be present if the receiver shall pick up. The relay picks up after two seconds, but it drops in a few milliseconds ([9] page B4).

HVI (high voltage impulse) track circuits.

HVI track circuits operate with 50 to 100 V amplitude pulses. These track circuits are used on track with low traffic or with old vehicle traffic, where the railhead can have a thin film of rust and/or dirt, which destroys the electrical contact between the rail and the wheels. The voltage peaks are high enough to penetrate the film.

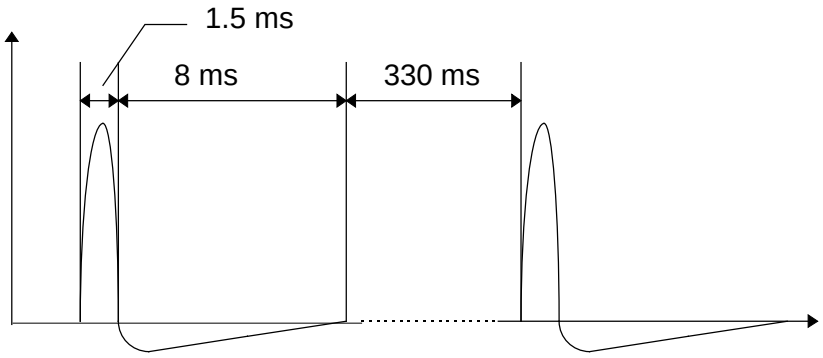

Figure 2-24. *The HVI track circuits pulses.*

The pulse is asymmetric where the positive amplitude is seven times the negative amplitude. The duration of the positive peak is 1.5 ms and the duration of the negative pulse is 8 ms. The repetition frequency of the pulses is only 3 Hz ([10] page B2), see figure 2-24.

HVI track circuits are immune to DC since both the transmitter and the receiver are connected to the track via transformers. The receiver is designed to recognise the asymmetric HVI pulse, and therefore it is immune to AC

interference signals that has a symmetric wave form (except under transient conditions) ([10] page B3).

2.5 Onboard signalling system for Automatic Train Control system (ATC)

One disadvantage with track side signalling systems is that there is no safety system which handles the problem when the train driver passes a red light signal. Also during stress, the driver can hesitate whether the latest signal he passed was ”red” or ”green”. At traffic jam the speed of the vehicles should be reduced in order to keep the traffic flowing. This can be solved with an ATC (automatic train control) system, which also includes an onboard presentation system where the information is displayed to the driver in the driving cab. Besides when the information is onboard the train it can be used to automatically apply the emergency brake of the train if the drivers fails to act correctly.

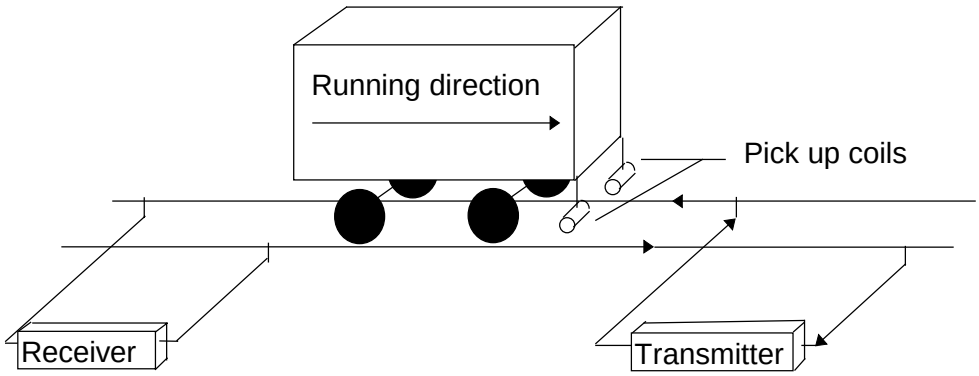

Figure 2-25. *An ATC system with pickup coils at vehicle front and with the information coded into the track circuit current.*

Until now we have regarded the track circuit signal current as being without extra information. However in **low frequency ATC system** the current is coded with information about the maximum allowed train speed, and after being picked up by the train the information can be presented to the driver. Just above each rail at the front end of the train, two pick up coils are mounted, where they pick-up the magnetic field from the track circuit current in the two rails. The output signal from the two coils are differentially connected, and they are therefore only sensitive to the differential mode signal current and insensitive to the common mode traction current, see figure 2-25.

The pick up coils can also pick up interference from other sources. The motor current in the motor cables can be inductively coupled to the coils. If the cables are not routed in symmetry to the coils, e.g. the motor cables can be more close to one of the coil than to the other, the interference from the motor cables will be picked up and the ATC system can be disturbed, see figure 2-26. The most effective solution to this problem is to twist the motor cables and to route them along the vehicle centre axle.

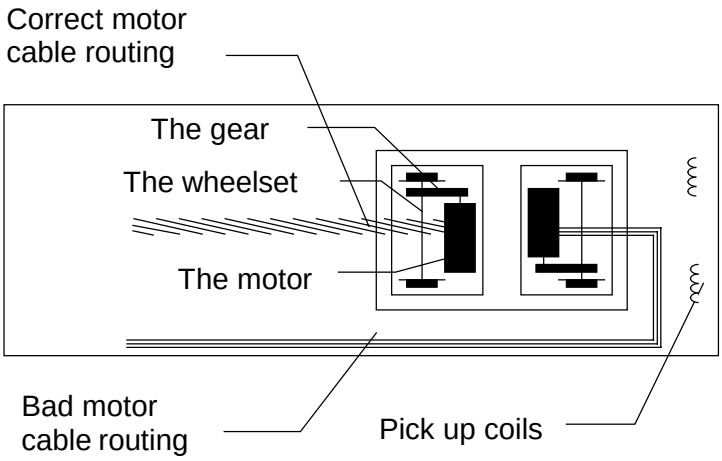

Figure 2-26. *Inductive interference from motor cables to pick up coils on board the train .*

In **audio frequency track circuits ATC system** the amount of information can be increased. The Swedish National Railway Administration, responsible for the main line track system uses a **radio communication ATC**-system which sends information from a micro-wave transmitter between the rails up to an antenna onboard the train. The consequence of the use of such a system is not taken into account in this thesis.

3 The Traction System

In this chapter, the traction system, depicted in figure 3-1, will be described. Traction is the action of drawing or pulling a vehicle over a surface by motor power. The traction system consists electrically of the substation, of the transmission line and of the vehicle drive system.

Both the DC and AC supplied drive systems, based on three phase induction motors fed from a machine converter will be studied in this work while DC motor trains are excluded. Special attention is paid to the DC supplied drives system, since the variable current spectrum will reach the line directly and interfere with the track circuits of the signalling system. Such a traction system often includes brake chopper phases. This kind of traction system is very common in metro traffic, of which Stockholm ”T-bana” (Underground) is one example.

The converter can either use GTO thyristors in combination with snubbers or use snubber-less IGBTs.

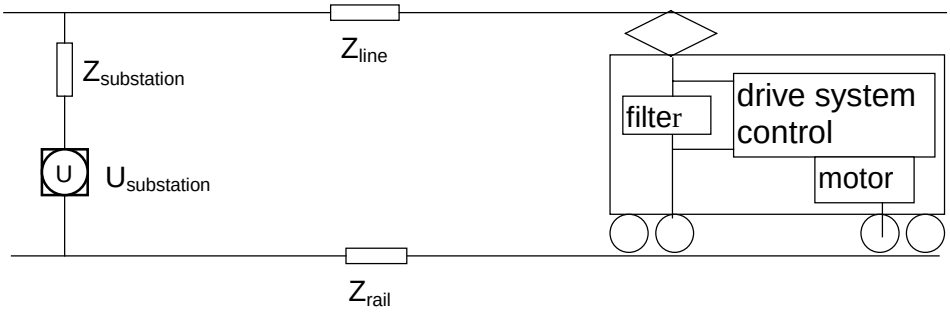

Figure 3-1. *A general traction system*

3.1 Energy supply

AC supplied lines use either 50 Hz or $16^{2/3}$ Hz in countries with 50 Hz mains, while in the USA corresponding supply frequencies are 60 Hz or 25 Hz. If the line frequency equals the frequency of the power grid, the supply system is only a transformer, if the line frequency differs from the public mains frequency, the line voltage is either produced in special power plant for traction, or in some kind of a rotating or a static converter. The general problem for AC supply is that on the public three phase side of the supply system the power flow is anticipated to be constant due to a three phase symmetrical load, while on the traction single phase side the active power is pulsating with twice the line

frequency. As the public electric companies normally do not allow this pulsating power the supply systems must be combined with filters. Power semiconductor converters will produce harmonics to the traction side, and those harmonic frequencies must be separate from the signalling system frequencies.

On DC lines the supply system consists of rectifiers. In these system the power flow is constant both on the public side and on the traction side, so the DC supply does not have the same filter problem as the AC supply. One major problem is that 50 Hz track circuits are often used in combination with DC supplied systems. Due to asymmetries in the firing angles of the rectifiers and in the three phase transformers, a large 50 Hz component can be found on the traction side. The asymmetry is especially pronounced when Hg-valve rectifiers are used.

A substation unit can normally supply a limited number of trains. In areas with a lot of traffic a number of such units are used to form a substation. Typical substation power is 10-30 MVA, and a typical locomotive power is 3-4 MW.

European main line railway electric supply system

The European countries have different railway supply systems and the supply systems at each side of a national border are often not the same. There are some exceptions: Germany, Austria and Switzerland form one group with 15 kV 16 2/3 Hz. Sweden and Norway form another group with the same system. But Denmark, located between Sweden and Germany, has a different system. France and UK have the same system as Denmark, 25 kV 50 Hz. However this supply system is mainly used on the main lines north of London. South and south-east of London the main lines are supplied with 750 VDC, which makes direct train traffic from France to London difficult.

The different supply systems are not the only reason why it is difficult for a train to cross a border. The supply system can be the same on both sides of a border, but the signalling systems with their track circuits are different. As an example: France has built a TGV train (”train de grand vitesse”) which can cross a number of borders in central and western Europe, but the train became very expensive. However there are high ambitions within the European community to harmonise the railway traffic ([6] page 275).

In table 3-1 the different supply systems on main lines are presented.

Table 3-1. Different main lines railway supply system in Europe ([6] page 276).

System	Voltage	Country
AC	25 kV 50 Hz	UK, France, Finland, Denmark, Luxembourg, Portugal, Spain
AC	15 kV $16^{2/3}$ Hz	Germany, Austria, Switzerland, Sweden, Norway
DC	3 kV	Belgium, Spain, Italy, Poland
DC	1.5 kV	France, Netherlands
DC	750 V	UK

DC railway traction power supply

This supply started to be used, mainly in the USA at the end of the last century. The voltage was 500-700 VDC, but at the beginning of this century systems with 1200 VDC started to be used ([11] page 582). The original advantage of DC supply was its simplicity to operate DC series motors, by means of series resistor control, in combination with switching from series to parallel connection during acceleration, all equipment mounted on board the vehicle. 3 kV supply systems is dating from 1920s and 1930s and are used on main lines. 1.5 kV is normally used on regional and interurban traffic with up to typically 100 km distance between feeding substations, but also some main lines use this voltage. Urban metros and trams use 600 V and 750 V, but mainlines in England are also electrified with this voltage.

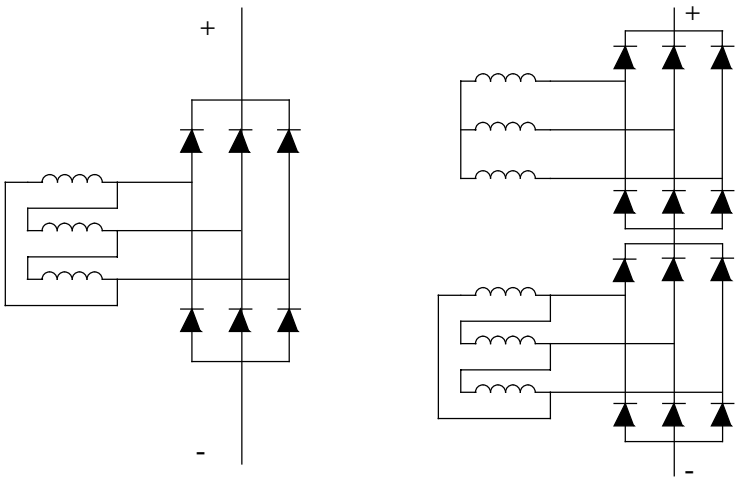

Figure 3-2. *Six pulse and twelve pulse rectifier.*

The DC voltage is fed from a converter which rectifies the three phase voltage of the mains, normally with a six pulse or a twelve pulse rectifier, into DC. Circuit diagrams for different rectifiers are depicted in figure 3-2.

By means of *(3.1)* the production of the ideal dc side harmonics can be calculated. This expression is not usable for calculation of the non ideal harmonic due to the rectifier imperfections. ([6] page 277):

$$v = \frac{pV_{\max}\sin(\frac{\pi}{p})}{\pi(m^2p^2-1)\sqrt{2}} \cdot \left[\left\{1-\cos(\gamma)\exp(jm\gamma)\right\} - jm\cdot\sin(\gamma)\exp(jm\gamma)\right] \qquad (3.1)$$

where:

γ is the overlap angle

m is the harmonic order.

p is six or twelve

From a 50 Hz six pulse rectifier the 300, 600, 900 Hz etc. harmonics are basically generated, and from a 50 Hz twelve pulse rectifier the 600, 1200, 1800 Hz etc. harmonics are basically generated.

The basic harmonics will also be found on the public three phase side of the rectifier, and can be calculated by means of *(3.2)* ([6] page 278).

$$i_A = I(\sin(\omega t) - \frac{\sin[(n-1)\omega t]}{n-1} + \frac{\sin[(n+1)\omega t]}{n+1}) \qquad (3.2)$$

Almost all multiples of 50 Hz appears in practical operation with slightly asymmetrical three phase supply and asymmetrical firing pulse patterns, and therefore track circuit frequencies are avoided at multiples of 50 Hz, e.g. no reed frequency are used at 400.

AC railway traction power supply

The disadvantage with DC supply is its rather low voltage which leads to a large line current for a certain vehicle power. The large current leads to high losses and high voltage drop on the supply line. The advantage of AC supply instead of DC is that it is easy to achieve a high voltage by means of a transformer. The high voltage makes it possible to supply main lines over long distances with a reduced number of substations. ([6] page 279). The AC supply became practical when the single phase commutator series motor was constructed, but the problem of commutating a 50 Hz current by the mechanical

commutator, lead to the use of a lower frequency. Initially the supply voltage on the Swedish mainlines was 15 Hz 15 kVAC. The voltage was produced in special power plant. Later on rotating converters, fed from the public mains produced the supply voltage, and then the frequency was changed to $16^{2/3}$ Hz ([11] page 585). Today power semiconductor converters are more and more coming into operation.

With the introduction of on board rectifiers, especially solid state rectifiers, it was possible to supply traction motors with DC voltage. Later AC electrification has therefore been 50 Hz 25 kV, with start in France after the Second World War. The 50 Hz can easily be supplied to the line via transformers directly from the public grid.

3.2 Energy distribution

DC line

DC supply lines are only defined by the line resistance when concerning the electrical power distribution. However when also the harmonics distribution is taken into account, the reactance of the line must be included. Normally the line impedance, (= inductance) reduces the line interference, and therefore the line interference is studied at worst case situations, i.e., when the vehicle is located directly at a substation where the supply line length diminishes.

When used for metros, and, if the voltage are below 1 kV, the power is normally distributed via a third rail just along the track, see figure 1-1a. However, for obvious reason, the distribution to trams and street cars is an overhead catenary, see figure 1-1b.

In DC supply the current return is formed by the rails, but the current return can split so a fraction will flow through the earth which can cause some problems, metallic construction in the earth is already mentioned, see DC track circuits in chapter 2.4. The earth current will not be shunted by short circuiting wheel axles, and this earth current can enter the rails again where it can interfere with the track circuit receiver. Also earth current from adjacent tracks can enter the rails and interfere with the track circuit receiver. Harmonics in the earth current can crosstalk and interfere with other signal cables routed in the ballast. For these reasons, as mentioned before, it is highly recommended that the rails are insulated from earth, ([14] page 103). Another solution to this problem is the use of an isolated fourth rail as the current return. This system is used in the London Underground, and an extra advantage with this four rail system is the separation of the signalling current in the running rails from the traction current return.

AC line.

AC supply lines normally uses high voltage in order to reduce the power loss, as the current becomes low. Therefore, the resistance of the supply line has a minor interest, it is rather the line inductance that determines the power distribution. The line inductance, together with the substation and vehicle transformer impedance and the line stray capacitance forms a resonance circuits that makes it difficult to predict the frequency behaviour of the line. As the long lines have a large inductance the power factor can be 0.8 as an average. In phase controlled drive systems the power factor is reduced and can be as low as 0.4 at start. The power factor can be a real problem on long single fed lines where the reactive power reduces the feeding voltage at the vehicle. The introduction of phase controlled drive system has also increased the generation of AC lines harmonics.

The simplest and least capital intensive way of connecting the supply to the line is to connect one end of the transformer secondary winding to the catenary and the other to the rail, see figure 3-3 ([6] page 281).

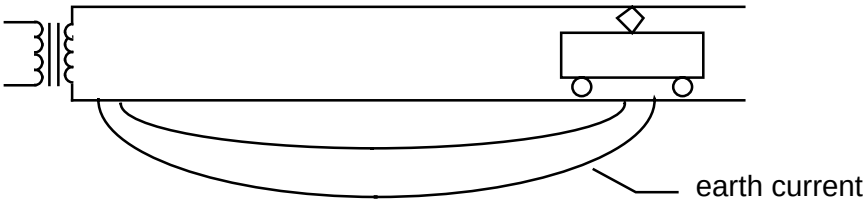

Figure 3-3. *Simple feeding.*

The disadvantage of this connection is that a major fraction of the return current will be through the earth. The earth current will crosstalk to other signal cables in the track bed, and it can also interfere with the track circuits as described in the DC line part above. Besides, the overhead catenary will, together with the current return in the rails, form a big loop that will act as a transmitter of radio frequency interference.

The problems of crosstalk with telephone lines became obvious from the start of AC railway electrification, and different attempts have been used to control the current return path.

The situation can be improved by connecting a return conductor in parallel with the running rails ([6] page 281).

With the installation of booster transformers with unity ratio, see figure 3-4, less current return will spread to earth and a larger fraction of the current will

remain in the rail ([15] page 107). This arrangement reduces both cross talk and emissions. It can also solve the problem of carrying the traction current over an insulated rail joint, see figure 2-1 and figure 2-13.

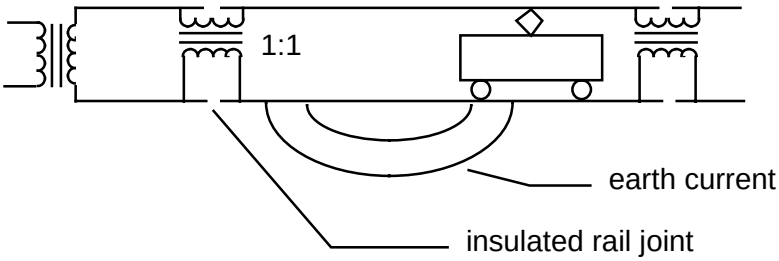

Figure 3-4. *AC supply with a booster transformer for reduction of the earth current.*

However as the current still is in the rail, it can disturb the telephone lines. Also the loop antenna is still rather big. Both these effects will further be reduced when booster transformers are used to pick-up the return current from the rails to a conductor installed close to the top of the masts, see figure 3-5. As the distance between the overhead power line and the current return now is small the line impedance is reduced ([13] page 92, [15] page 107).

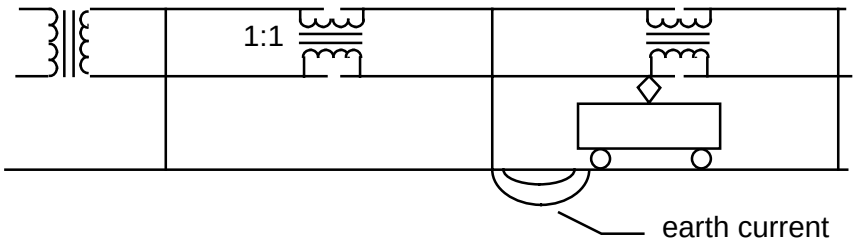

Figure 3-5. *AC supply with a booster transformer in combination with a mast top current return cable for further reduction of the earth current.*

The same advantage as with the booster transformer in combination with the mast top current return conductor can be achieved with an auto transformer, see figure 3-6. With this arrangement the line inductance is further decreased and the voltage drop along the line is reduced, which allows higher power to be distributed at a long distance from the substations. Also the spacing between substations can be increased. ”Malmbanan” in the northern part of Sweden uses auto transformer distribution.

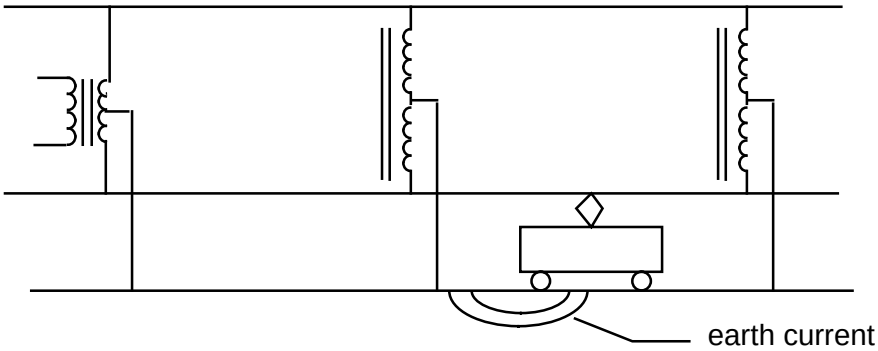

Figure 3-6. *Auto transformer feeding for further reduction of the line inductance.*

In AC system, the distance between substation is normally much longer than in DC systems. This will together with line inductance result in high rail potentials, and therefore the rails must be earthed ([12] page 89, [13] page 92). With the use of booster or auto transformers the earth current problems, as described in the DC system, are reduced as the earth current is reduced. However earth current from adjacent tracks or other installation can still interfere with the track circuits. So, care must be taken if the rails must be earthed at more than one position per track circuit.

3.3 The three phase AC motor drive systems.

The first attempt with three phase induction motors goes back to 1920s. At the turn of the 20th century some tracks in Germany, Italy, Switzerland and USA were built for trains with three phase induction motor drives. The power was either supplied with three overhead catenaries, or with two overhead catenaries and the running rails as the third phase. The speed and torque control were achieved with pole changing and with resistors in series with the rotor.

The main problem was the supply of three-phase motors from DC or from a single-phase AC. Kando in Hungary built a drive system with slip ring induction motor fed from a rotary phase converter, ([5] page 143). During the 1970s the development of high-power thyristors led to three phase drives mainly based on current source converters, which soon was replaced by voltage source converters in combination with high-power gate turn off (GTO) thyristors. In 1976 the first voltage source inverter drives system was tested in a locomotive (DB 120). The voltage source converter is now established as the standard traction approach. The latest development step is to use bipolar or

insulated gate bipolar transistors (IGBT) as the standard component in low and medium power drive systems. The three phase induction motor has the following advantages ([5] page 143):

- High maximum speed
- Robustness and reliability with low maintenance requirement
- Simple cooling arrangement with enclosed frames
- High uniform torque with inherent overload management
- High power/weight ratio
- Low cost/power ratio
- High voltage operation
- Inherent regenerative braking capability
- Steep torque-speed characteristics
- Parallel connection feasible

From a traction point of view these advantages make a drive system based on three phase AC motors very good. From a signalling point of view there is a big disadvantage, the motor must be fed from a variable voltage, variable frequency machine converter. As the frequency is allowed to vary over a wide range the converter will produce variable frequency line interference in the DC supply and in the AC supply with finite DC-link capacitor, i.e. also including critical frequencies.

A modern machine converter consists of three phase branches. Often brake chopper branches are connected in parallel with the DC-link, see figure 3-7.

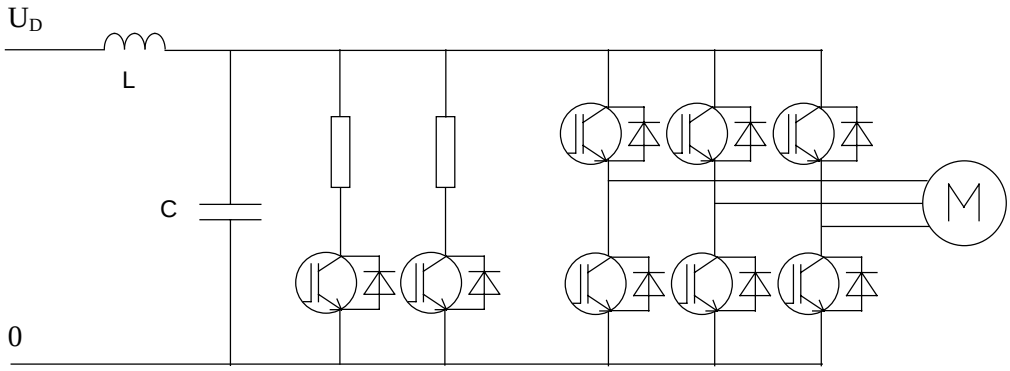

Figure 3-7. *A three-phase machine converter with a two-phase brake chopper, used in DC supplied drive systems. The converter switching elements are IGBTs.*

Two transistor/diode pairs forms a phase leg, where the semiconductor switches either connect the DC-link high voltage or the DC-link low voltage to the motor phase winding. The converter consists of three such phase legs. When power-transistors are used, the diode is normally integrated in the same module. When the upper position in a phase is conducting, a positive current will go through the upper transistor. When the modulation pattern to the phase is changed to lower position, a positive current commutes to the lower diode. In a corresponding way, a negative current will flow through the upper diode and commutes over to the lower transistor. The switching sequence is critical, a fast switching gives low switching losses but stresses the semiconductor. At turn-off, the voltage will be high due to *Ldi/dt*. When transistors are used the switching speed can and thus the voltage can be controlled.

When GTO-thyristors are used instead of transistors the turn-off is faster and a snubber capacitor is required in parallel with the thyristor. To reduce the diode current inrush also a snubber inductor is needed..

A well designed induction motor traction drive system will have the base frequency where the machine converter gives its maximum output voltage with nominal DC-link voltage, at about one third of maximum speed. The drive system is designed to have full flux below base frequency, i.e. the motor voltage/stator frequency ratio is kept constant. Above base frequency the field weakening region starts. In the field weakening area, square wave modulation is normally used and the output voltage is kept constant. The maximum output power is also kept constant. The limiting speed for maximum constant power will be above typically two third of maximum speed, where the pull out (break down) torque will limit the power. In 750 VDC and 1500 VDC fed voltage-source-converter traction drives, the DC-link capacitance is connected to the DC line supply via an inductor. The DC-link voltage will therefore vary as the

supply line voltage varies, and when the DC-link voltage is low the field weakening area will start at lower speeds than the base speed.

DC supplied vehicle uses a LC filter, of at least second order, as an input filter to reduce the harmonic generation to the line, but the filter is also used to reduce the harmonics generated by the substation.

The control system

In normal mode accelerations and retardation, the feedback control system has small influence on the production of harmonics. Therefore relative simple open-loop slip frequency control with current feedback was implemented in early induction motor drive systems, fed from machine converters. The torque was controlled at constant rotor flux by the ratio of slip frequency and rotor resistance. Acceptable steady-state behaviour is obtained with speed and stator current feedback, by calculating the slip frequency and by adding this frequency to motor speed the converter frequency is found. Correction of the motor voltage by the current control loop is sufficient to maintain the flux at the reference value, ([5] page 149).

However this kind of control system is not fast enough in more dynamic control action like slip/slide control, or the control of transient caused by voltage interruptions at pantograph bouncing. A fast and accurate vector control system can prevent the production of torque pulsation and corresponding line interference. A fast control system can be used in active elimination of critical frequencies.

Vector control with pulse-width modulation is now used in most modern induction motor drive systems fed from a machine converters, see figure 3-8. This drive system is today used in all kind of rail vehicles from trams and street cars with limited rating up to big freight locomotives.

A vector control system is usually oriented to either the stator-flux or the rotor-flux linkage vector. The following description is based on a stator flux vector orientation. Since the stator flux cannot economically be measured directly, it has to be calculated based on the measured quantities stator voltage, stator current and rotor speed. There are several ways to perform these calculations, generally referred to as flux observers. In this case, a flux observer reported in ([21], page 38) is used. Both the stator flux estimate, and the stator current are expressed in a reference frame *(d,q)* oriented to the stator flux linkage vector estimate.

The three phase voltages and the three phase currents are measured and expressed as the complex voltage $(u_{s_\alpha}, u_{s_\beta})$ and the complex current (i_{s_α}, i_{s_β}.). The

resistive voltage drop in the stator is calculated and subtracted from the voltages $u_{s\alpha}$ and $u_{s\beta}$, and thereafter the magnitude and the argument of the flux is formed in the flux observer by integration. A new reference frame *(d,q)* is attached to the stator flux linkage vector, and thus the flux magnitude is identical to the direct component ψ_d.

The stator flux estimate is compared to the stator flux reference, and the error is fed to a flux controller. The output of the flux controller is the voltage-time area reference for the output voltage along the *d*-axis of the machine converter during the coming sampling interval.

The torque reference is divided by the modulus of the stator flux linkage vector, resulting in a reference for the torque producing stator current component. By means of the angle θ_s the current components $i_{s\alpha}$ and $i_{s\beta}$ can be transformed to the quadrature current component. This current reference is then compared to the measured equivalent and the error is fed to a PI current controller, calculating the reference for the output voltage along the *q*-axis of the machine converter during the coming sampling interval.

The direct and the quadrature component of the voltage-time area are by means of the angle θ_s transformed to the α,β-frame, which after 2/3 transformation forms the desired three phase voltage-time area references.

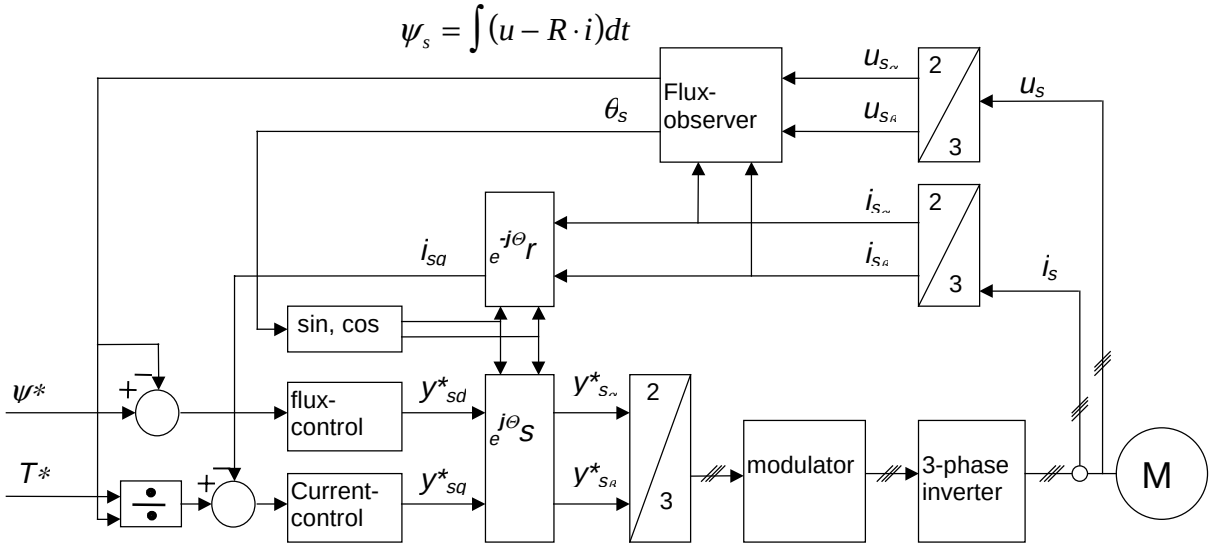

Figure 3-8. *Induction motor torque control based on stator flux*

The following seven equations form the control algorithm ([19] page 3-75):

Torque control:

$$i_{sq}^{*}(k)=\frac{T^{*}(k)}{\psi_{sd}(k)} \tag{3.3}$$

where $T^{*}(k)$ is the torque reference and $\psi_{sd}(k)$ is the stator d-axis flux approximately, with the same amplitude as the air-gap flux amplitude.

Flux control:

$$\begin{aligned}
&y_{sd}^{*}(k)=R_s\cdot i_{sd}(k)\cdot T_s+\left[\psi_{sd}(k+1)-\psi_{sd}(k)\right]=\\
&=\left\{\psi_s^{*}(k)=\psi_{sd}(k+1), i_{sd0}\approx\frac{\psi_s}{L_s}\right\}=\\
&=\frac{R_s}{L_s}\cdot T_s\cdot\psi_s+\left(\psi_s^{*}(k)-\psi_s(k)\right)=\\
&=\left\{\psi_s=\sum_{0}^{k-1}\psi_s^{*}(k)-\psi_s(k)\right\}=\\
&=\frac{R_s}{L_s}\cdot T_s\cdot\sum_{n=0}^{k-1}\left[\psi_s^{*}(n)-\psi_s(n)\right]+\left[\psi_s^{*}(k)-\psi_s(k)\right]
\end{aligned} \tag{3.4}$$

where y_{sd}^{*} is the direct component of the voltage-time area reference.

Current control:

$$\begin{aligned}
&y_{sq}^{*}(k)=\left(R_s+\frac{L_s}{\tau_r}\right)\cdot\sum_{0}^{k-1}\left[i_{sq}^{*}(n)-i_{sq}(n)\right]\cdot T_s+\\
&\left[\sigma\cdot L_s+\frac{\left(R_s+\frac{L_s}{\tau_r}\right)\cdot T_s}{2}\right]\cdot\left[i_{sq}^{*}(k)-i_{sq}(k)\right]+\omega_r(k)\cdot\psi_{sd}(k)\cdot T_s
\end{aligned} \tag{3.5}$$

where y_{sq}^{*} is the quadruple component of the voltage-time area reference.

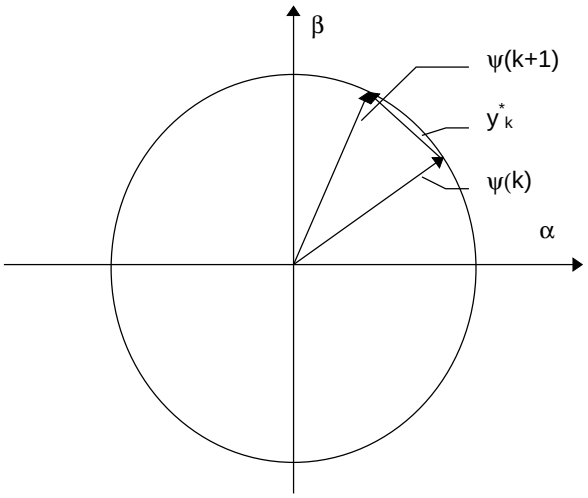

Figure 3-9. *The integral of the terminal voltage, i.e. the terminal flux, ψ(k), will grow to ψ(k+1) with the vector y(k) during the time between the sampling instants k and k+1 .*

In this control system seven transducers are needed: three current transducers, three voltage transducers and one stator winding temperature-transducer. The number of transducers can be reduced. As the neutral point of the stator windings is not connected to zero the third phase current can be calculated from the other two:

$$i_c = -(i_a + i_b)$$

The three voltage transducers can be reduced to a single one, the DC-link voltage transducer, which anyway is needed for the modulation. By combining the DC-link voltage with the actual modulator output for the three phases, the three phase voltages can be found. However these phase voltages are the ideal voltages, in reality the commutations are delayed, and therefore the real flux will differ from the estimated, but this will be taken care of by the flux observer.

The modulator

The three output phase voltage references from the control system are sinusoidal in stationary operation. However a machine converter can only form discrete levels, in the actual case described by two levels. By means of pulse width modulation, PWM, the output voltage-time area has sinusoidal shape.

In a machine converter eight (=2^3) different voltage vectors are available, see figure 3-10. Only one of the transistors in a phase leg can be conducting, either the upper (=”1”) or the lower (=”0”). The voltage vectors are shown in figure 3-10.

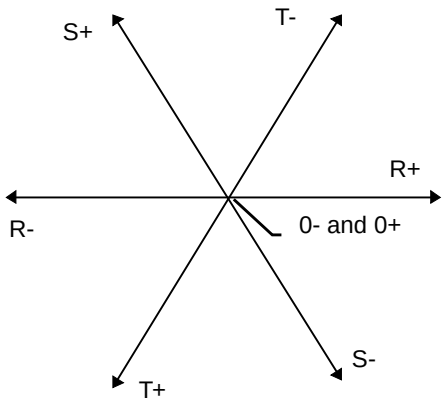

Figure 3-10. *The magnitude and direction of the six voltage vectors and the two zero voltage vectors in a machine converter.*

These voltage vectors are used in different combinations. The intention for the choice of combinations is to produce a constant torque. To do this, a three phase close to sinusoidal output phase voltage with a low amount of harmonics, especially low frequency harmonics, must be produced. This is achieved by means of a high switching frequency, the higher the switching frequency the lower the amount of harmonics. However, the cost is high switching losses.

As long as the desired reference voltage amplitude is lower than half the DC-link voltage, sinusoidal PWM modulation can be used. This is not quite true, the sinusoidal amplitude region can be increased with about 15%, by subtraction of a third harmonic common mode voltage to the desired output voltage. This third harmonic will be cancelled in a machine converter. The maximum fundamental phase voltage amplitude is 0.64 (=2/π) of the DC-link voltage when generated with square wave modulation, which produces a output voltage with constant amplitude. This modulation is normally used in the field weakening area. Between sinusoidal and square wave modulation, polar modulation is used to overlap the output voltage gap. Polar modulation generates an output voltage with variable amplitude but the generated harmonics has lower frequency.

In sinusoidal PWM modulation the combination of voltage vectors is generated by carrier wave modulation. The desired voltages of the three phases are indicated as three sinusoidal shaped curves, and the carrier is the triangular wave intersecting the sinusoidal waves. When a phase voltage reference is higher than the triangular wave the modulation pattern is ”one” and when the phase voltage is lower the modulation pattern is ”zero”. Around the points where the triangular wave is changing direction a zero voltage vector is generated, the ”(0,0,0)”-voltage vector is generated at the high peak and the ”(1,1,1)” vector at the low peak. In figure 3-11 the generation of a modulation pattern is demonstrated. The ratio between the carrier frequency and the desired stator frequency equals 9.

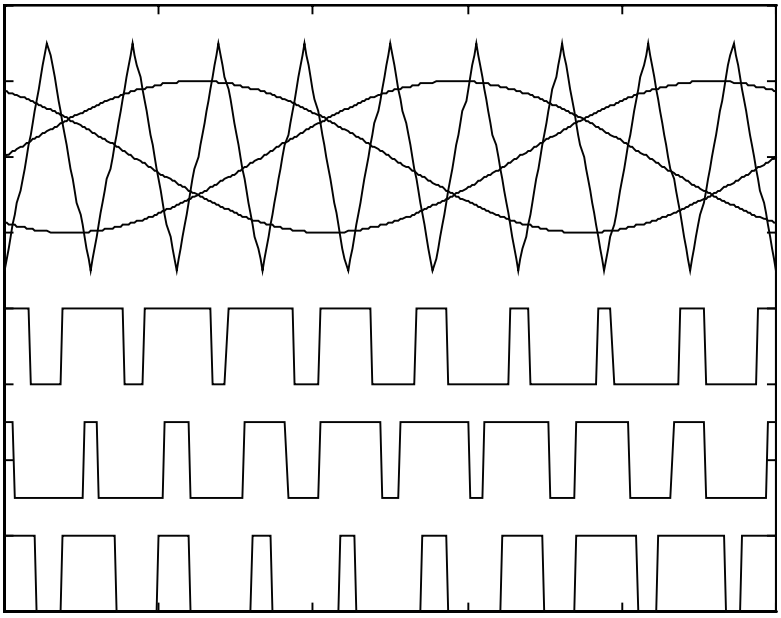

Figure 3-11. *Generation of SIN modulation pattern by means of carrier wave*.

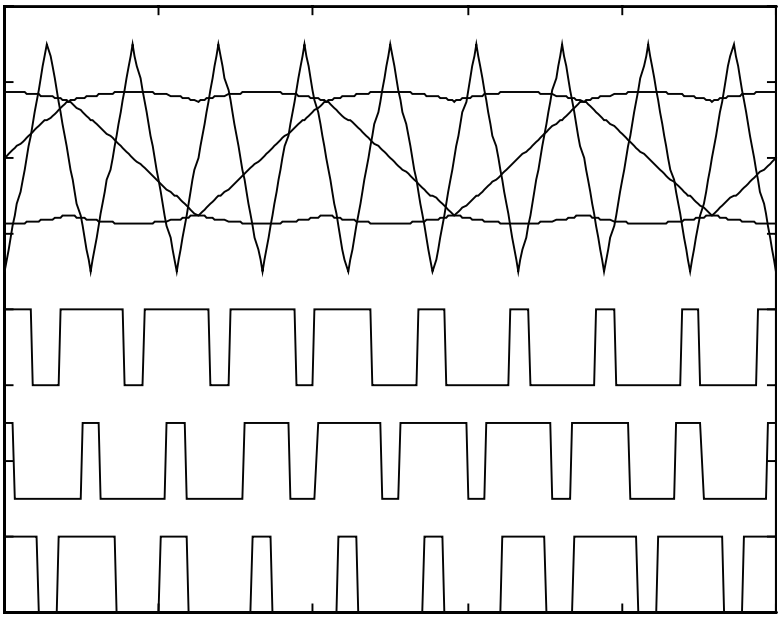

Figure 3-12. *Generation of SIN modulation pattern by means of carrier wave. A third harmonic is added to the fundamental frequency by symmetrisation.*

In figure 3-12 the same generation is demonstrated, but here the third harmonic is added by symmetration. The corresponding flux trajectory is found in figure 3-13.

The trajectory is almost circular, created by the six voltage vectors directions available. The zero voltage vectors are placed equidistant on the circumference of the desired flux circle. In the figure the trajectory is divided in six sectors, each one using a certain combination of voltage vectors, see figure 3-10:

sector 1: R+ and T-
sector 2: T- and S+
sector 3: S+ and R-
sector 4: R- and T+
sector 5: T+ and S-
sector 6: S- and R+.

The change from one sector in figure 3-13 to the next happens when two of the sinusoidal curves crosses, see figure 3-11.

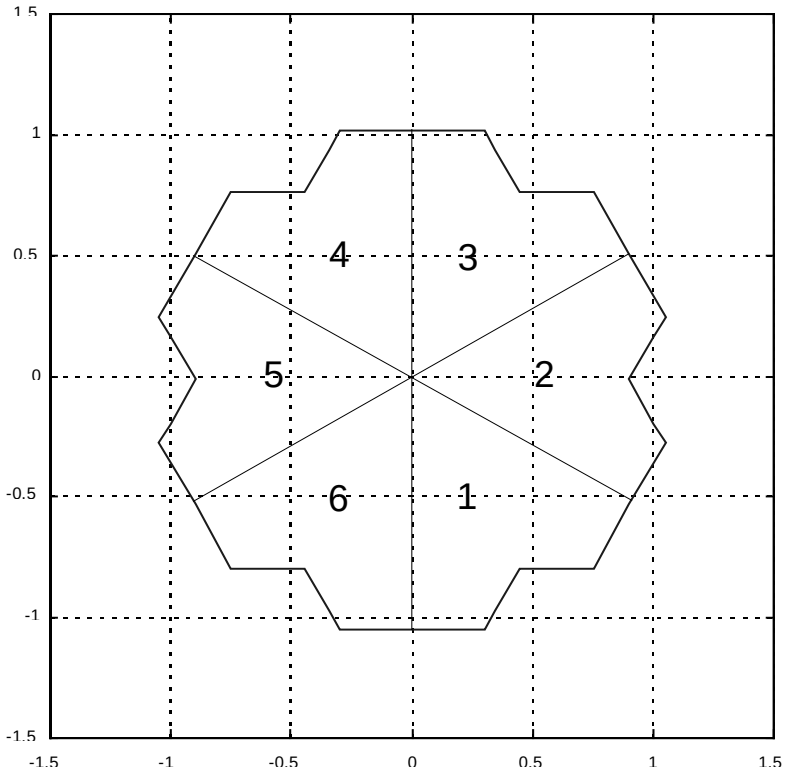

Figure 3-13. *The flux trajectory at SIN modulation with the ratio between the switching frequency and the fundamental frequency equals 9*

The carrier frequency can either be synchronous or asynchronous with the fundamental frequency. When the ratio between the carrier frequency and the fundamental frequency is high asynchronous modulation can be used, but as the fundamental frequency is increased the ratio becomes lower and lower and the need for synchronous modulation increases. In figure 3-14 a modulation strategy is shown where asynchronous sinusoidal modulation with 550 Hz switching frequency is used up to 26 Hz. Thereafter synchronous sinusoidal modulation is used with different ratio steps 21, 15 and 9. Maximum voltage for sinusoidal modulation is at 85 Hz, before maximum switching frequency is reached. From 85 to 95 Hz polar modulation with a ratio of 3 is used, after which square wave operations takes over for the constant power region.

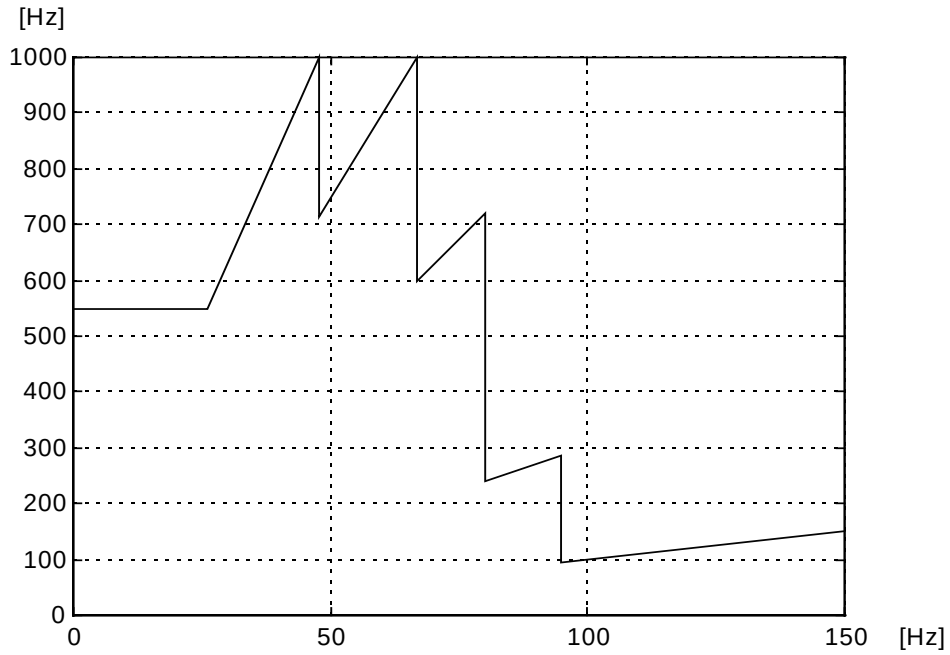

Figure 3-14. *A three phase motor drive system modulation strategy with switching frequency versus stator frequency.*

3.4 The AC fed single phase line converter

AC fed voltage source traction drives.

An AC fed voltage source induction motor drive system consists of a machine converter, a line converter and between them the intermediate voltage source DC-link, see figure 3-15.

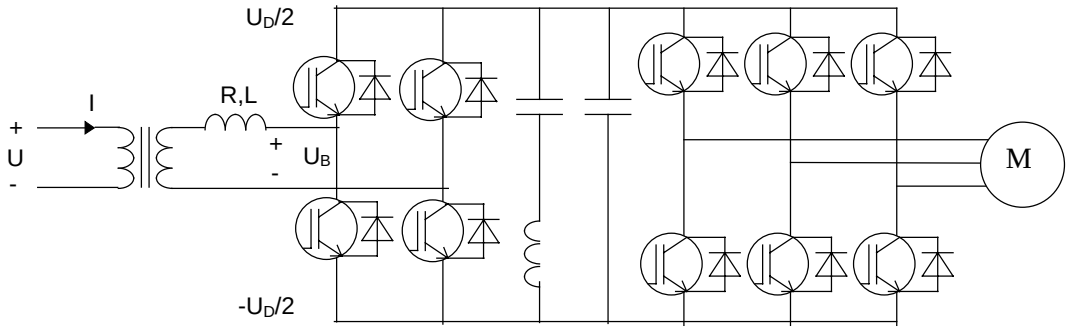

Figure 3-15. *A three phase machine converter fed from an one bridge line converter, used in AC supplied drive systems. The switching element are here IGBTs.*

The line converter, an AC-DC converter, is required to supply the DC-link. It is either a diode or thyristor-controlled rectifier or a four quadrant converter, which is controlled with PWM, normally with unity power factor operation with full power regeneration capability. The phasor diagrams for motoring and regeneration are shown in figure 3-16. Note that all quantities are referred to the transformer primary side. At high line voltages it can be impossible to keep unity power factor at regeneration, then the phase angle must be changed. The principle was first developed in Germany and Japan and is now being widely applied in Europe for most AC fed vehicles ([5] page 151). The machine converter is already described.

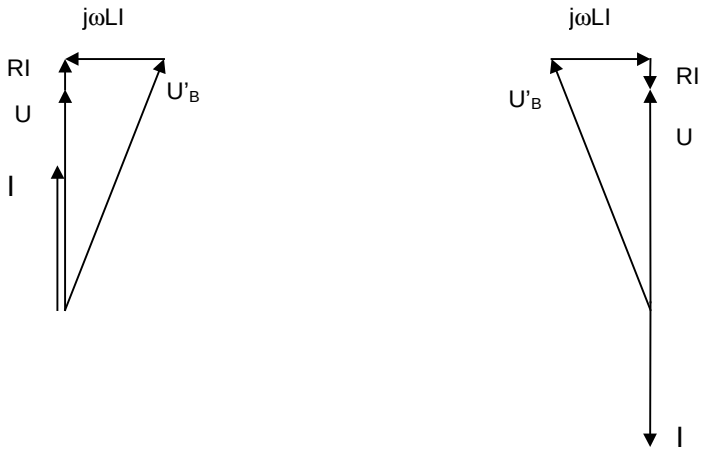

Figure 3-16. *The phasor diagram of the line converter in motoring and in regenerating mode*

In the line converter one transformer secondary winding is connected between two line converter phase legs. The line converter voltage applied to the transformer is the difference between the two phase potentials. A simplified picture of the line converter is found in figure 3-17. If the line converter bridge voltage u_B is lower than the secondary winding voltage u, the current will flow through the inductor, in reality formed by the transformer leakage inductance, into the drive system. If u_B is higher than u the current will flow out from the drive system. In this way the line converter can control the power direction by varying the voltage. However, if the line converter shall produce a voltage higher than the secondary winding voltage u, the DC-link voltage must be higher than $\hat{u}$. The line converter must be a step up chopper, and the transformer connected to it must have a high leakage inductance, typically 30% ([20] page 97).

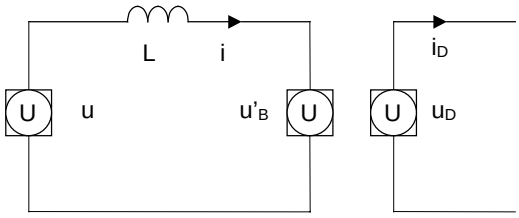

Figure 3-17. *A simplified model of the line converter*

Often two (or more) secondary windings are connected in parallel to the same DC-link. The modulation pattern of these are normally inter-laced in order to increase the line interference frequency and to decrease its amplitude.

As the supply is a single phase voltage, the AC-DC converter will produce a current to the DC-link with twice the line frequency. Therefore a second harmonic link is connected in parallel to the DC-link, tuned to have zero impedance at the double frequency in order to minimise the DC-link voltage ripple. A voltage ripple will otherwise be modulated again by the line converter and high order harmonic frequency due to frequency multiplication will be produced to the line, see figure 3-18.

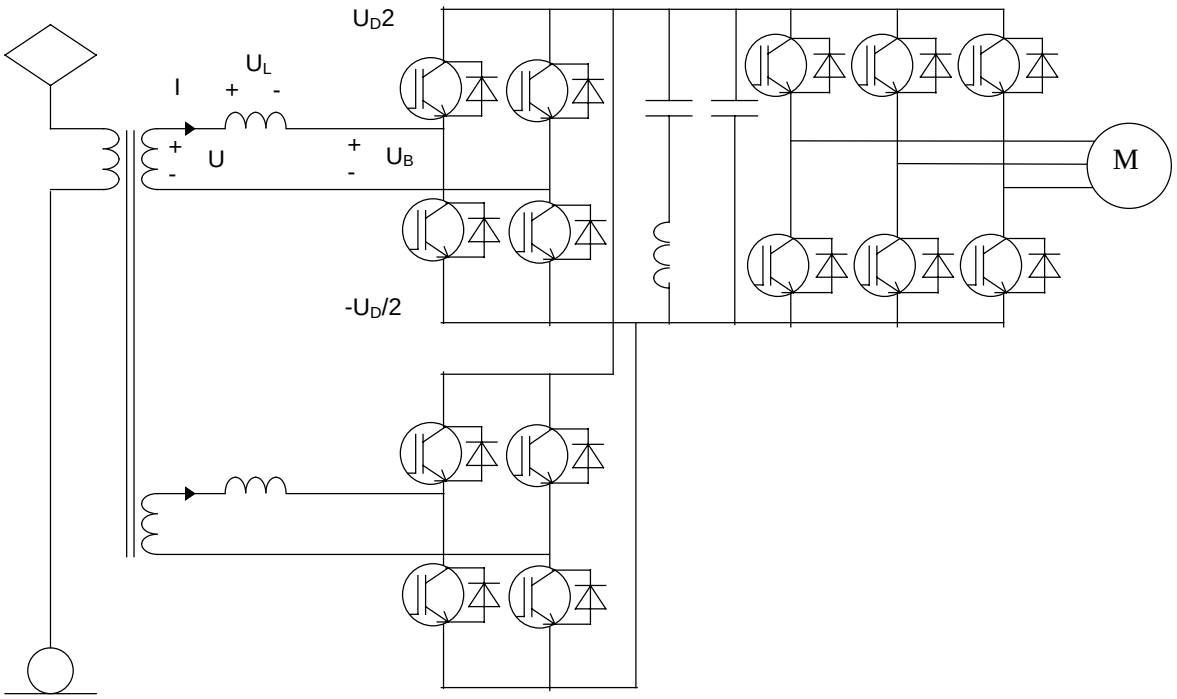

Figure 3-18. *An AC supplied AC motor drive system with two bridges and four phase legs.*

The line converter uses a constant switching frequency, which should be different from the actual track circuit frequency. The harmonics generation will not only have constant frequency. The variable machine converter frequency will be modulated by the line converter and will be found in the line current as side band around the line converter switching frequency.

The control system

The measured DC-link voltage is compared with the DC-link voltage reference, see figure 3-19. The difference ε is fed to a PI controller. The output ξ from the controller is the current needed for maintaining the DC-link voltage. To this value, the feed forward current, calculated from the machine and auxiliary converter power is added. The current reference is formed by multiplying this value with $sin(\omega t+\phi)$, where ω is synchronised with the measured line voltage. The current reference is used in the control algorithm for the desired line converter voltage ([20] page 101, 102), see figure 3-19:

$$u_B^*(t) = u - L_s \frac{di^*}{dt} \approx u - \frac{L_s}{T_s} \cdot \left(i\left(t_{k+1}\right) - i\left(t_k\right) \right) \qquad (3.9)$$

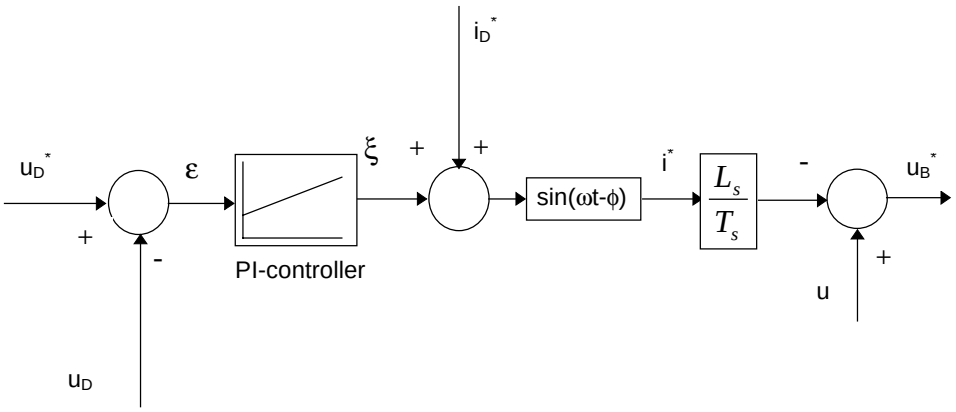

Figure 3-19. *The line converter control system.*

The Modulator.

The output $u_B^*(t)$ from the control system is the desired line converter bridge voltage and is fed to the modulator. The bridge voltage is the difference between the voltages of the two phases connected to a bridge. The two phase voltages have the same magnitude, each equals half the desired bridge voltage, and with a 180 degrees phase shift, see figure 3-20.

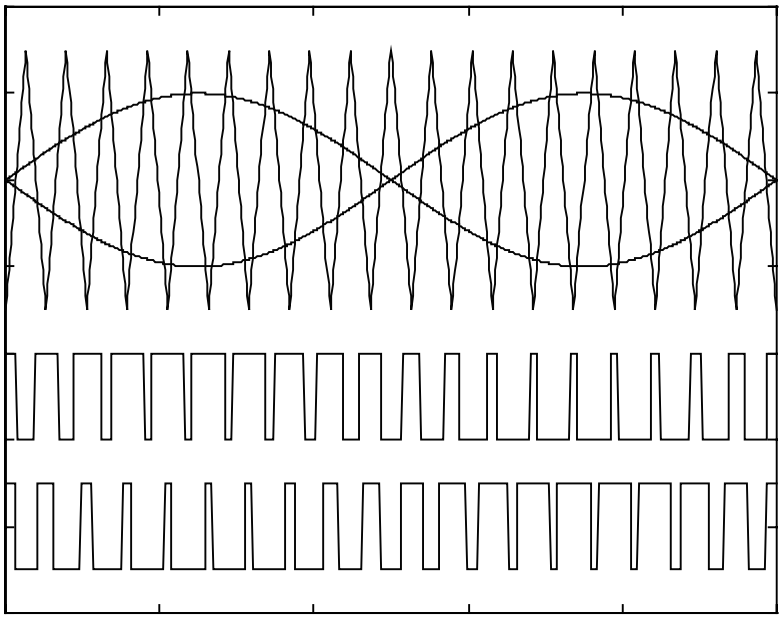

Figure 3-20. *Generation of the modulation pattern for one bridge by means of one carrier wave.*

The line converter modulation is similar to the machine converter sinusoidal modulation, and the modulation pattern is found at the points where the carrier frequency triangular wave intersects the desired sinusoidal curves

In figure 3-21, the modulation pattern of two interlaced bridges are presented.

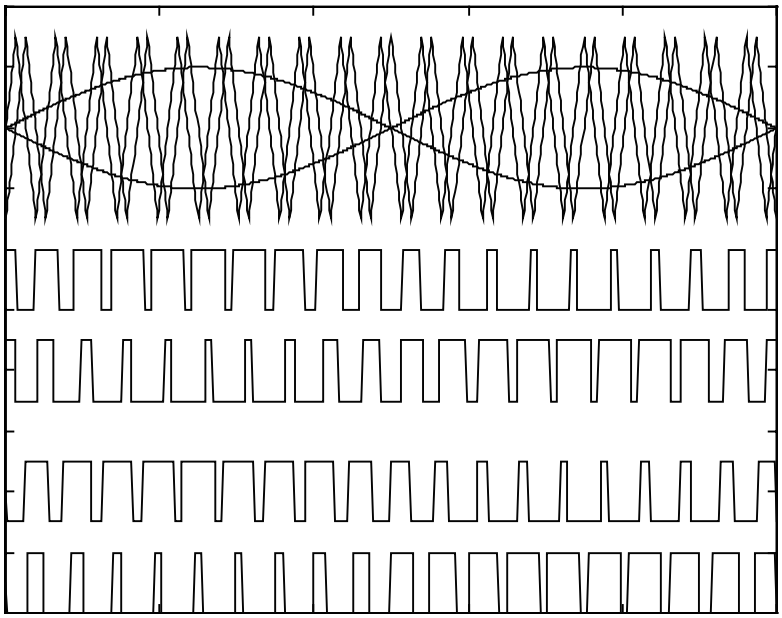

Figure 3-21. *Generation of the modulation pattern for two bridges (= four phases) by means of two carrier waves.*

4 EMC Model of the Traction System

The output from a machine converter is the required fundamental three-phase voltage to run an induction motor with a certain torque at a certain speed. The inverter can be regarded as an amplifier which amplifies the controller output to a real motor voltage. Ideally, the output shall be sinusoidal, but then the difference between the constant DC-link voltage and the output sinusoidal voltage would cause power losses in the semiconductors, high enough to destroy them. Therefore the inverter sinusoidal output is achieved by pulse modulation. In a two level inverter, the output is either the DC-link high voltage or the DC-link low voltage, in a three level inverter also the DC-link mid voltage is available as a switching level. By varying the pulse duration, the inverter output can produce the desired motor voltage-time area, the inverter uses pulse width modulation (PWM). The advantage of modulation is the production of the desired fundamental voltage output with low power loss. The disadvantage is the production of not desired harmonics covering the frequency interval from some Hz up to several tens or even hundreds of MHz.

There are two ways to reduce the line interference, by using a certain modulation strategy or by using a line filter. Normally, a train has several traction modules, each one with a line filter. All this filters will together shunt the interference current further and prevent it from reaching the line and the track relay.

At the design stage of a drive system it must be possible to predict the generation of harmonics, both the level and the frequency. The inverter semiconductors are often regarded to be ideal switches, but experience tells us the opposite. It must also be possible to predict the production of harmonics from a non ideal motor drive inverter. At the design, the track circuit trip level and the rails imbalance, concerning how the traction current return is shared between the rails, must be known, see figure 4-1.

In this chapter the generation of harmonics from a three phase voltage source machine converter will be studied, including the effect of non ideal switches. The production from a two phase and a four phase line converter will also be studied.

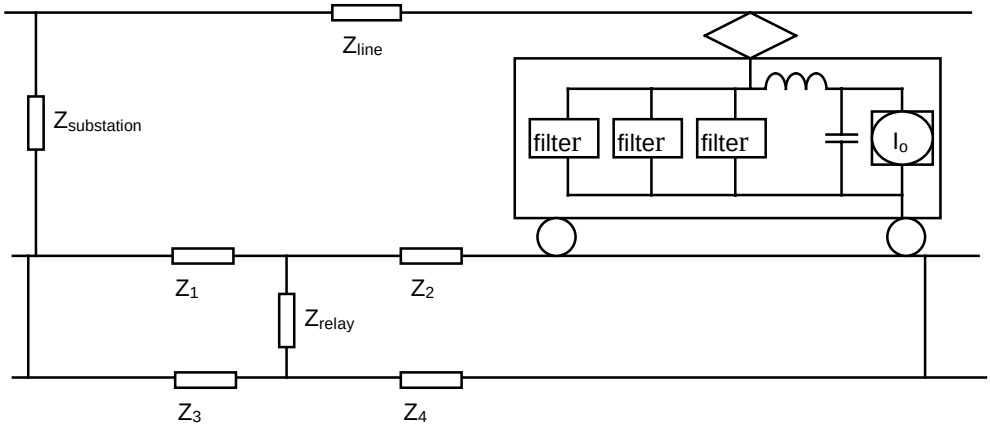

Figure 4-1. *The interference model, including the substation impedance, the line impedance, the impedance of the rails, the track relay impedance and the vehicle impedance. The source of interference is modelled as current source.*

4.1 ASCALP description

At Adtranz, Sweden, the calculation program Ascalp (asynchronous motor drive system calculation program) has been developed by the author for predictions in the design process of a propulsion system.

Most of the calculations are done in the frequency domain at steady state conditions. Ascalp is not a tool to analyse transient effects. Despite the fact that the calculations are done in the frequency domain, some results must be converted to the time domain to be able to calculate such data as maximum turn-off current, current peak values and semiconductor switch losses. In this context Ascalp's capability of line interference calculations will be studied.

To calculate the line interference at all possible operating conditions while running the train a certain distance, the calculation must be done with various combinations of time, tractive/braking effort, vehicle speed and catenary voltage. In Ascalp such a combination defines a operating point. A ride from, for instance Stockholm to Gothenburg, will contain thousands of such calculations points. Together with the operating point data also a large number of component parameters must be specified. At each operating point, the line interference and the DC-link current spectra will be stored. The DC-link current can afterwards be used in the design of special line filters.

About the mathematical background for Ascalp, see appendix B.

Ascalp calculation of a DC supplied drive system

A *traction module*, see figure 4-2, has one DC-link and one line inductor, i.e. the default line filter. A traction module also has an arbitrary number of identical machine inverters, connected in parallel. The DC-link is the sum of the DC-links in each machine inverter connected to the DC-link.

Each *machine inverter* has an arbitrary number of identical *three phase induction motors*, connected in parallel. Each motor is mechanically connected to one *mechanical gear* and one wheel-set. A traction module has an arbitrary number of identical *brake chopper phases*. A *DC supplied drive* consists of an arbitrary number of identical traction modules.

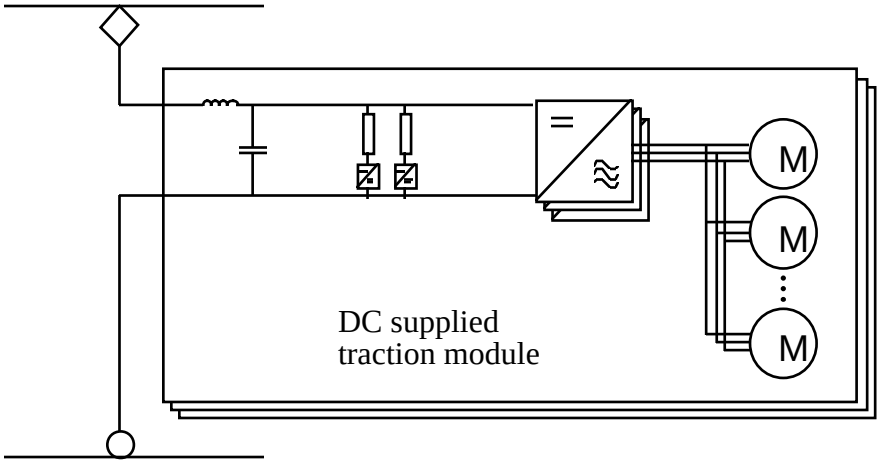

Figure 4-2. *A DC supplied drive system*

The first step of the calculation is to find the desired motor operating point. With the tractive/braking effort together with the wheel radius and the mechanical gear ratio as actual input data, the desired motor speed and the motor torque is calculated. Based on the DC-link voltage and the motor parameters the necessary motor voltage and stator frequency is found. Once again using the DC-link voltage together with maximum allowed switching frequency for the semiconductors and using such limiting parameters as minimum allowed time between two commutations the time domain modulation pattern is found. The calculations are based on the defined rules for the modulation pattern. The next step is to move the modulation pattern to the frequency domain by fourier series expansion (not FFT), and then by multiplication of the modulation pattern and the DC-link voltage, the complex phase voltage is formed. In the calculation of the complex phase current the traditional impedance model of the motor is used. The three phases form an

equation system, that is easily solved. This calculation process will be repeated for every harmonic.

When the phase current in the frequency domain is formed with all harmonics, it can be converted to the time domain by means of inverse fourier series expansion. The time domain signal is of most interest for calculation of switch losses etc., but it has also interest in the line interference calculations, the current value at every commutation will be used for finding the commutation delay, which to some extent is current dependant. The time domain phase current will also be used to find the voltage drop across the semiconductors. With the knowledge of the commutation delay and the semiconductor voltage drop, a new time domain modulation pattern can be formed. The whole calculation will then be repeated, and now the result will also contain the effects of non ideal commutations and on-state voltage drop.

The DC-link current is found by multiplication of the time domain phase current and the time domain modulation pattern in each phase, and then add the contributions from all three phases. There are two methods for this multiplication; either multiply the pure time functions of the phase current and the modulation pattern, or express these functions as Fourier series and then multiply the Fourier series components, using the trigonometric multiplication rules. In the first case the result will be the DC-link current in time domain, in the second case, which Ascalp uses, the result is the frequency domain DC-link current. The frequency domain DC-link voltage ripple is found by multiplying the frequency domain DC-link current with the impedance formed by the DC-link capacitor impedance in parallel with the impedance formed of the line inductor in series with the line and the substation.

When calculating the phase current at the start a pure DC DC-link voltage is used. Now the whole calculation can be repeated and then also the contribution from a DC-link ripple will be taken into account. The DC-link ripple can originate from the machine converter or from any other source connected to the DC-link, and thus Ascalp can be used also for calculation of cross modulation products, see figure 4-3.

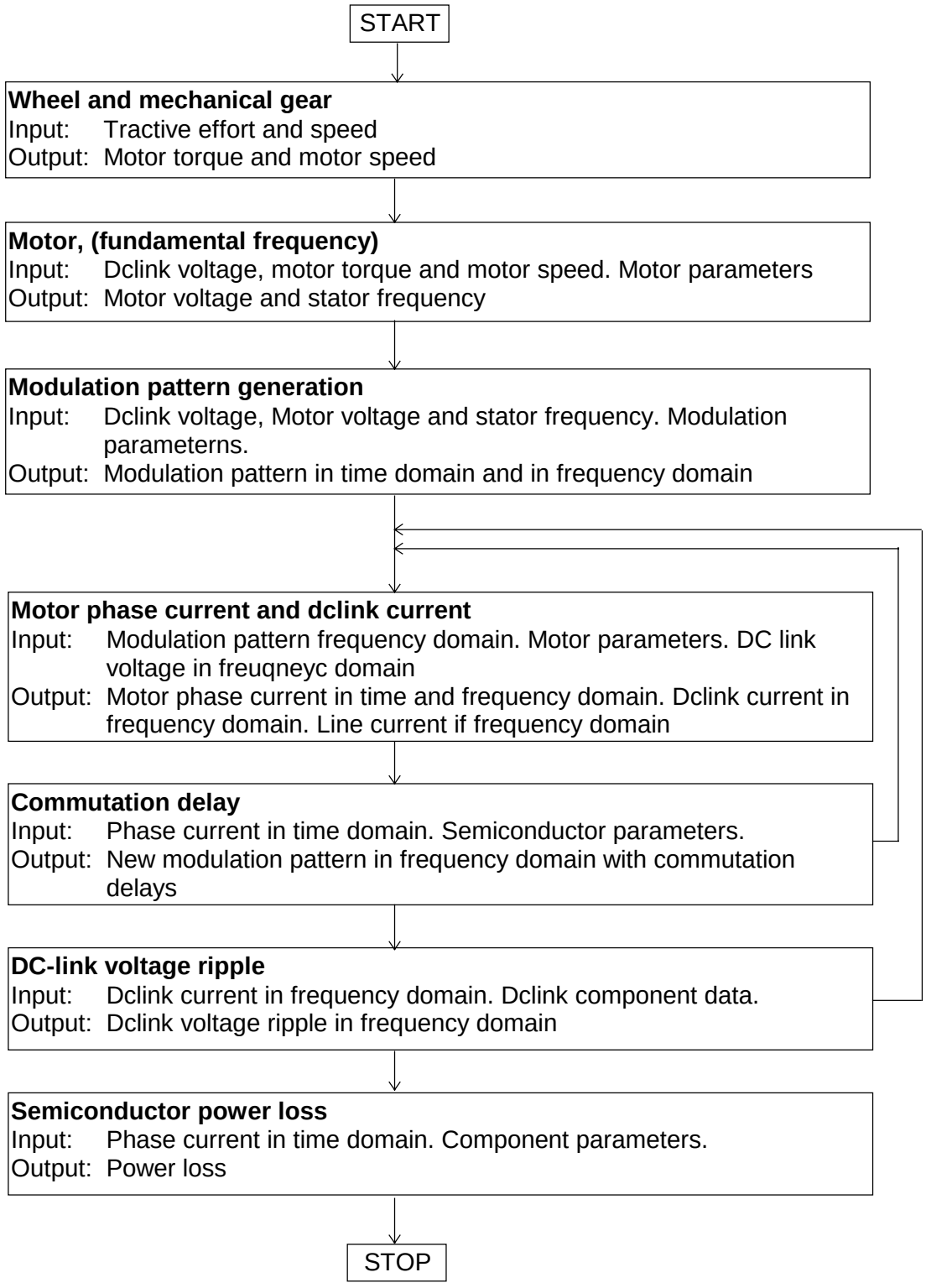

Figure 4-3. *The calculation flow when calculation of the DC supplied drive system*

Ascalp calculation of an AC supplied drive system.

An AC supplied *drive*, see figure 4-4, consists of one transformer and a number of identical traction modules. A *traction module* has one DC-link and normally one second harmonic link. Sometimes also an attenuation filter link is used. A traction module consists of an arbitrary number of identical *machine inverters*, an arbitrary number of identical *three phase auxiliary inverters* and up to three identical *line converters*. All different inverter types are connected in parallel to the DC-link. Each machine inverter has an arbitrary number of identical *three phase induction motors*, connected in parallel. Each motor is mechanically connected to one *mechanical gear* and one wheel set. A traction module can have an arbitrary number of identical *brake chopper phases*.

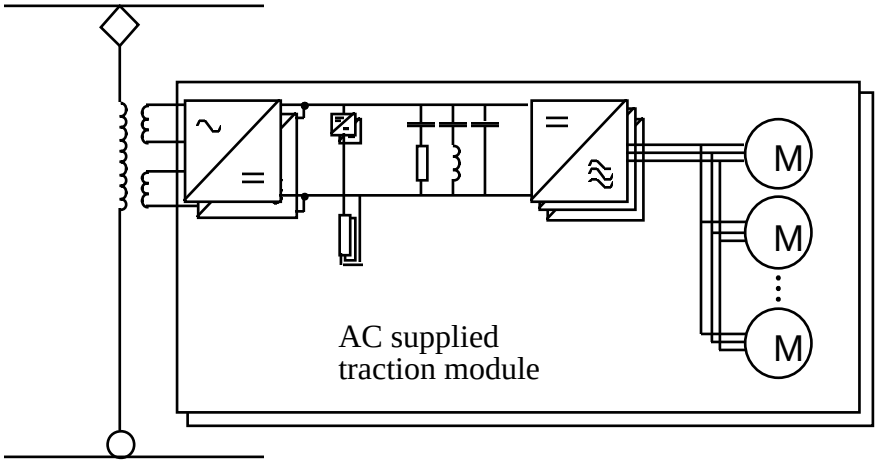

Figure 4-4. *An AC supplied drive system*

The description of the DC supplied drive system in chapter 3 ended with the calculation of the DC-link current, either based on a pure DC-link voltage or a DC-link voltage containing ripple components. The DC-link component multiplied with the DC-link voltage DC component defines the power the line converter shall produce. Based on this together with a desired unity power factor, the fundamental phase current and the corresponding fundamental bridge voltage are calculated. This calculation is based on the average leakage impedance of the transformer. The bridge voltage is split into the two phase voltages at each end of the bridge. The phase voltages have identical amplitude and a 180 degrees phase shift. The modulation pattern of each phase is found in the same way as described in chapter 3, very similar to sinusoidal modulation. The time domain modulation pattern of each phase is converted to frequency domain by means of fourier series expansion.

The complex phase voltages are found by using the fourier coefficients multiplied by the DC-link DC component. The complex phase currents are found by solving the complex equation system formed of the transformer secondary voltage vector, the line converter phase voltage vector and the transformer impedance matrix. The transformer impedance also includes the line and substation impedance. The equation system shall be solved for each harmonic frequency. The time domain phase current is found by inverse fourier series expansion. Similar to the machine converter the time domain phase current can be used to correct the original modulation pattern by taking the commutation delay and the on state voltage drop into account. With the corrected modulation pattern, the calculation shall be repeated once again, and now also the effect of commutation delay and on state voltage will be found in the result. In a similar way as in the machine converter, the time domain and frequency domain DC-link current can be found.

Assuming that all harmonics in the DC-link current will pass through the DC-links, the second harmonic filter link and a possible attenuation filter link, the frequency domain voltage ripple is calculated. The whole calculation can be repeated based on a DC-link voltage containing ripple components. In this way, it is possible to study how the interference produced by the machine converter can be modulated to the line by the line converter. Also the effect of a poorly tuned second harmonic link can be studied. If the line converter produced second harmonic DC-link current does not see a zero impedance, a second harmonic voltage ripple can be found in the DC-link voltage. This voltage will be modulated back to the line as both a fundamental line frequency component but also as a frequency with three times the line frequency, see figure 4-5.

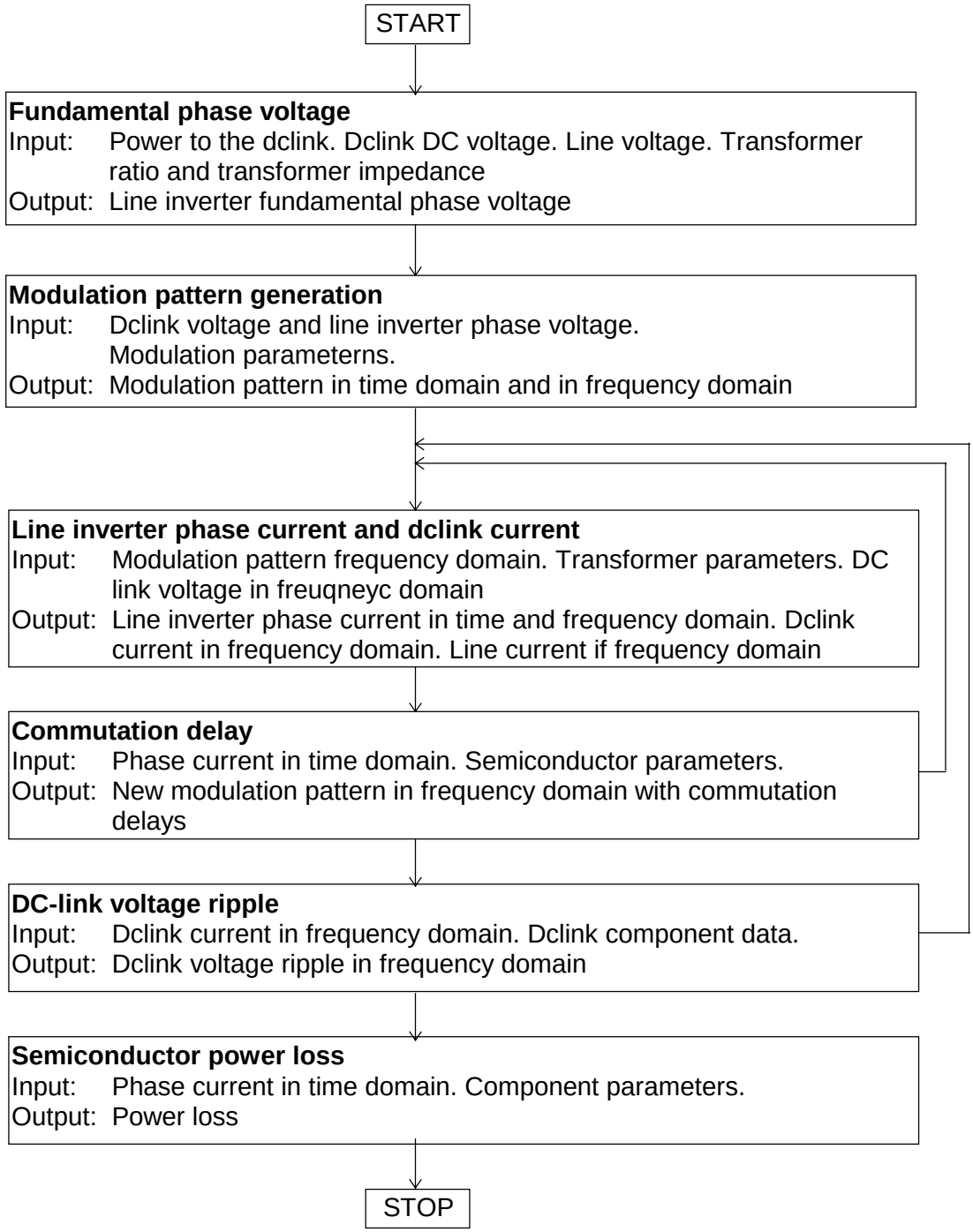

Figure 4-5. *The calculation flow when calculation the line converter in an AC supplied drive system. The calculation of the machine converter in the AC drive system, see calculation of the DC supplied drive system.*

4.2 Modulation of the three phase machine converter with ideal commutations

In this paragraph the generation of harmonics in the DC-link from a three phase inverter with three different modulation patterns is investigated. The following modulation patterns are some of the modulation patterns which can be studied;

- sinusoidal PWM
- polar modulation with 6 zero vector interval per turn (E6) and with folded corners, which gives the flux trajectory a more circular shape.
- square wave modulation.

All modulations are used in driving mode with high load. The three cases give the opportunity to study how different modulation patterns affect the generation of DC-link current harmonics. For each modulation the time domain diagram of the phase current and the frequency domain diagram of DC-link current are presented, see figure 4-6. Sinusoidal PWM is presented in figure 4-7, polar modulation in figure 4-8 and square wave modulation in figure 4-9. Data for the drive system is presented in appendix C3.

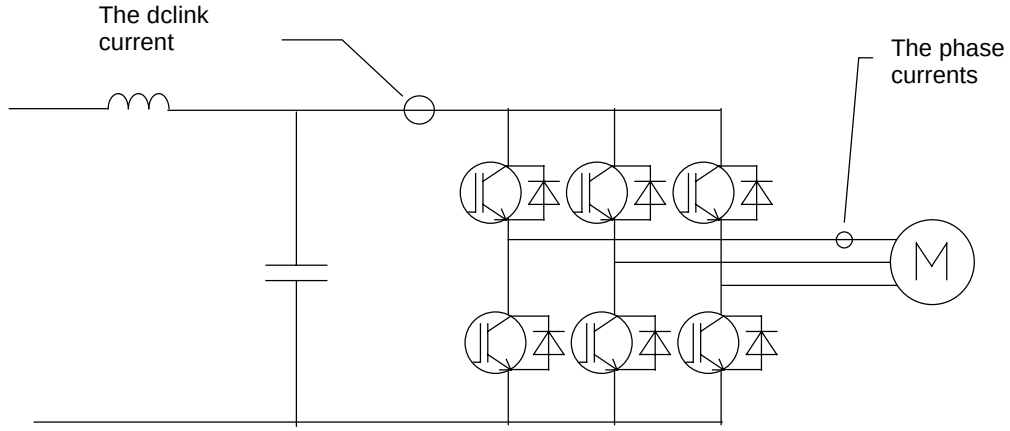

Figure 4-6. *In the three phase inverter the calculated DC-link current and the phase current are indicated.*

When sinusoidal PWM is used, the spacing between the sidebands in the DC-link current equals six times the fundamental frequency f_s. The sidebands are grouped around multiples of the switching frequency f_c, and the position of the sidebands are different around odd multiples of the switching frequency compared with even multiples, see figure 4-7:

n is an odd multiples of f_c (no odd multiples of the switching frequency is generated): $nf_c \pm 3f_s$, $nf_c \pm 9f_s$, $nf_c \pm 15f_s$, $nf_c \pm 21f_s$ etc.

n is an even multiples of f_c: nf_c, $nf_c \pm 6f_s$, $nf_c \pm 12f_s$, $nf_c \pm 18f_s$, $nf_c \pm 24f_s$ etc.

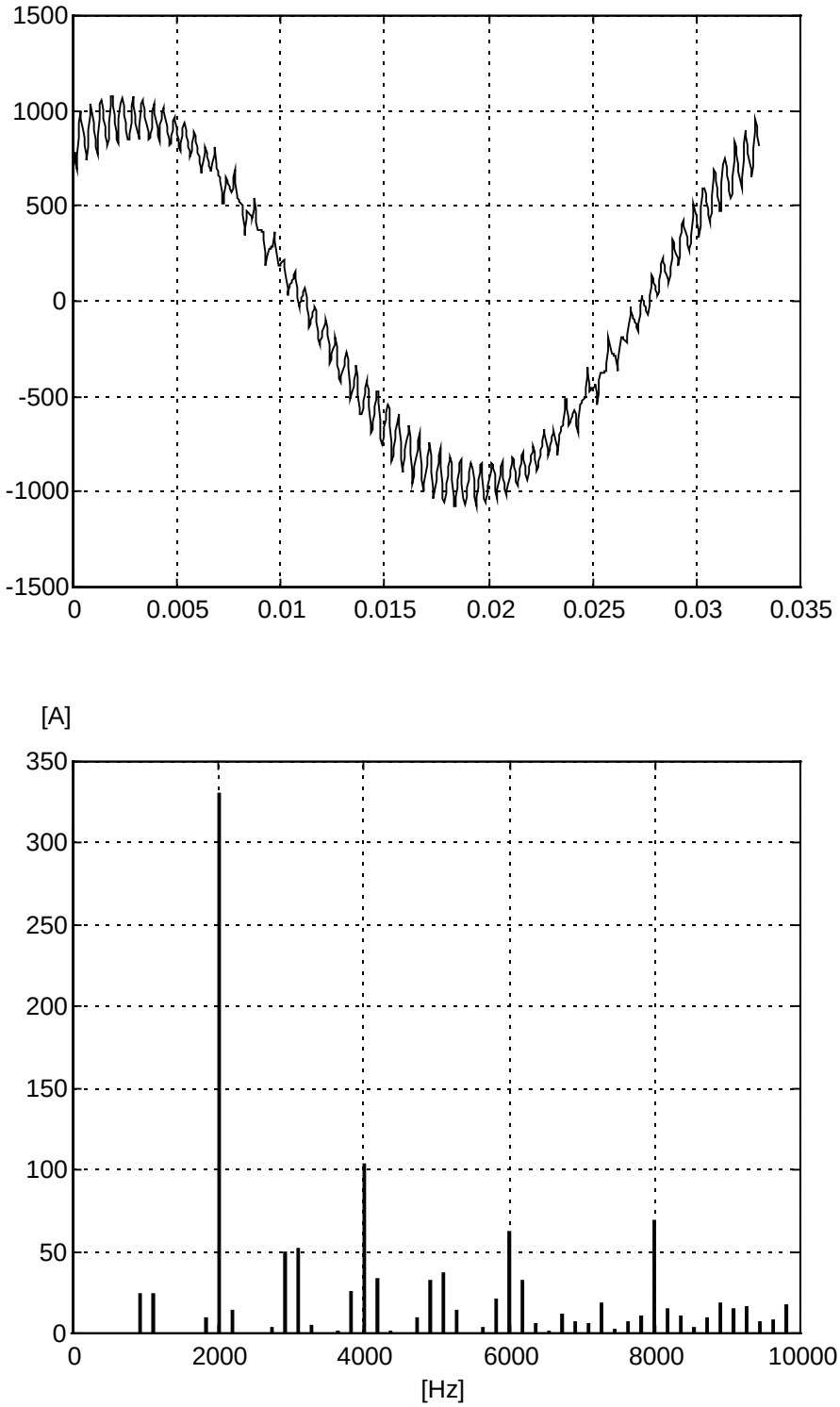

Figure 4-7. *The time domain graph of the phase current and the frequency domain graph of the DC-link current in sinusoidal PWM modulation*

Driving effort	30.0 kN
Fundamental frequency	30.3 Hz
Switching frequency	1 kHz

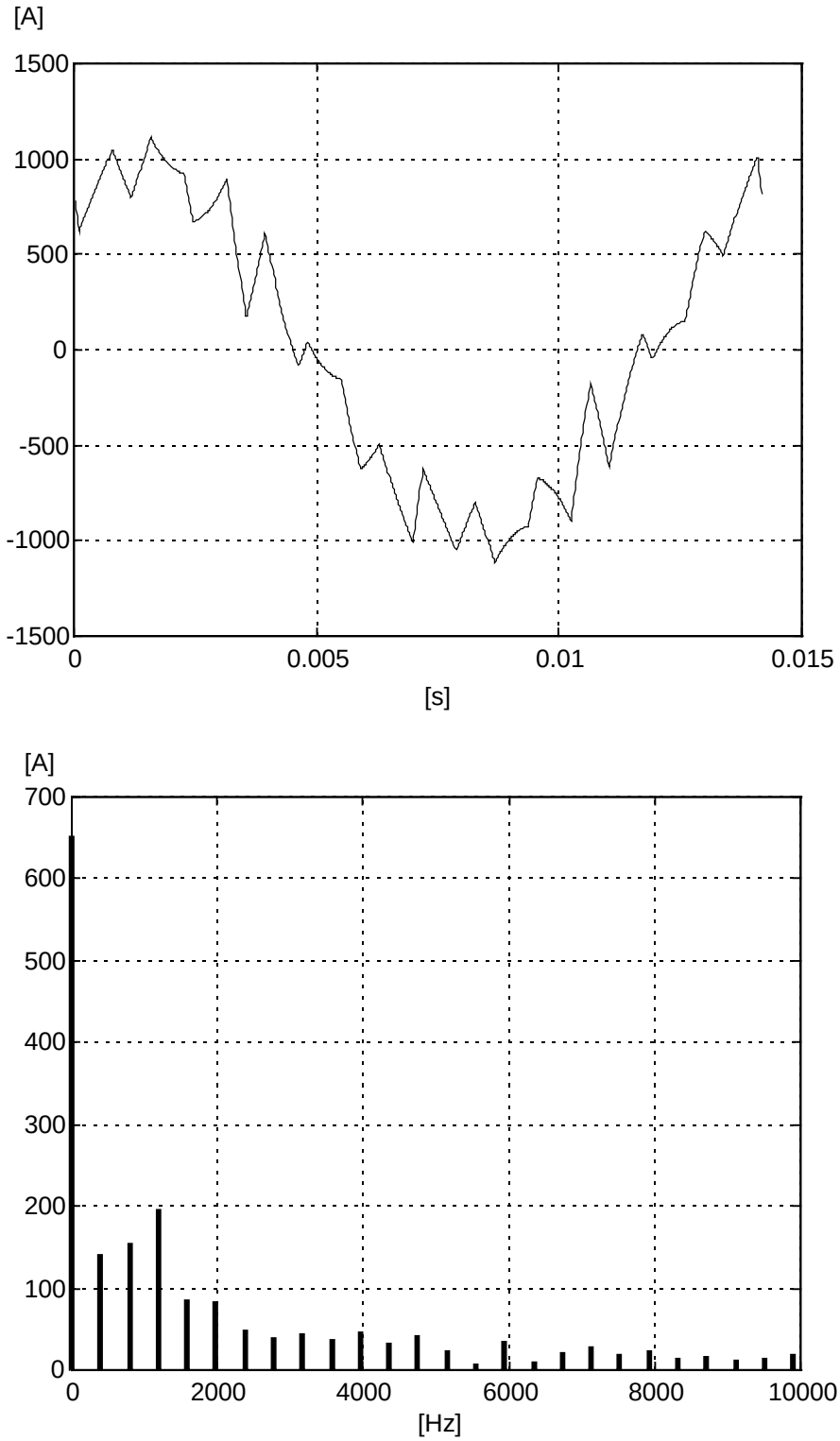

Figure 4-8. *The time domain graph of the phase current and the frequency domain graph of the DC-link current in E6 polar modulation:*

Driving effort	33.6 kN
Fundamental frequency	70.5 Hz

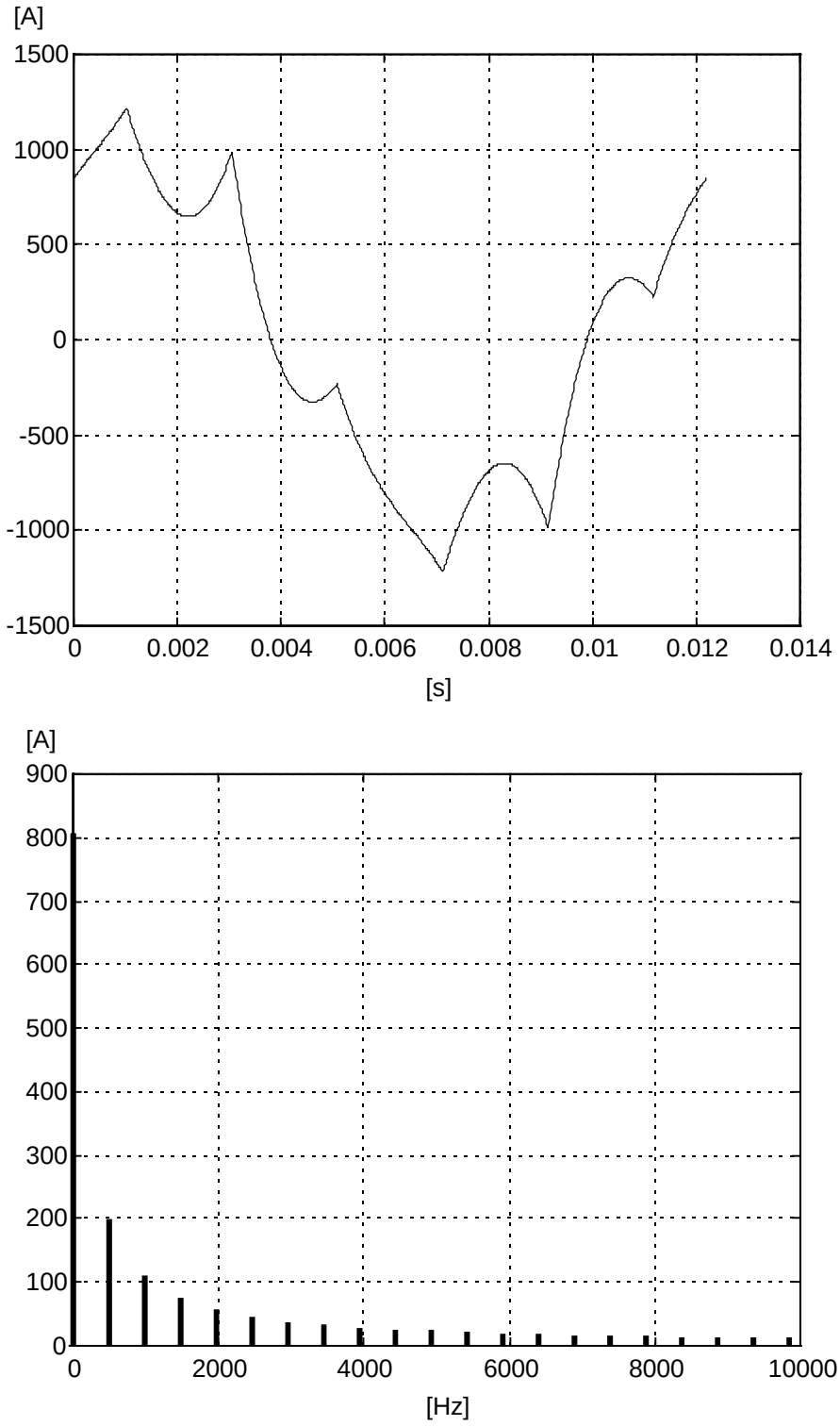

Figure 4-9. *The time domain graph of the phase current and the frequency domain graph of the DC-link current in square wave modulation.*

Driving effort	33.6 kN
Fundamental frequency	82.0 Hz

An example how low frequency harmonics are avoided

Many track circuit systems like vane track circuit, reed track circuit etc. operate with a frequency lower than 423 Hz, the upper limit for reed track circuits, see ([23]). With sinusoidal PWM the generated line interference is the switching frequency minus 3 times, 9 times, 15 times etc. the fundamental frequency, i.e., with sinusoidal PWM the line interference frequency decreases as the fundamental frequency increases. With the switching frequency 1065 Hz and the stator frequency 71 Hz, the line interference frequency has dropped to 426 Hz with sinusoidal PWM when considering the 9 times the fundamental frequency sideband. The sideband with 15 times the fundamental frequency can normally be neglected due to low current levels. If the modulation here changes to polar modulation the line interference starts to increase from 426 Hz as the fundamental frequency increases. With this modulation strategy the interference frequency is greater than 423 Hz plus the reed track circuit bandwidth. The line filter must be designed to handle only the 15 times the fundamental frequency sideband. However this presumes ideal commutations.

4.3 Modulation of a double bridge line converter with ideal commutations, with and without interlacing

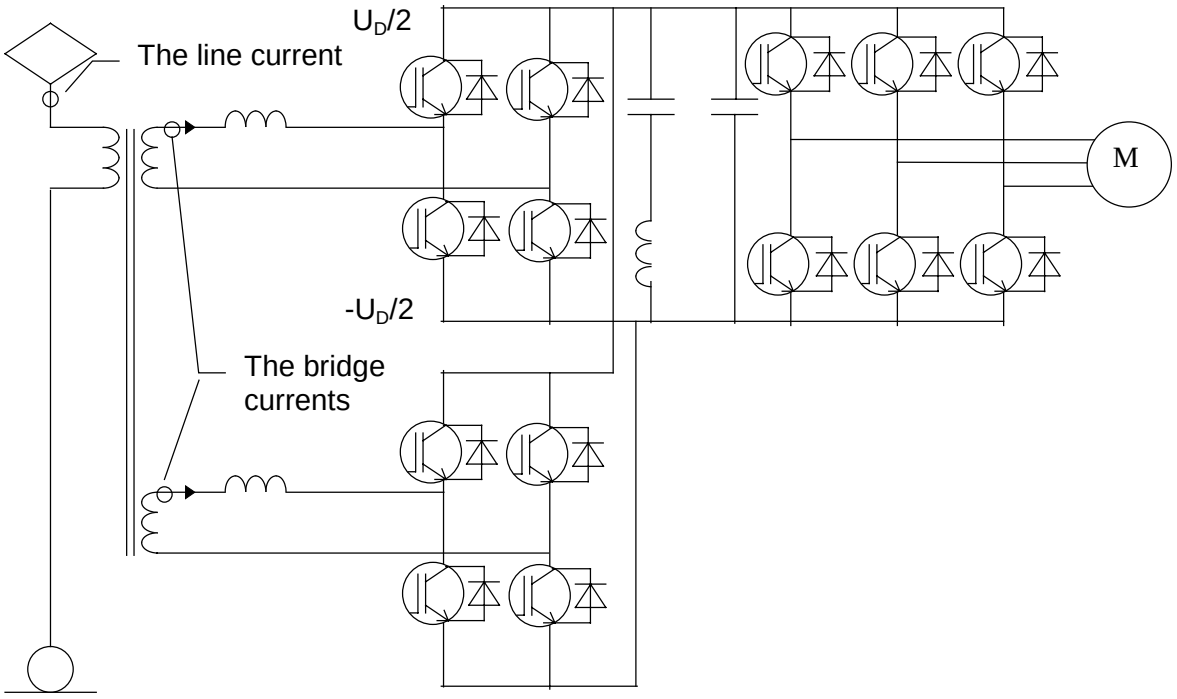

Figure 4-10. *In the double bridge line converter the two bridge currents and the line current are indicated.*

In this section the production of harmonics from a line converter will be studied. Two cases, non-interlaced double bridge and double interlaced bridge, in driving mode with high load is investigated, see figure 4-10. Also in this study, the calculation program Ascalp is used. For each case the time domain diagram of the phase current(s) and frequency domain diagram of the line current will be presented. Constant load is assumed.

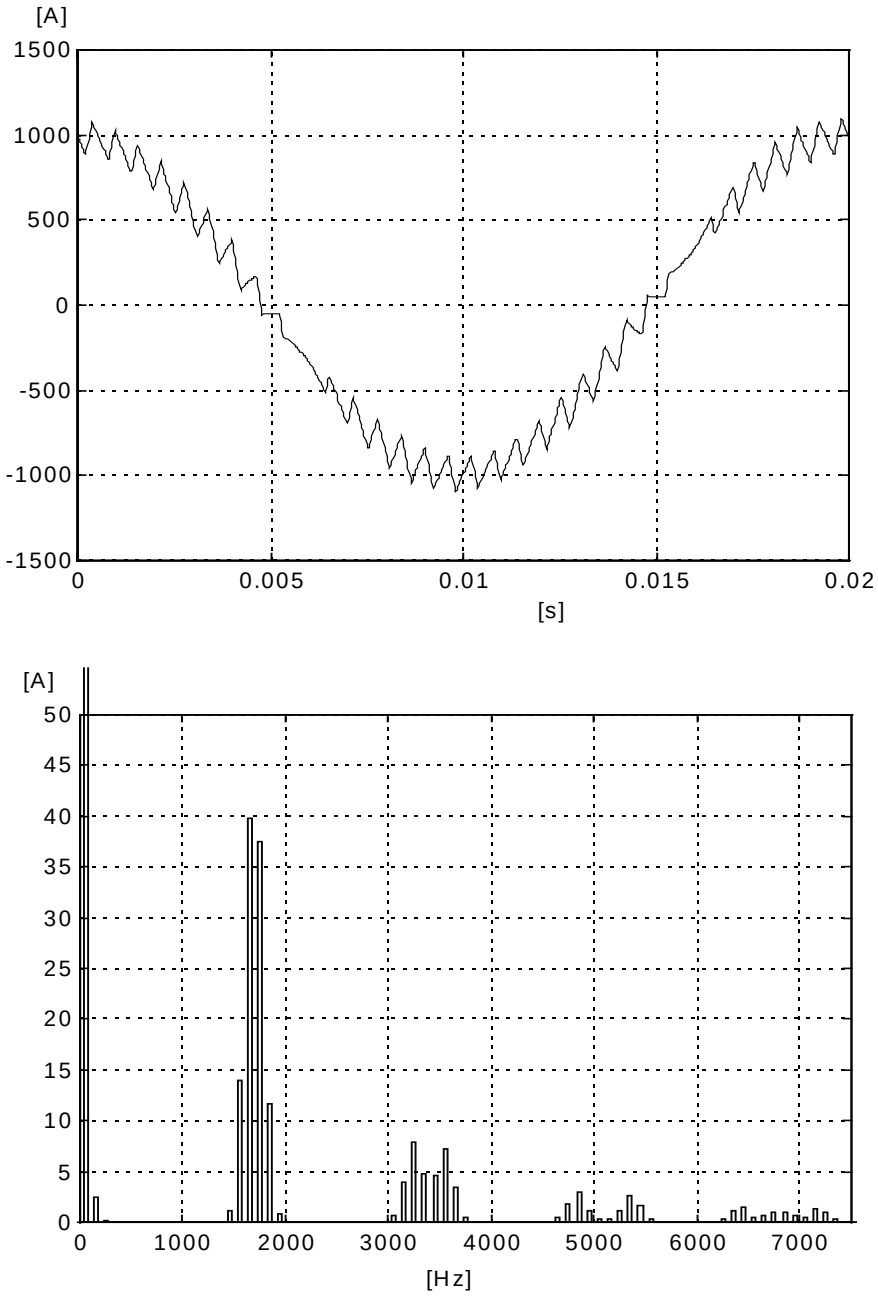

Figure 4-11. *A non-interlaced double bridge line converter. The time domain graph of the bridge current and the frequency domain graph of the line current.*

Driving effort 530 kW
Switching frequency 850 Hz

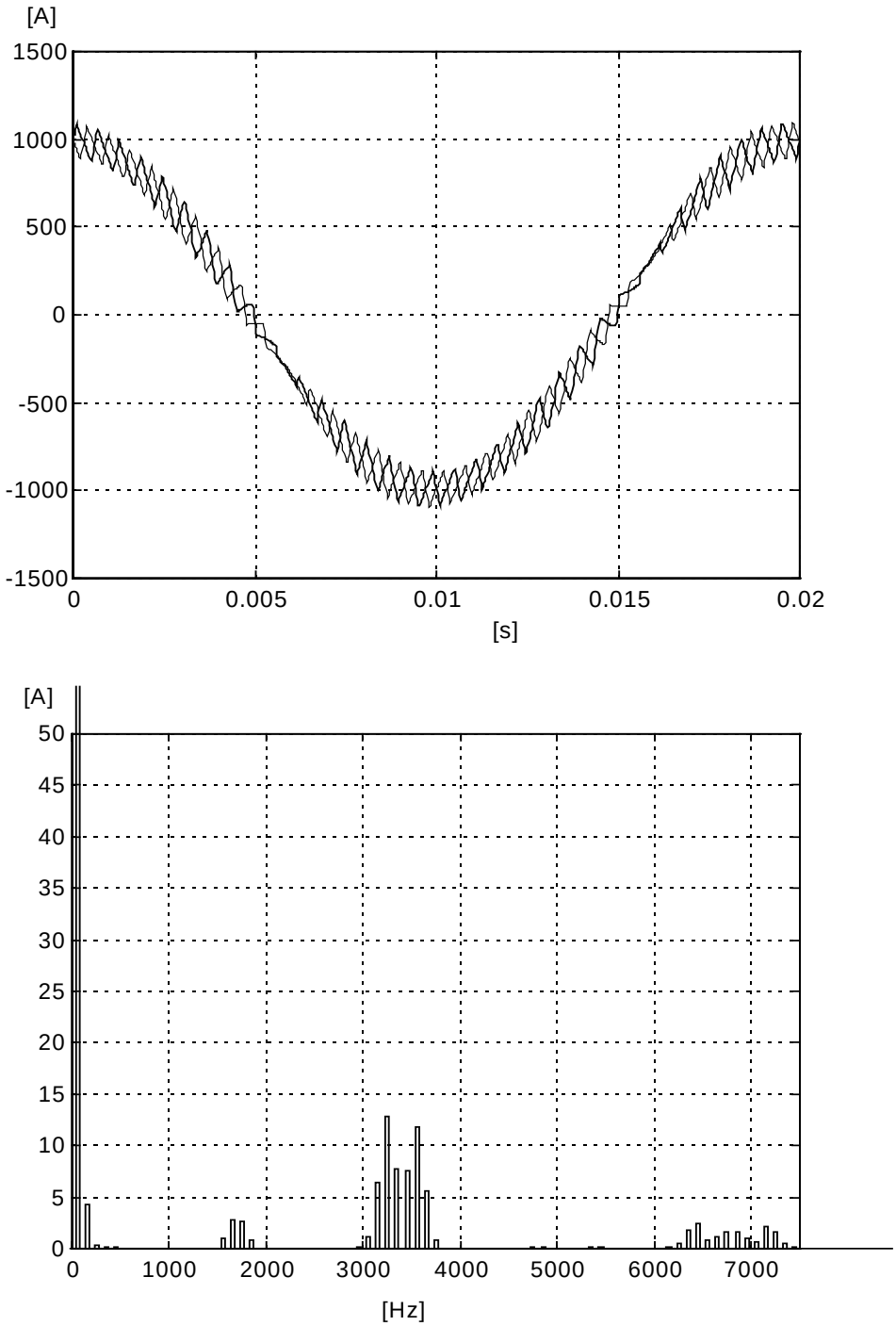

Figure 4-12. *The double bridges line converter. The time domain graph of the two bridge currents and the frequency domain graph of the line current.*

Driving effort	530 kW
Switching frequency	850 Hz

4.4 Non-ideal commutations

Due to a number of physical effects the commutation process will differ from the ideal case. In this text the effect of commutation delay and the effect of semiconductor on state voltage is studied. Below is a full commutation sequence discussed in detail, see figure 4-13.

1. At start the phase current is positive and the lower antiparallel diode is conducting. The phase output voltage is lower than zero relative to the DC bus bar, due to the diode on state voltage. A switch command is given, and a turn off order is applied to the lower transistor. However, nothing happens with the output voltage as the current is flowing through the lower antiparallel diode.

2. After a certain time, the dead time, a turn on order is given to the upper transistor. The dead time is to guarantee that the upper and lower transistors are not conducting simultaneously.

3. The turn on process starts but it takes some time before the transistor is really conducting, the delay time t_{delay_on}.

4. The upper transistor is conducting and the phase current commutates over to the upper transistor. It takes the time t_{rise} until the output voltage has changed totally.

5. Due to inductance the voltage continues to increase over the DC-link voltage, a voltage overshot is produced .

6. When the magnetic energy is consumed the overshot disappears and the output voltage is steady and slightly lower than the DC-link high voltage due to the on state voltage drop in the upper transistor.

7. A new switch command is given. The turn off order is applied to the upper transistor. After the delay time, t_{delay_off}, in the upper transistor has elapsed the transistor is non-conducting.

8. The phase current commutates over to the lower diode, without waiting for the dead time as the phase current was flowing through the upper transistor. It takes the time t_{fall} for the voltage to drop. When the current has commutated totally there will be a voltage under shot due to inductance in the circuit. After a while the undershot has disappeared and the output voltage is slightly lower than the DC- voltage due to the on state voltage drop in the lower diode.

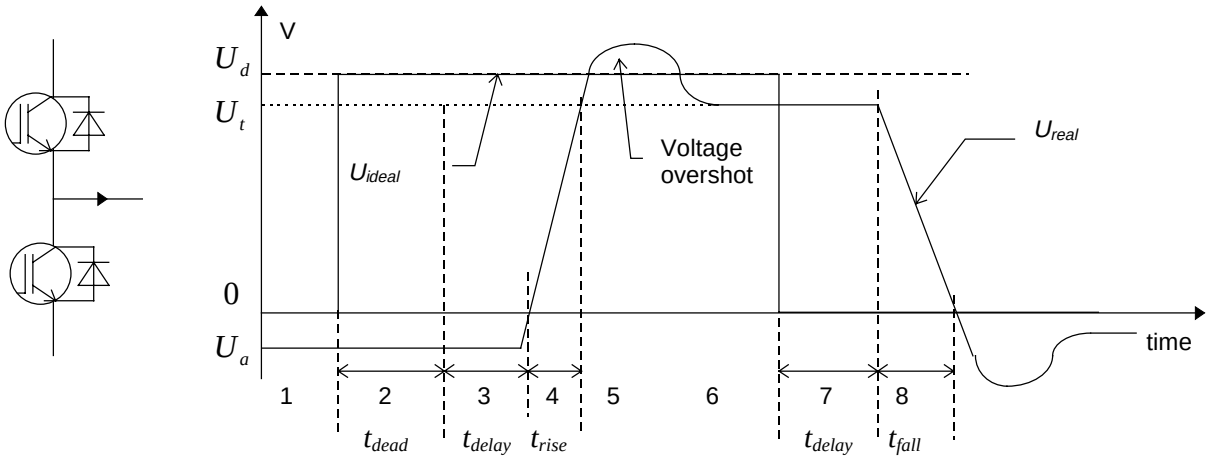

Figure 4-13 *a) The power circuit, b) The output voltage wave form*

As a consequence of the points above, the output voltage and its integral deviate from their reference values in following way:

1. In PWM sinus modulation: The dead time gives rise to a harmonic current in the DC-link with six times the fundamental frequency.

2. The commutation delay causes a voltage-time area loss.

3. The voltage overshot causes a voltage-time area gain. The difference between this volt- second area and the voltage-time area loss due to commutation delay is the effective voltage-time area loss. After division with the DC-link voltage, the effective commutation delay time is received.

4. Both the transistor (or the thyristor) and the antiparallel diode has an on state voltage drop when conducting.
   - When the upper thyristor/transistor is conducting the phase output voltage is lower than the DC-link high voltage. When the lower thyristor/transistor is conducting the phase output voltage is higher than the DC-link low voltage. At thyristor/transistor conduction the total output voltage is lower than the ideal voltage.
   - When the upper antiparallel diode is conducting the phase voltage is higher than the DC-link high voltage, and when the lower diode is conducting the phase voltage is lower than the DC-link low voltage. At diode conduction the total phase output voltage is higher than the ideal voltage.

5. A snubber has the task to decrease component stress at both turn on and turn off, mainly to decrease the component *dv/dt* at turn on and the component

di/dt at turn off. Their disadvantage is extra commutation delay and an increased voltage overshot.

Commutation delay expressions in an IGBT inverter without snubbers.

In upper transistor commutation, the phase current is positive and commutates from the upper transistor, T_u, to the lower antiparallel diode, D_l. The commutation delay:

$$t = t_{delay} + \frac{t_{rise}}{2} \qquad (4.1)$$

In lower diode commutation, the phase current is positive, and commutates from the lower antiparallel diode, D_l to the upper transistor T_u. The total commutation delay is

$$t = t_{dead} + t_{delay} + \frac{t_{rise}}{2} \qquad (4.2)$$

In lower transistor commutation, the phase current is negative and commutates from the lower transistor, T_l, to the upper antiparallel diode, D_u. The total commutation delay :

$$t = t_{delay} + \frac{t_{rise}}{2} \qquad (4.3)$$

In upper diode commutation, the phase current is negative, and commutates from the upper antiparallel diode, D_u, to the lower transistor, T_l.

$$t = t_{dead} + t_{delay} + \frac{t_{rise}}{2} \qquad (4.4)$$

Commutation delay expressions in a GTO-thyristor inverter with a snubber.

The snubber, presented in figure 4-14, is used in this investigation. In appendix A some relatively simple expressions have been developed. From these equations it will be possible to make quantitative studies of the commutation delay effects. Similar expression can be derived for any snubber. The real phase output voltage will differ from the ideal output voltage, due to loss of voltage-time area. The loss of voltage-time area is a function of both the semiconductor properties and the properties of the snubber components.

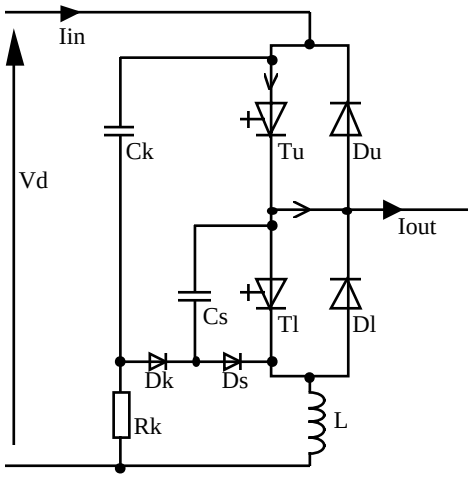

Figure 4-14. *The asymmetric snubber used at Adtranz in GTOs inverters [26].*

In the upper GTO-thyristor commutation, the phase current is positive and commutates from the upper GTO-thyristor, T_u, to the lower antiparallel diode, D_l. The commutation delay becomes:

$$t = MIN\left((k_{st} I_{out} + l_{st} + \frac{t_f}{2} + \frac{C_s}{2}(1 - \frac{C_s}{C_k})\frac{V_d}{I_{out}} - \frac{LI_{out}}{V_d}), (t_{dead} + t_{delay} + \frac{t_{rise}}{2}) \right). \quad (A1.1)$$

where $(k_{st}I_{out}+l_{st})$ forms a turn-off delay which depend on the magnitude of the commutated current. See figure 4-15.

In lower diode commutation, the phase current is positive, and commutates from the lower antiparallel diode, D_l to the upper GTO-thyristor T_u. see figure 4-15 and figure 4-16. The total commutation delay is

$$t = t_{dead} + t_{delay} + \frac{t_{rise}}{2}. \quad (A2.1)$$

In lower GTO commutation, the phase current is negative and commutates from the lower GTO-thyristor, T_l, to the upper antiparallel diode, D_u. The total commutation delay becomes:

$$t = MIN\left((l_{st} - k_{st} I_{out} + \frac{t_f}{2} - \frac{C_s}{2}\frac{V_d}{I_{out}}), (t_{dead} + t_{delay} + \frac{t_{rise}}{2}) \right). \quad (A3.1)$$

In upper diode commutation, the phase current is negative, and commutates from the upper antiparallel diode, D_u, to the lower GTO-thyristor, T_l. The total commutation delay is

$$t_2 = t_{dead} + t_{delay} + \frac{t_{rise}}{2} - L\frac{I_{out}}{V_d}. \qquad (A4.1)$$

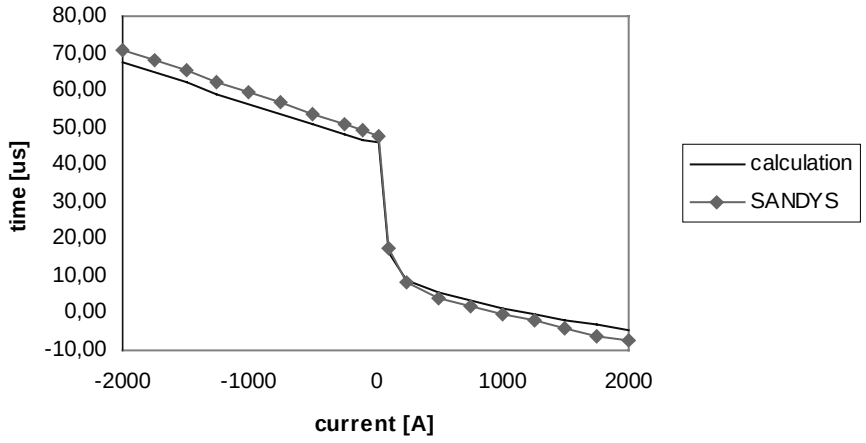

Figure 4-15. *Commutation delay in [ms] in upper GTO-thyristor/antiparallel diode versus commutated current, see eq. (A1.1) and (A4.1).*

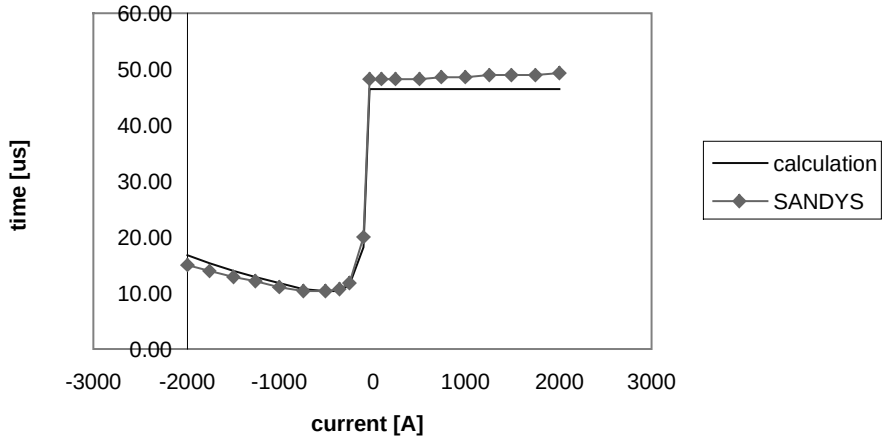

Figure 4-16. *Commutation delay in [ms] in lower GTO-thyristor/antiparallel diode versus commutated current(A2.1) and (A3.1).*

The algorithms are compared with simulations in SANDYS (a simulation program for dynamic simulations, used at ABB) of the voltage-area loss in the snubber circuit. The upper GTO-thyristor together with the upper diode commutation delay is depicted in figure 4-15, and the lower GTO-thyristor together with the lower diode commutation delay is depicted in figure 4-16.

4.5 Asymmetry

An asymmetry is defined as a commutation delay, an on state voltage drop etc. which is not identical in all phases or in all component positions in an inverter.

A *phase asymmetry* is present in a three phase inverter if one of the inverter phases is different from the other two. A typical origin for this kind of asymmetry is an asymmetric three phase load connected to an auxiliary inverter. Another origin can be variation in data of a snubber component, shared by both upper and lower position semiconductor. This asymmetry will create a component in the DC-link current with twice the fundamental frequency.

An *upper/lower asymmetry* is present when the commutation properties of the upper position semiconductor in all three phases is different from the lower position semiconductor. A typical example of this asymmetry is an asymmetric snubber, which will be present even with semiconductors and snubber components with nominal data. This asymmetry will give a third harmonic in the DC-link.

Position asymmetry is present when a semiconductor in one position in the inverter has different commutation properties than the other semiconductors in the inverter. For instance, if a semiconductor in upper position has a turn-on characteristic which is more delayed than the nominal value,”one”-pulses with shorter duration than the ”zero”-pulses in the same phase will be created. It will also be shorter than the ”one”-pulse in the other phases. In an ideal voltage source inverter phase the average output phase voltage will be exactly half the DC-link voltage. However, if the ”one”-pulse has shorter duration than the ”zero”-pulse, the average output phase voltage will be $-\varepsilon$, i.e., a slightly lower voltage than half the DC-link voltage. If the other phases have exactly half the DC-link voltage, there will be a DC current component flowing between the phases, see figure 4-17. These DC current components will be modulated by the machine converter to the DC-link side and will be found there as a fundamental frequency current. Position asymmetry can be regarded as a combination of phase asymmetry and upper/lower asymmetry.

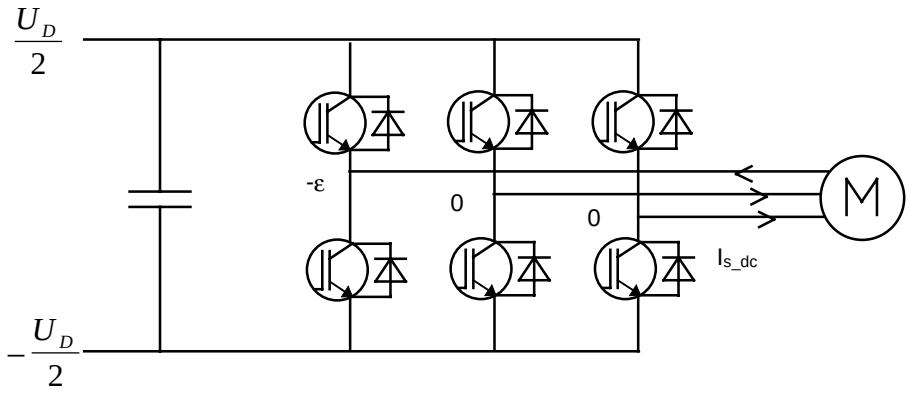

Figure 4-17. *Normally the average phase voltage shall be half of the DC-link voltage. Due to position asymmetry the average voltage will differ slightly from this value.*

Fast/slow semiconductors

The origin for this asymmetry is mainly a variation in commutation properties among the semiconductors. On this stage of the description an assumption of the semiconductor generation of charge carriers can be made. One semiconductor which easily creates charge carriers will turn on rapidly, turn off slowly and will have a low on state voltage. These components are called *"fast"*. The opposite, a *"slow"* semiconductor will turn on slowly, turn off rapidly and have a high on-state voltage. This assumption is not verified experimentally but is probably true for semiconductors of the same type and especially if they are produced in the same batch.

If a slow semiconductor is used in upper position in a phase and if the lower position semiconductor is normal, the phase will produce "one"-pulses with shorter duration and lower amplitude, and therefore their voltage-time area will be reduced. This asymmetry will be increased if a fast semiconductor instead is used in lower position. If then fast semiconductor are used in upper positions and slow in lower positions in the other two phases the worst case position-asymmetry is formed.

If slow semiconductors are located in all upper positions and fast semiconductors in all lower positions, we have created upper/lower-asymmetry.

DC biased phase current transducers

If the phase current transducers are DC-biased on the signal amplifier side, the control system will interpret the situation as there is a DC-component in the phase current and will try to cancel it, i.e., to add a DC-component with

opposite sign to the phase current. This real DC-component will be modulated by the modulator to a current in the DC-link with fundamental frequency.

4.6 The generation of low frequency harmonics

With the program Ascalp the current in the DC-link is calculated, and the effect of different asymmetries can be found. So far there are limited data available concerning the turn on/turn off delay properties of IGBTs. The lack of data makes it difficult to make careful statistical analysis of realistic commutation delays. Instead typical data measured from a limited number of IGBTs have been used in this work:

- ”fast” IGBT: Turn on delay 0.8 μs.
- ”fast” IGBT: Turn off delay 1.2 μs.
- ”slow” IGBT: Turn on delay 1.2 μs.
- ”slow” IGBT: Turn off delay 0.8 μs.

Different combination of how fast and slow components can be put in an inverter have been used in order to form the different types of asymmetries, and in the calculations the worst case asymmetry is assumed. The dead time effect has also been calculated. The 10 lowest harmonics in the DC-link current are presented in frequency domain graphs with logarithmic current axis.

The first example is the frequency domain DC-link current generated with ideal commutations. In the case, presented in figure 4-18, the following data have been used:

Stator frequency	30.3 Hz
Switching frequency	1 kHz
DC-link voltage	750 VDC

Ideal commutations.

Sinusoidal modulation is supposed to generate a circular flux trajectory and the harmonic with six times the fundamental frequency is not supposed to be present. However, as can be seen in figure 3-13, even in sinusoidal modulation the trajectory can be rather hexagon shaped. That is the explanation why the harmonic is found.

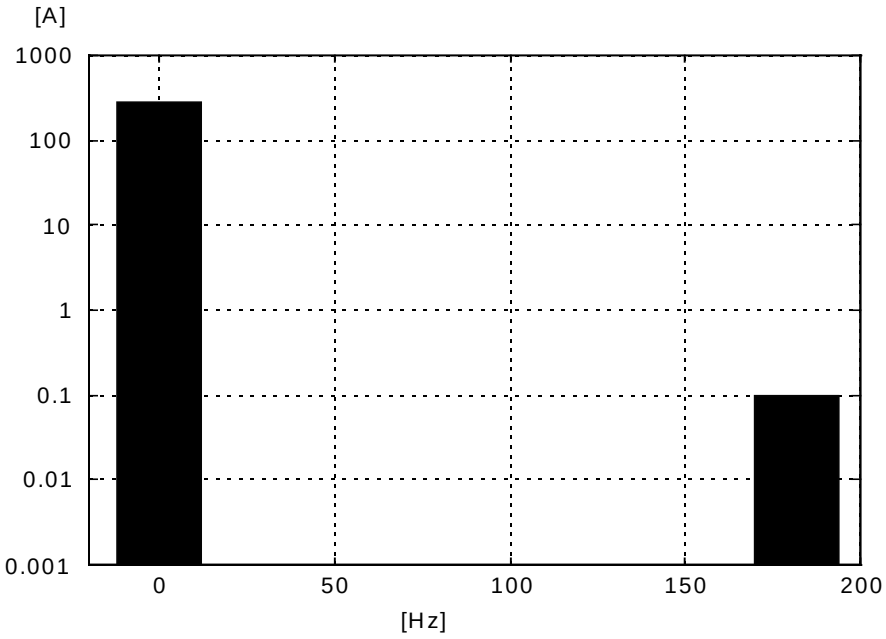

Figure 4-18. *Even with ideal commutations a small amount of a harmonic with six times the fundamental frequency can be found*

The dead time effect.

A dead time of 10 μs is used in this calculation. The dead time is the same in all three phases, see figure 4-19. The harmonic with six times the fundamental frequency has increased 30 times compared to the ideal case.

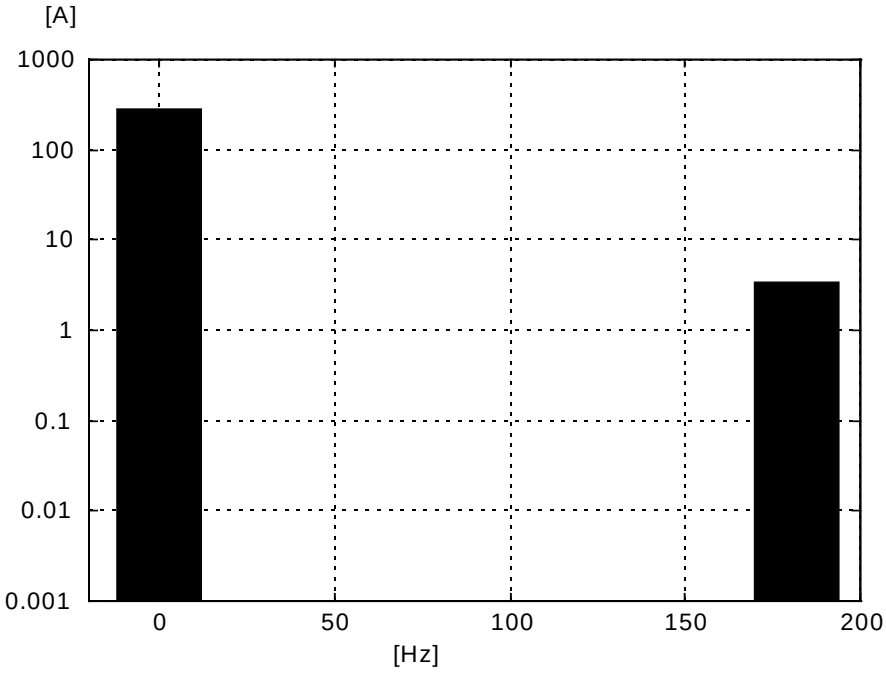

Figure 4-19. *The dead time causes a harmonic in the DC-link current with six times the fundamental frequency*

The phase asymmetry

In this calculation two phases are identical and the third is different. However, in each phase upper and lower position are identical. Therefore a fast component is located in both upper and lower position in phase R. The semiconductors in phase S and T are identical and are neither fast nor slow. With phase asymmetry the stator flux trajectory becomes slightly elliptic, which together with the circular rotor-current trajectory, generates a low-frequency torque, which varies with twice the fundamental frequency. Therefore both the power and the DC-link current have a frequency component with twice the fundamental frequency, see figure 4-20 and figure 4-21.

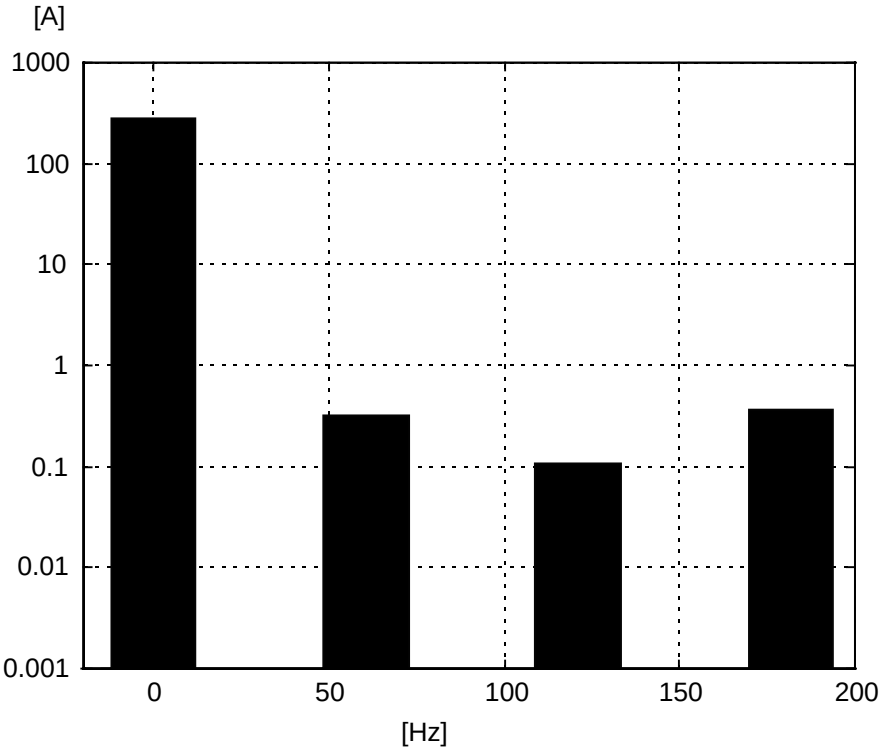

Figure 4-20. *In phase asymmetry a harmonic with two times the fundamental frequency and a harmonic with four times the fundamental frequency are produced. Also a harmonic with six times the fundamental frequency is present.*

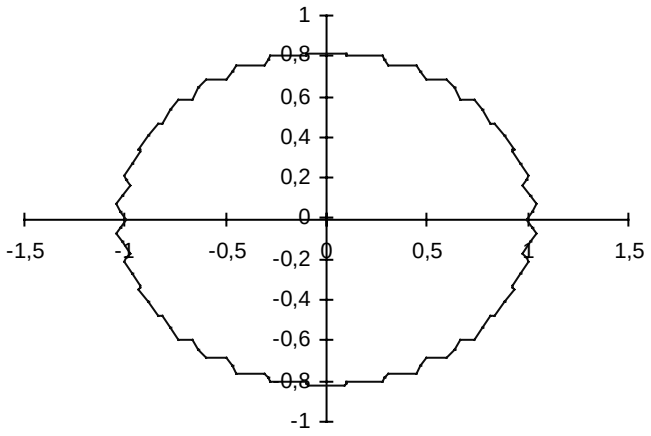

Figure 4-21 *The phase asymmetry gives rise to a slightly elliptic-shaped flux-trajectory. The impact of phase asymmetry on the flux trajectory is exaggerated in this picture.*

Upper / lower asymmetry

In this calculation all three phases are identical. However, in each phase upper position and lower position are different. Therefore fast components are located in upper position and slow components in lower position in all three phases.

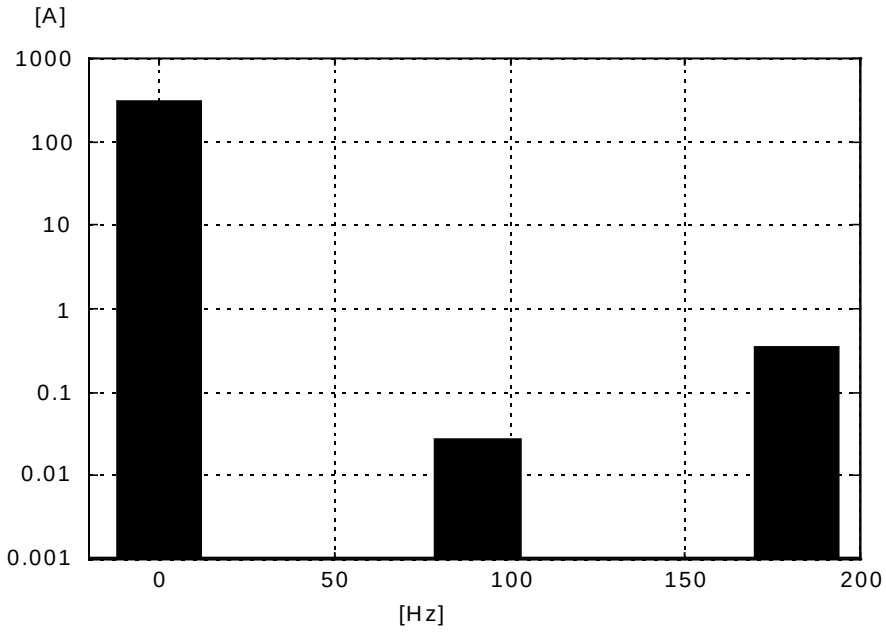

Figure 4-22. *In upper/lower-asymmetry a harmonic with three times the fundamental frequency and a harmonic with six times the fundamental frequency are present.*

With upper/lower-asymmetry the stator flux trajectory is slightly egg-shaped, which together with the circular rotor-current trajectory, generates a low-

frequency torque, which varies with three times the fundamental frequency. Therefore both the power and the DC-link current have a frequency component with three times the fundamental frequency, see figure 4-22 and figure 4-23.

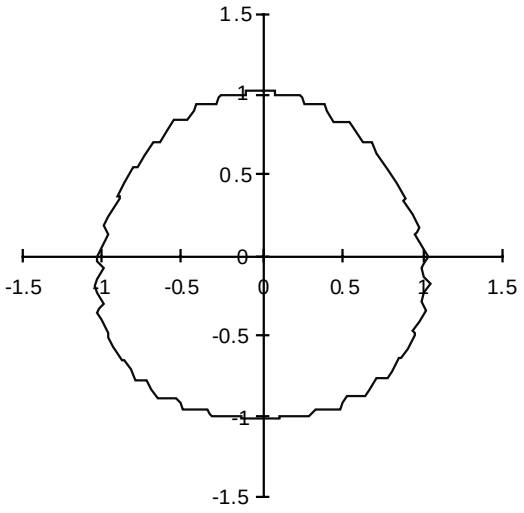

Figure 4-23 *The upper/lower asymmetry gives rise to an egg-shaped flux trajectory. The impact of upper/lower-asymmetry on the flux-trajectory is exaggerated in this picture.*

Position asymmetry

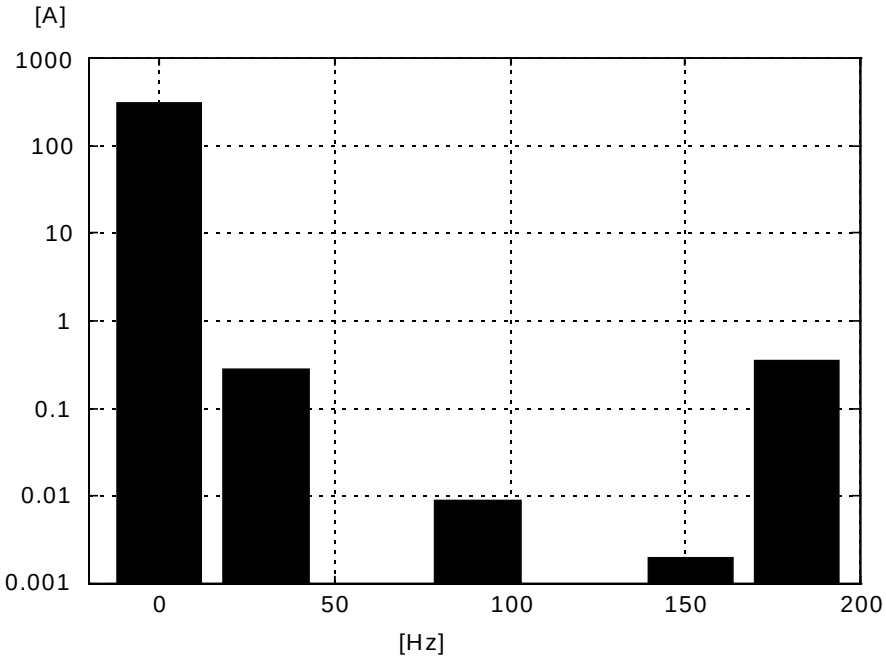

Figure 4-24. *In position asymmetry a fundamental harmonic is present. Also a harmonic with three times the fundamental frequency can be found.*

Fast components are used in upper position in phase R and in lower positions in both phase S and T. Slow components are used in the other positions. With position-asymmetry the stator flux trajectory is eccentric, which together with the circular rotor-current trajectory, generates a low-frequency torque, which varies with the fundamental frequency. Therefore both the power and the DC-link current have a fundamental frequency component, see figure 4-24 and figure 4-25.

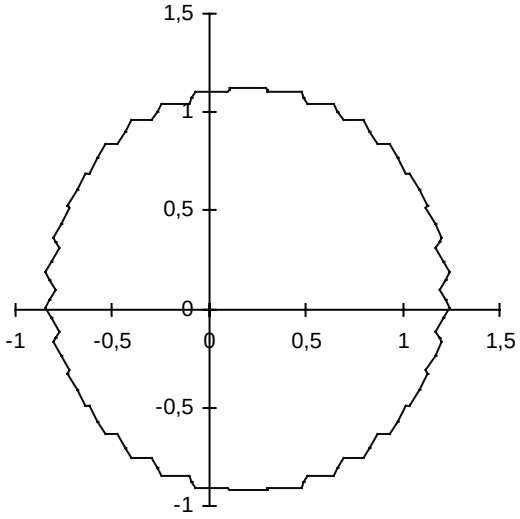

Figure 4-25 *The position asymmetry gives rise to an eccentric flux trajectory. The impact of position-asymmetry on the flux-trajectory is exaggerated in this picture.*

4.7 Conclusions on asymmetries

In this chapter it has been found that it is possible to detect the presence of asymmetries by measuring the DC-link current. The information found in the DC-link will be used to compensate for the asymmetries. In the next chapter the following compensation methods will be studied:

- dead time compensation
- position asymmetry compensation
- DC biased transducer compensation

5 Compensation Methods

In chapter 4, it was studied which influence the dead time had on the output voltage from a three phase inverter, and how a DC-link current component with six times the fundamental frequency is generated. It was also studied how different kinds of commutation asymmetries generate current components in the DC-link current with certain frequencies. At the end of section 4.2, it is demonstrated how the choice of modulation strategy can be done in order to avoid line harmonics lower than a certain frequency. However, the strategy presumes ideal commutations and with non ideal commutation also low frequency harmonics will be generated.

In this chapter the following compensations methods will be presented:

- **Dead time compensation.** A combined method will be proposed. First it is checked if the next commutation in a phase branch is a transistor or a diode commutation. At transistor commutation there is no delay. At diode commutation the commutation is delayed one dead time. This is handled in a feed-forward method, combined with a feedback method, where the differential of the integral of the inverter output voltage, or rather the output flux will be compared with the voltage time area reference. The difference will be fed back to a control system which adds to the flux reference and thereby reduces the dead time effect. The dead time compensation is formed of an ideal delay feed forward and a non ideal delay feed back. The dead time compensation corrects the output voltage, Δu.
- **Position asymmetry compensation.** In a three phase inverter with position asymmetry, as mentioned earlier, a fundamental frequency current component will be found in the DC-link and a DC component will be found in all three, or at least in two, phase currents. The idea of a compensation method is to feed back the information, either in the DC-link current or in the phase currents, to a control system which reduces the effects of position asymmetry. Here one principle is suggested, which uses the information in the phase current. The position asymmetry compensation corrects the output voltage, Δu.
- **DC biased phase current transducer.** The phase currents are normally measured with Hall element current transducers. Such transducers have one disadvantage, their output to the electronic control circuitry can be DC biased. The control system tries to cancel a virtual DC component by forcing the inverter to produce a real DC component with opposite sign. As the reason for this action is virtual, the effect will be a real DC component in the phase currents and thus a fundamental frequency component in the DC-link

current. The effect is very similar to the effect of position asymmetry, and can also be used to compensate position asymmetry. The current transducer DC bias compensation corrects the output voltage, Δu and the phase current Δi.

5.1 Dead time compensation

Compensation principle.

There are different ways to compensate the loss of voltage time area caused by the dead time. In section 4.4 we have found that at transistor commutations the commutated current immediately commutates over to the diode in opposite position in the phase, i.e. at transistor commutation there is no loss of voltage time area. At a diode commutation the current continues to flow through the diode even when the transistor is turned off, until the transistor in the opposite position of the phase is turned on, i.e. the change in output voltage is delayed one dead time. This effect can be quantified, see the diagrams in figure 4-15 and in figure 4-16, where the commutation delay for a phase with snubbers was presented. Similar diagrams can be formed for all kinds of snubber and snubber-less commutations.

The first method proposed is a *feed forward method*. The technique is to check the sign of the phase current at the modulation pattern change. If a transistor commutation is expected, the modulation pattern change shall be delayed one dead time and if a diode commutation is expected no extra delay shall be introduced. In this way, all commutations will be delayed one dead time. The opposite is also possible, at an expected diode commutation the modulation pattern change can be done one dead time earlier. The advantage with the latter method is that all commutation will be at the expected instant.

The *feed back method* is to measure the inverter output voltage and then integrate it to form the motor (terminal) flux. This flux is compared with the flux reference. The difference is the actual loss of voltage time area, which will be fed back to the control system and added to the next output voltage time area reference for compensation. The loss is mainly due to the dead time effect but also other effects of asymmetry can partly be compensated.

These two methods can preferably be combined. The known nominal loss of voltage-time area will first be compensated in a feed-forward loop, as described above, and the remaining error due to non-nominal effects will thereafter be compensated in a feedback loop.

In the following a more detailed study of the latter method will be done.

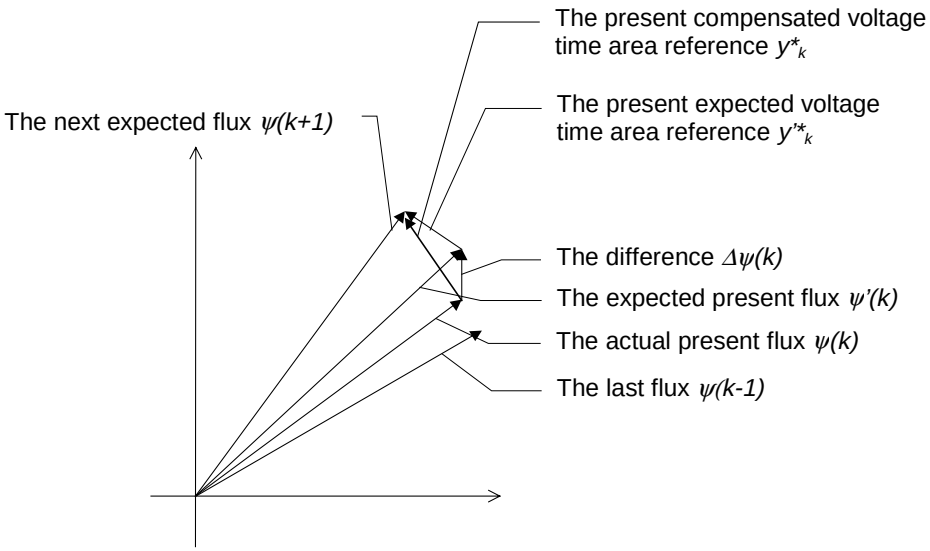

Figure 5-1. *The principle for the dead time compensation*

At the last sample the voltage time area reference was y^*_{k-1}
Due to the dead time the realised flux was not the expected. The error

$$\varepsilon_k = y^*_{k-1} - (\psi(k) - \psi(k-1))$$

can then be added to the next present voltage-time area reference, y^*_{ko}. The total present voltage-time area reference is than obtained as

$$y^*_k = y'^*_{k0} + \varepsilon_k$$

Stability analysis

In order to analyse the stability of the proposed method for compensation of dead time effects, a simplified model of the control system is made, see figure 5-2. The control system is scalar, not vectorial, and the flux controller purely proportional (gain k_1). The delay of a ”fast” or ”slow” computer is included, as well as an external error source to account for the voltage time area error due to dead time effects.

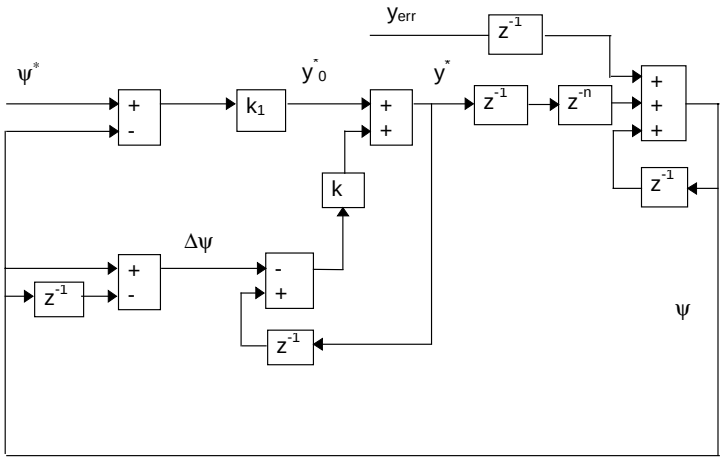

Figure 5-2 *The control system of the dead time compensation. The delay z^{-n} is used to demonstrate the difference between a measurement without delay (n=0, and a measurement with a one sample delay (n=1).*

Referring to figure 5-2 we have the relations:

$$\begin{cases} y_0{}^* = k_1 \cdot \left(\psi^* - \psi\right) \\ \Delta\psi = \psi - \psi \cdot z^{-1} = \psi \cdot (1 - z^{-1}) \\ y^* = y_0^* + k \cdot \left(y^* \cdot z^{-1} - \Delta\psi\right) \\ \psi = y^* \cdot z^{-(1+n)} + y_{err} \cdot z^{-1} + \psi \cdot z^{-1} \end{cases}$$

$$\begin{cases} y^* = k_1 \cdot \left(\psi^* - \psi\right) + k \cdot \left(y^* \cdot z^{-1} - \psi \cdot \left(1 - z^{-1}\right)\right) \\ y^* \cdot z^{-(1+n)} = \psi \cdot \left(1 - z^{-1}\right) - y_{err} \cdot z^{-1} \end{cases}$$

$$\psi = \psi^* \cdot \frac{k_1 \cdot z^{-(1+n)}}{z^{(2+n)} - z^{(1+n)} \cdot (k+1) + z^n \cdot k + z \cdot (k_1 + k) - k} +$$

$$+ y_{err} \cdot \frac{z^{-1} \cdot \left(1 - k \cdot z^{-1}\right)}{z^{(2+n)} - z^{(1+n)} \cdot (k+1) + z^n \cdot k + z \cdot (k_1 + k) - k}$$

The characteristic equation is

$$z^{(2+n)} - z^{(1+n)} \cdot (k+1) + z^n \cdot k + z \cdot (k_1 + k) - k = 0$$

If the roots of the characteristic equation are located inside the unit circle the system is stable. ([22] page 320).

The tests are performed with two different measurement delays:

- a test with no measurement delay; *n=0*

- a test where the measurements are delayed one sample; *n=1*

No measurement delay.

The characteristic equation for *n=0* becomes:

$$z^2 + z \cdot (k_1 - 1) = 0$$

$$\begin{cases} z_1 = 0 \\ z_2 = 1 - k_1 \end{cases}$$

The root z_2 is situated inside the unit circle if $0 < k_1 < 2$.

One sample delay.

The characteristic equation for *n=1* is:

$$z^3 - z^2 \cdot (k+1) + z \cdot (k_1 + 2 * k) - k = 0$$

The first step in this investigation is to decide which gain, the value of k_1, that shall be used in the normal flux control. For this test *k* in the characteristic equation is set to zero, i.e. the compensation is cancelled.

The characteristic equation becomes:

$$z^3 - z^2 + z \cdot k_1 = 0$$

The system is stable in the interval $0<k_1<1$, as the poles then are situated inside the unit circle. In the smaller interval $0<k_1<0.25$ all roots are real, which is advantageous concerning oscillations. This latter case is presented in figure 5-3.

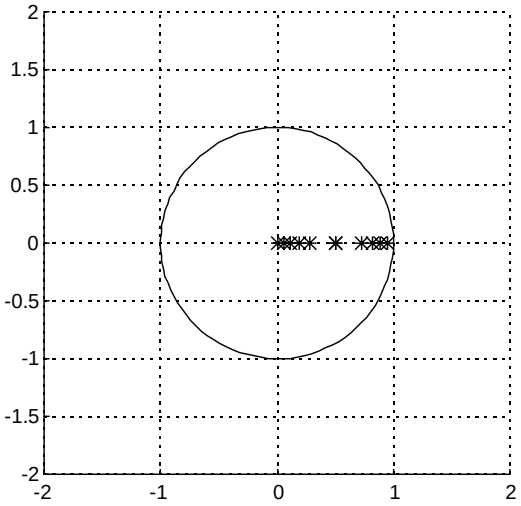

Figure 5-3 *The theoretical root loci for the flux control syste, gain k_1=0...0.25, with one sample period measurement delay and no feed back compensation.*

The next step in the investigation is to find a suitable gain k in the compensation feed back loop. The characteristic equation is analysed for k_1=0.1 and k_1=0.25, and the intervals where the feed back gain k gives a stable system is calculated. The results are presented in table 5-1. Figure 5-4 shows the corresponding root loci.

Table 5-1 *Stable combinations of flux controller gain and kompensation feedback gain*

Flux controller gain k_1	**Compensation feedback gain k**
0.1	- 0.52 ... + 0.89
0.25	- 0.56 ... + 0.74

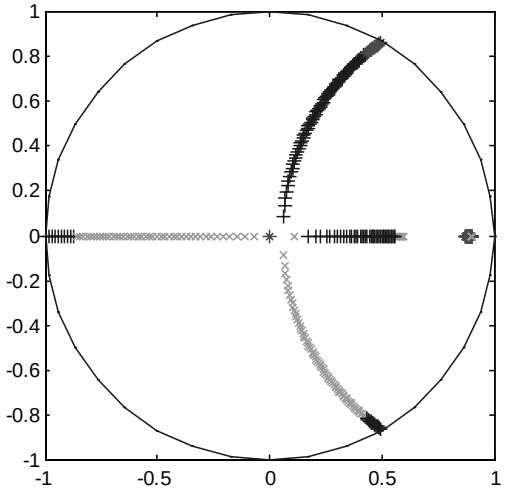

Figure 5-4 *The theoretical result of the stability analysis for the test with the dead time compensation system included. The system is stable as the poles are situated inside the unit circle. k_1=0.1 and –0.52<k<0.89.*

Simulated results

In order to illustrate the dynamic effects of the flux control and the compensation feed back, six simulations are made on the system shown in figure 5-2. The two different flux control gains in table 5-1 are simulated together with the three different compensation feedback gains k= [0 0.35 0.7]. The sampling time is T_s=0.1 ms. The flux reference makes a step from zero to one at t=1 ms, and the voltage time area error y_{error}=0.01 is imposed at t=5 ms. The results are shown in figure 5-

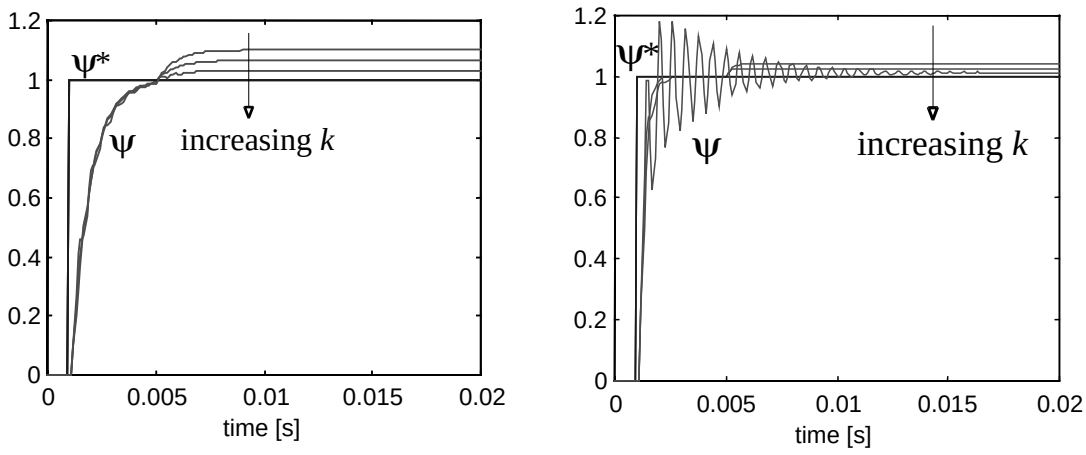

Figure 5-5 *Step response of flux control with flux controller gain k_1=0.1 (left figure) and k_1=0.25 (right figure). Step step responses are shown for the three different compensation feedback gains k=0, k=0.35 and k=0.7.*

Note that the error imposed by the dead time is reduced with increasing flux controller gain as well as with increased feedback compensation gain. The combination k_1=0.1 and k=0.7 as well as the combination k_1=0.25 and k=0.35 do both give a significant supression of the flux error, with maintained stability.

5.2 Position asymmetry compensation by feed back of the dc components in the phase currents

Compensation principle

Assume the upper position transistor in phase A is ”fast” and the upper position in phase B is ”slow”. Then the ”1”-pulses in phase A and the ”0”-pulses in phase B will have longer duration than expected, see figure 5-6. In figure 5-7 the dotted lines indicate the expected pulse duration and the solid line the actual duration. The compensation method is obvious, if the turn-on of the upper position switch can be delayed and if the turn-off in lower position switch in the same phase can be done earlier, and the opposite in phase B, the compensation is done. The problem is that it is not the actual commutation time that is measured, it is the DC component in the phase current. Thus it is not possible to judge if it is a fast component in upper position or a slow in lower position. The compensation will therefore be done in both positions.

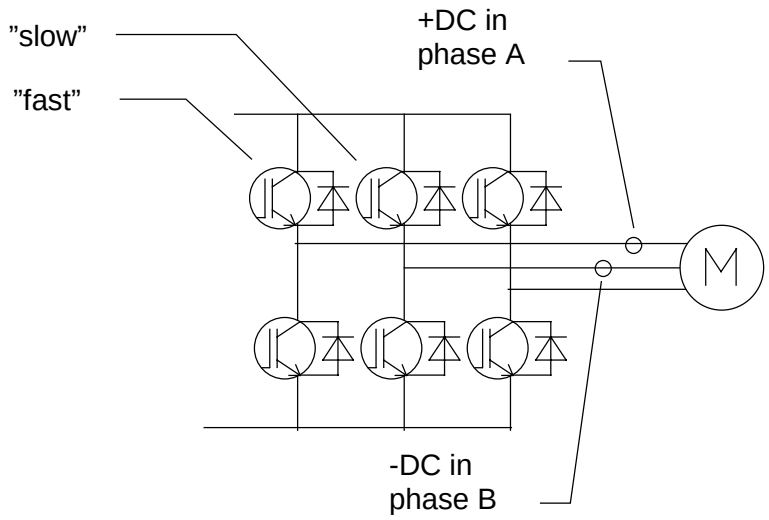

Figure 5-6 *The asymmetry in phase A and phase B.*

In phase A, positive dc component is found in the phase current and therefore the ”one”-pulses are made narrower. In phase B, a negative dc component is found in the phase current and therefore the one pulses are widened. In phase C no dc component is found in the phase current and the modulator pulses are left unaffected, see figure 5-7.

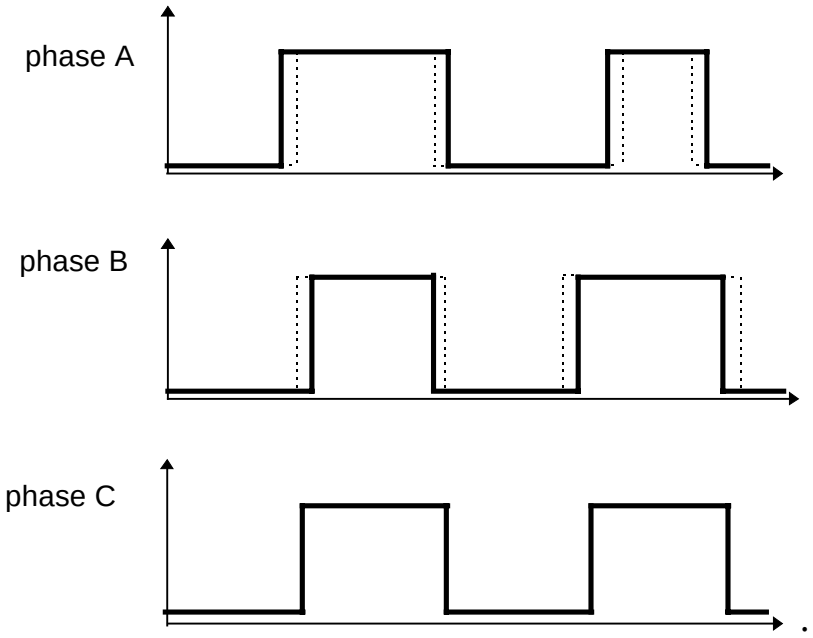

Figure 5-7. *The effect of the asymmetry is found in the pulse duration.*

The control system.

The compensation control system is depicted in figure 5-8. The dc current component reference is zero. The dc component in the phase current is found after low pass filtering of the phase current signal. The error signal is connected to the PI controller. The PI controller output is acting on the modulator. A positive dc current component in the phase current will make the modulator

”one”-pulses narrower. In the same way, a negative dc current will make them wider.

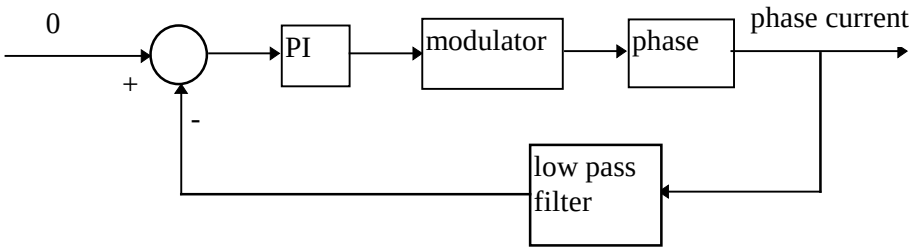

Figure 5-8. *The control system*

The test set up.

When the compensation method is tested the asymmetry is done by delaying the turn-on order to the upper position GTO-thyristor in phase A, see figure 5-9. In a standard production of GTO-thyristors the turn-on and turn-off properties are very stable, they do not vary considerably. The extremes are rare. In order to test the control system, an extra delay unit was connected between the gate drive unit and the GTO-thyristor, as shown in figure 5-9. At the test it was assumed that it is safer to delay the turn-on instead of delaying the turn-off, otherwise there is always a risk that both upper and lower position GTO-thyristor can be conducting simultaneously.

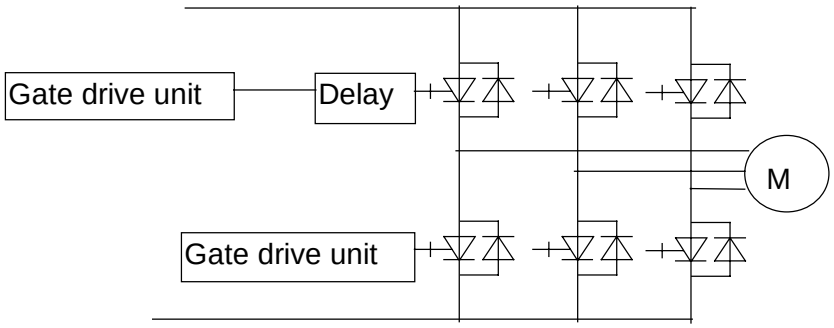

Figure 5-9 *The test set up*

The delay could be varied in four steps 2, 4, 8 or 16 μs. The longer the delay the easier it is to study the effects of position asymmetry, but what delay is acceptable for the control system? The first investigation was to check if the control system can accept even 16 μs. This was possible and therefore this delay was chosen for this investigation, but this delay is longer than what can be expected in reality.

Result

The expected DC-link fundamental current component versus commutation delay is a straight line passing the origin. The result shows an almost straight line but it does not pass the origin, and the reason is that position asymmetry already is present in the inverter before this extra asymmetry, see figure 5-10.

Data for the drive system is presented in appendix C2.

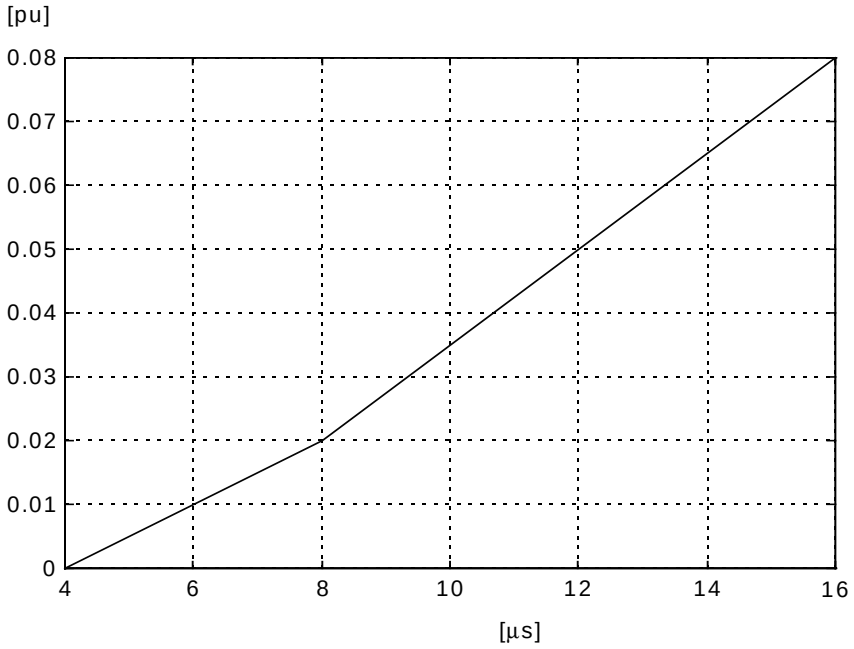

Figure 5-10. *Generation of a dc component in the phase current versus commutation delay.*

Driving mode. The motor torque is 50% of nominal torque

In the upper curve of figure 5-12, it can be found that the normal control system reduces the effect of position asymmetry up to about 50 Hz stator frequency, but at higher frequencies the control system is too slow. When the commutation frequency decreases (other modulations patterns are used) at higher stator frequency, see figure 5-11, the effect of position asymmetry decreases. In the lower curve in figure 5-12 it is found that the compensation is effective, but can not totally reduce the effect of position asymmetry. The reason is probably a remaining dc bias in the current transducer.

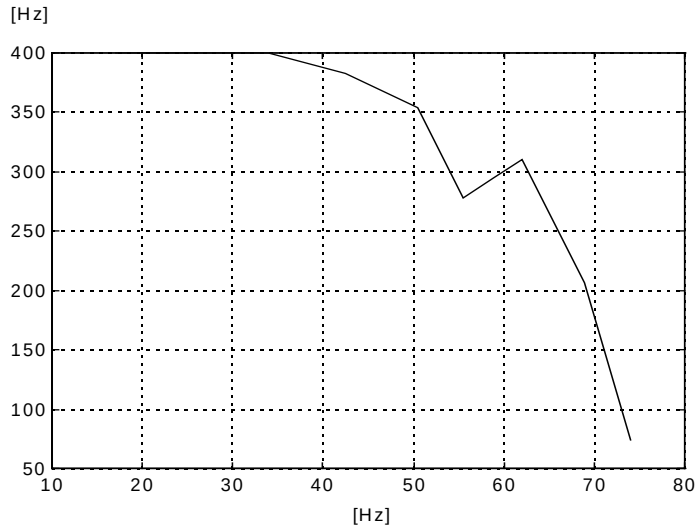

Figure 5-11. *Commutation frequency versus stator frequency*

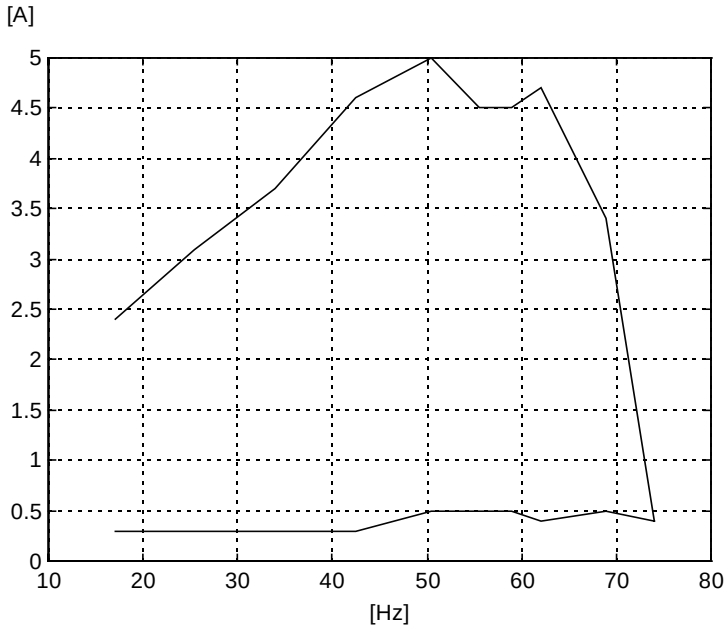

Figure 5-12. *Generation of a dc component in the phase current versus stator frequency. Upper curve without compensation, and lower curve with compensation.*

Driving mode. The motor torque is 100% of nominal torque at 17 Hz, but 80% at the other frequencies.

The reduction of the torque at higher frequency is caused by a limited feeding capability in the test set up. The same effect of position asymmetry as in driving mode with 50% torque can be seen here. In this test the result at 100 Hz in compensated mode is unexpectedly high. The reason is contribution from the second harmonic in the mains supply, see figure 5-13 and 5-14.

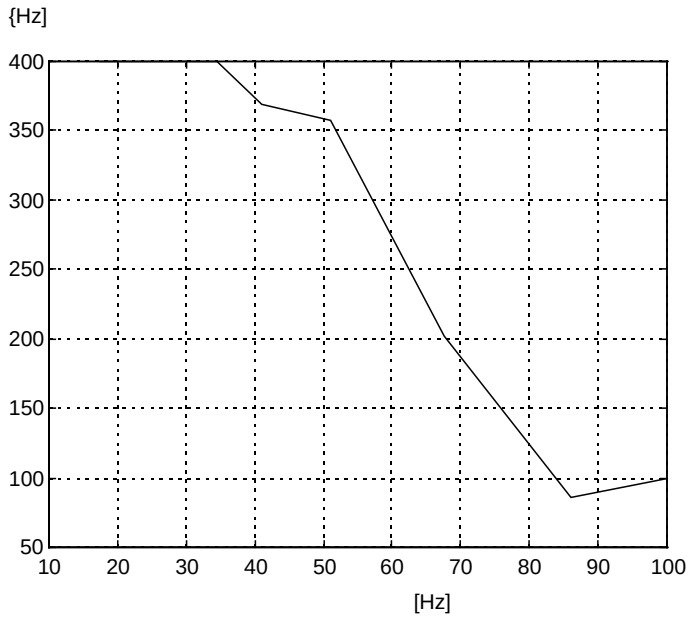

Figure 5-13. *Commutation frequency versus stator frequency*

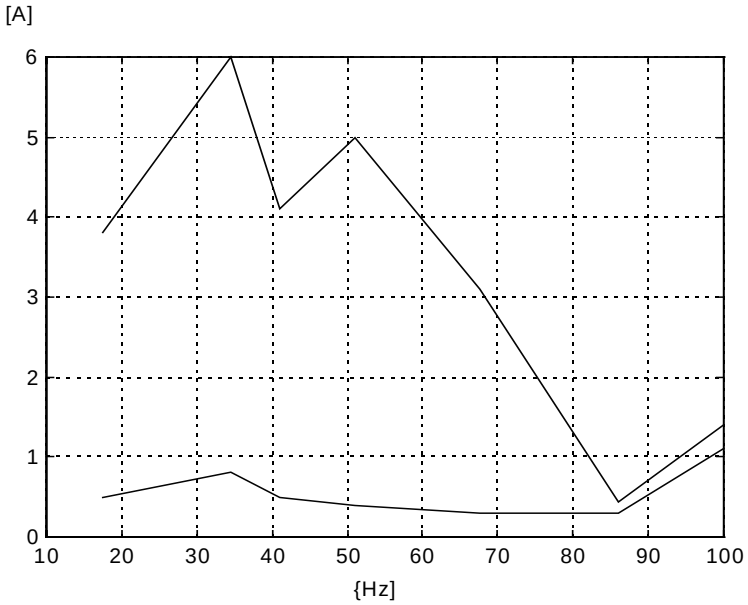

Figure 5-14. *Generation of a dc component in the phase current versus stator frequency. Upper curve without compensation, and lower curve with compensation.*

Braking mode. The motor torque is 40% of nominal torque.

In figure 5-15 and in figure 5-16 the effect of compensation in braking mode can be studied. The result is similar to the driving mode result.

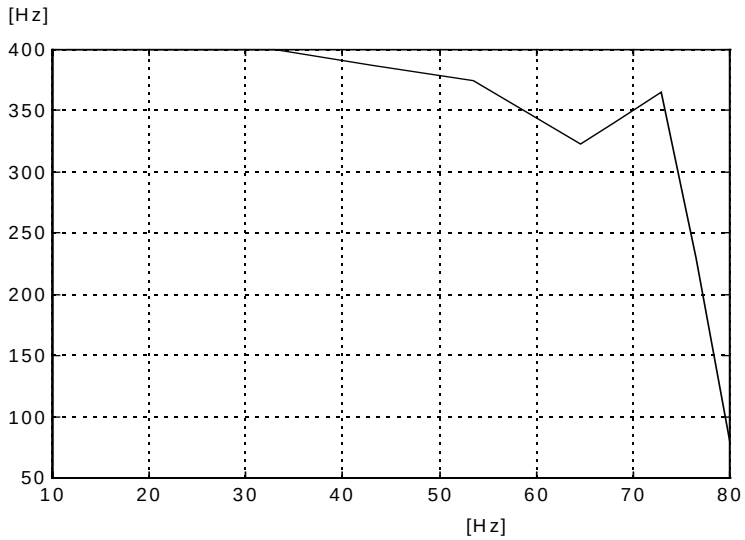

Figure 5-15. *Commutation frequency versus stator frequency*

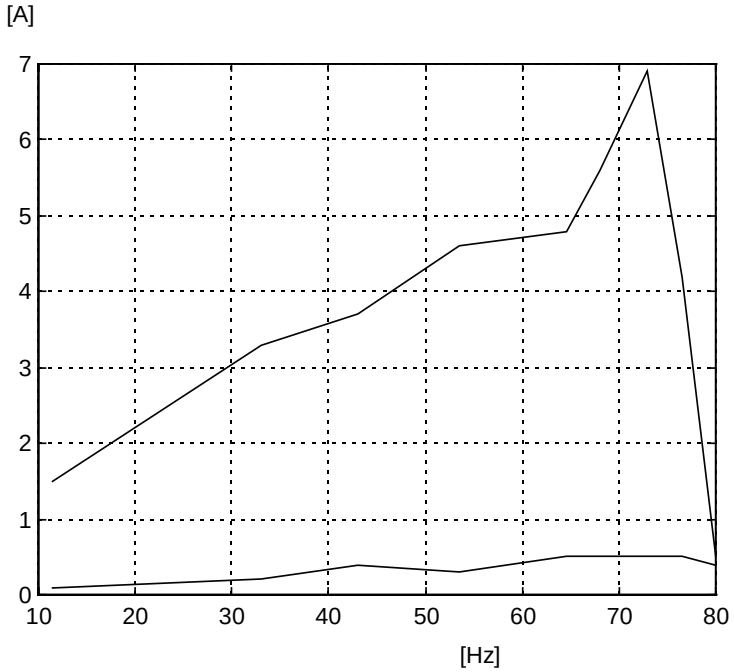

Figure 5-16. *Generation of a dc component in the phase current versus stator frequency. Upper curve without compensation, and lower curve with compensation. The same effect of position asymmetry as in driving mode can also be seen here.*

Discussion

It is obvious from these tests that the control system effectively can detect and compensate the position asymmetry. It is clearly shown in the diagrams that the higher the commutation frequency, the higher is the fundamental component in the DC-link current. At square wave modulation with low switching frequency, the DC current is low, even without the compensation. The control system demands high current transducer dynamics, it must be able to measure several hundreds of AC amps at the same time as it measures a few amps of DC in the phase current. The disadvantage with the method is that with asymmetry only in one phase, DC components will be found in all three phases. The control systems acts in all phases where a DC current is present, thus also in phases without asymmetry. The largest disadvantage with this method is that a remaining DC bias in a phase current transducer will totally ruin the compensation and can even make things worse.

5.3 DC biased current transducer compensation by feed back of fundamental frequency current component in the dc link

In the previous section the position asymmetry was studied where the asymmetry has been achieved by delaying the turn on of a GTO-thyristor. The

compensation method changed the modulation pattern until the asymmetry disappeared. This is a way to simulate asymmetry, caused by asymmetric commutation properties.

In this section, a position asymmetry caused by a DC bias in one phase current transducer is studied. In section 5.2, it was found that the control system at low stator frequencies is able to reduce the effect of asymmetry, compare figure 5-12, 5-14 and 5-16. When the control system measures a dc component in the phase current it tries to reduce it. If the case is a real asymmetry, it will be reduced. On the other hand, if the measured asymmetry only is a DC-biased current transducer, then the compensating action will cause a real DC-component, see figure 5-17.

The time domain DC-link current is formed by multiplying the time domain modulation pattern and the time domain phase current in each phase and then add the contribution from all three phases. If we simplify the situation and regard the three modulation patterns and the three phase currents as being fundamental components, i.e. pure sinusoidal currents, the DC-link current will only contain a DC-component. If one of the phase currents has a DC-component, it will be modulated to the DC-link by the modulation pattern of this phase.

As a DC-component has no phase-angle, the DC-link current will have the same frequency and the same phase-angle as the modulation pattern in the phase, where the current has a DC-component. If there is no DC-component in the measured current from the start, only a biased current-transducer, the ordinary current controller will compensate for this DC-component and then in fact produce a real DC-component, and the theory is still valid.

The thin circle in figure 5-17 is the desired motor current trajectory. Due to position asymmetry the current trajectory instead is the thick circle. To compensate the position asymmetry the compensation vector, length A and phase angel γ, has to be subtracted from the actual current, see figure 5-17A. However if there is no position asymmetry, just a DC bias in a current transducer, the control system will interpret the situation as an asymmetry and will try to compensate it by subtracting the compensation vector. Then the system in fact has created a position asymmetry, see the thick circle in figure 5-17B.

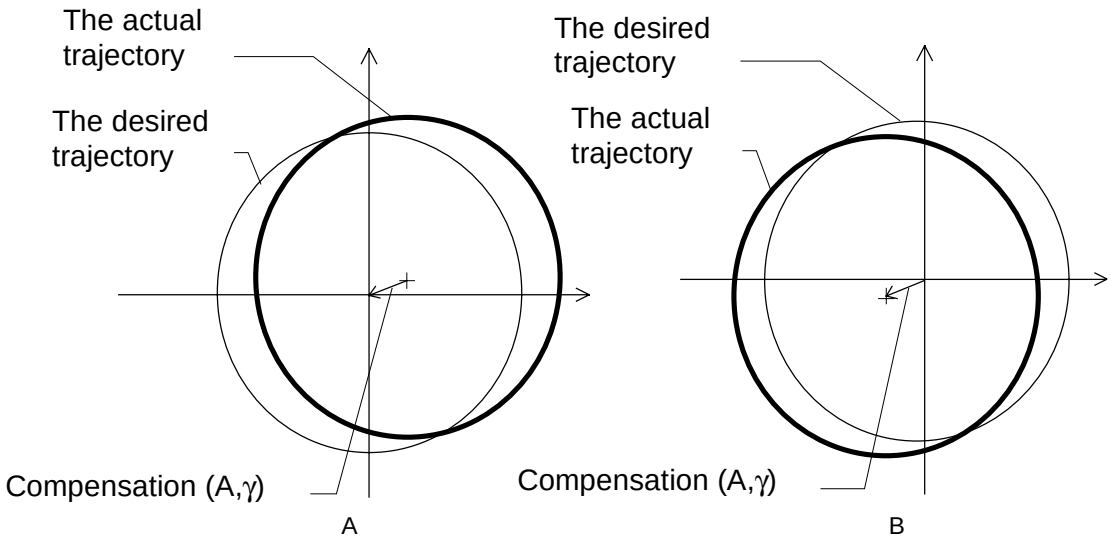

Figure 5-17. *A) a real position asymmetry current trajectory (thick circle), compared with the desired current trajectory (thin circle). B) a position asymmetry current trajectory, caused by a dc biased current transducer (thick circle), compared with a the desired current trajectory (thin circle).*

In the latter case the position asymmetry can be detected in the fundamental frequency current in the DC-link.

The control system.

Assume the offset errors of the phase current transducers expressed as a vector $\vec{i}_{offset}$. The control system in figure 3-8 will then produce the error signal $\vec{i}_{error}$, which forms a fundamental frequency current component in the DC-link current as $i_{dc,error}$, see figure 5-18. The signal $\vec{i}_{offset}$ will in figure 3-8 be found in the three-phase signal $\vec{i}_s$. The goal here is to estimate the magnitude and phase of the current measurement offset vector $\vec{i}_{offset}$. The approach is to use the information in the dc link current ripple in a PLL circuit that locks the estimate of the measurement offset vector $\vec{i}_{offset}$. The compensation principle is derived in the next paragraph.

$$\vec{i}_{error} = -\vec{i}_{offset} = -\hat{i}_{offset} \cdot e^{j(\gamma-\pi)}$$

$$P_{error} = \mathrm{Re}\left\{\vec{e} \cdot \vec{i}^{\,*}_{error}\right\} = \mathrm{Re}\left\{\hat{e} \cdot e^{j(\theta+\frac{\pi}{2})} \cdot \hat{i}_{offset} \cdot e^{j(\pi-\gamma)}\right\}$$

$$i_{dc,error} = \frac{P_{error}}{U_{dc}}$$

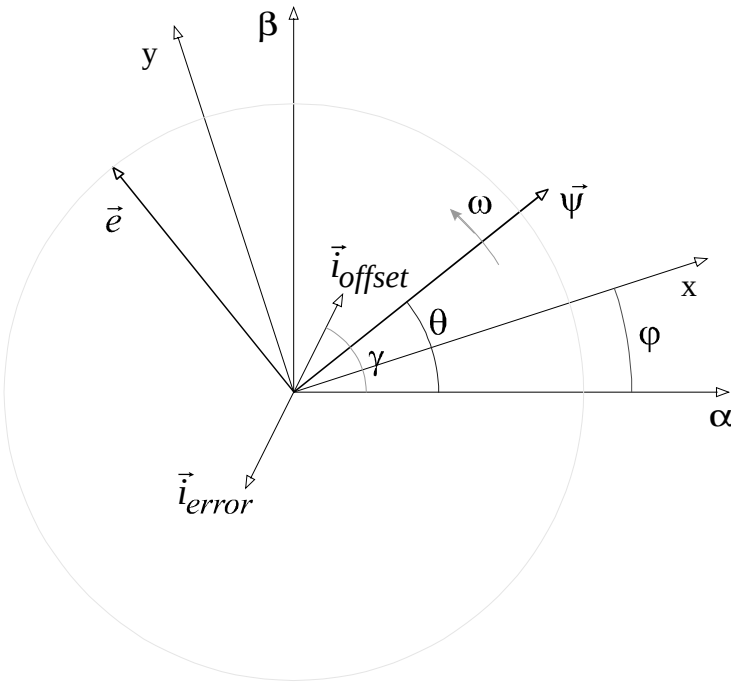

Figure 5-18 *The stator flux vector ($\vec{\psi}$), the induced emf ($\vec{e}$), the (α,β) reference frame and the reference frame (x,y) used in the serach for the offset vector $\vec{i}_{offset}$.*

Compensation principle

The task is to find the vector of length i_{offset} and angle γ, which then shall be subtracted from the measured value of the phase current, see figure 5-18. The compensation will in figure 3-8 be found in the three-phase signal i_s.

To find i_{offset} and γ, a "search"-signal *AP* is used in a PLL circuit. *AP* is the product of a band pass filtered (around the fundamental frequency) DC link current and the unity vector $\vec{s}^{xy} = 1 \cdot e^{j(\theta - \phi)}$. The components of *AP* are via two integrators driving the phase and the amplitude of the estimated vector $\vec{i}_{offset}$ until the band pass filtered dc link current signal is reduced to zero.

The two components of AP are derived according to the following expressions. Note that the help variables $\Delta\gamma$ and ξ are introduced.

The real component of *AP*, Re{*AP*}=

$$= s_x \cdot i_{dc,error} = \mathrm{Re}\left\{1 \cdot e^{j(\theta-\phi)}\right\} \cdot \frac{\mathrm{Re}\left\{\hat{e} \cdot e^{j(\theta+\frac{\pi}{2})} \cdot \hat{i}_{offset} \cdot e^{j(\pi-\gamma)}\right\}}{U_{dc}} =$$

$$= \cos(\theta-\phi) \cdot \hat{e} \cdot \cos\left(\theta + \frac{\pi}{2} + \pi - \gamma\right) \cdot \frac{\hat{i}_{offset}}{U_{dc}} = \cos(\theta-\phi) \cdot \cos\left(\theta - \gamma - \frac{\pi}{2}\right) \cdot \frac{\hat{e} \cdot \hat{i}_{offset}}{U_{dc}} =$$

$$= \{\theta = \omega \cdot t\} = i_{dc,error} \cdot \cos(\omega \cdot t - \phi) \cdot \cos\left(\omega \cdot t - \gamma - \frac{\pi}{2}\right) = \begin{Bmatrix} \phi = \gamma + \Delta\gamma \\ \omega \cdot t - \gamma = \xi \end{Bmatrix} =$$

$$= i_{dc,error} \cdot \cos(\xi - \Delta\gamma) \cdot \cos\left(\xi - \frac{\pi}{2}\right) = i_{dc,error} \cdot (\cos\xi \cdot \cos\Delta\gamma + \sin\xi \cdot \sin\Delta\gamma) \cdot \sin\xi =$$

$$= i_{dc,error} \cdot \left(\sin\xi \cdot \cos\xi \cdot \cos\Delta\gamma + \sin^2\xi \cdot \sin\Delta\gamma\right)$$

Note that the average of $\mathrm{Re}\{AP\} = \frac{i_{dc,error}}{2}$ when $\Delta\gamma=\pi/2$, see figure 5-18.

The imaginary component of *AP*, Im{*AP*}=

$$= s_x \cdot i_{dc,error} = \mathrm{Im}\left\{1 \cdot e^{j(\theta-\phi)}\right\} \cdot \frac{\mathrm{Re}\left\{\hat{e} \cdot e^{j(\theta+\frac{\pi}{2})} \cdot \hat{i}_{offset} \cdot e^{j(\pi-\gamma)}\right\}}{U_{dc}} =$$

$$= \sin(\theta-\phi) \cdot \hat{e} \cdot \cos\left(\theta + \frac{\pi}{2} + \pi - \gamma\right) \cdot \frac{\hat{i}_{offset}}{U_{dc}} = \sin(\theta-\phi) \cdot \cos\left(\theta - \gamma - \frac{\pi}{2}\right) \cdot \frac{\hat{e} \cdot \hat{i}_{offset}}{U_{dc}} =$$

$$= \{\theta = \omega \cdot t\} = i_{dc,error} \cdot \sin(\omega \cdot t - \phi) \cdot \cos\left(\omega \cdot t - \gamma - \frac{\pi}{2}\right) = \begin{Bmatrix} \phi = \gamma + \Delta\gamma \\ \omega \cdot t - \gamma = \xi \end{Bmatrix} =$$

$$= i_{dc,error} \cdot \sin(\xi - \Delta\gamma) \cdot \cos\left(\xi - \frac{\pi}{2}\right) = i_{dc,error} \cdot (\sin\xi \cdot \cos\Delta\gamma - \cos\xi \cdot \sin\Delta\gamma) \cdot \sin\xi =$$

$$= i_{dc,error} \cdot \left(\sin^2\xi \cdot \cos\Delta\gamma - \cos\xi \cdot \sin\xi \cdot \sin\Delta\gamma\right)$$

Note that the average of Im{*AP*}= 0 when $\Delta\gamma=\pi/2$, see figure 5-18.

The imaginary component of AP, Im{*AP*}, can thus be used to locate the angle of the offset current vector in a PLL circuit. Similarly, once the phase of the offset current vector is known, the real component of AP, Im{*AP*}, can be used

to identify the amplitude of the offset current vector and then compensate it in the stator current measurement.

The structure of the control system is described in figure 5-19.

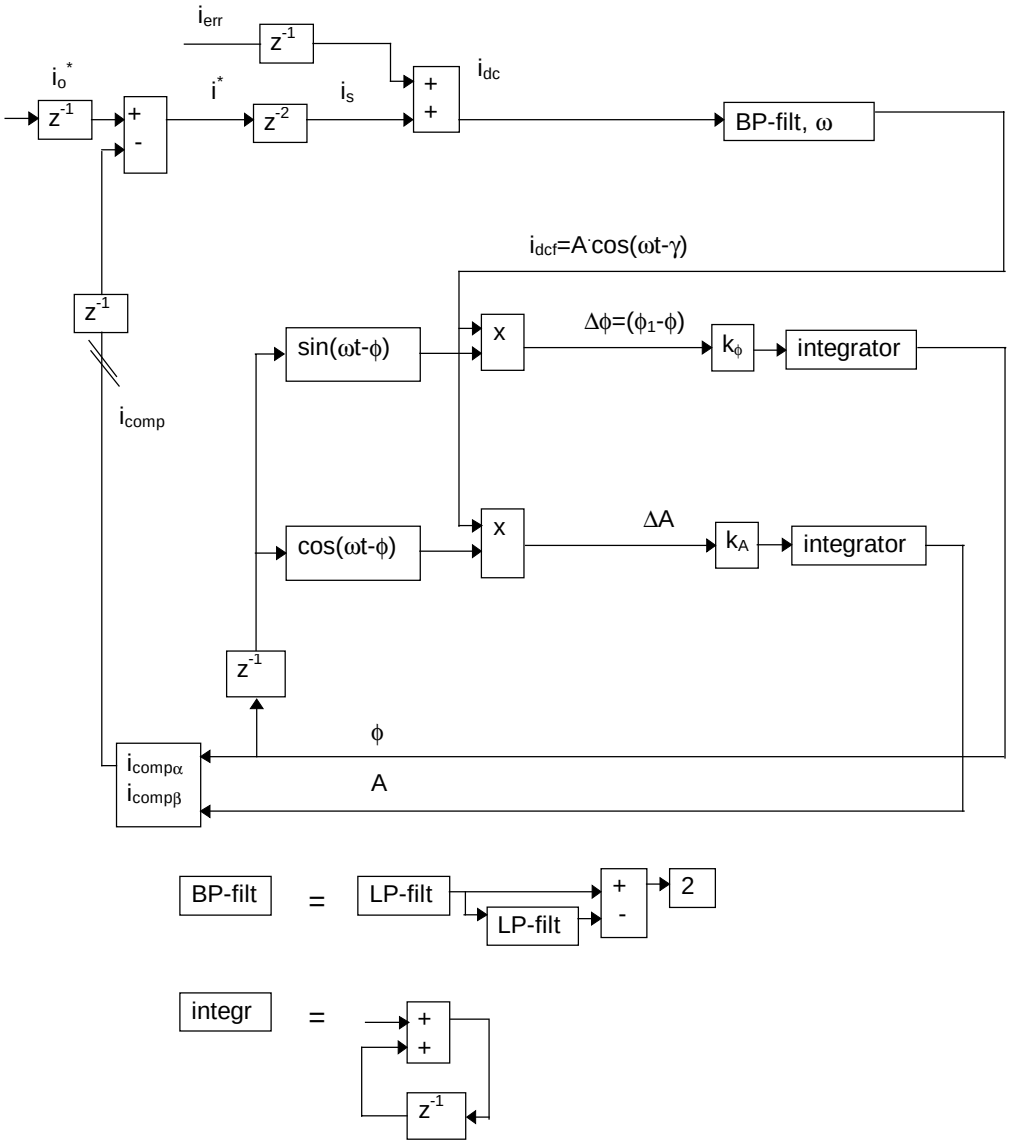

Figure 5-19 *The control system. i_o* is a generalised stator current reference, i* an intermediate variable and i_s the stator current that is reflected into the dc link current i_{dc}.*

Stability analysis

In order to analyse the stability of the proposed method for compensation of current sensor offset, a simplified model of the control system is made, see figure 5-19. The transformation between different frames is not included as this process does not contribute to the dynamics of the system. The system is also scalar and represent only the active power flow in the drive system. The delay

of a ”fast” or ”slow” computer is included, as well as an external error source to account for the voltage time area error due to dead time effects.

$$\begin{cases} i^* = z^{-1} \cdot \left(i_0^* - i_{comp} \right) \\ i_s = z^{-2} \cdot i^* \\ i_{dc} = z^{-1} \cdot i_{err} + i_s \\ i_{comp} = i_{dc} \cdot H(z) \\ H(z) = (BP - filt) \cdot z^{-1} \cdot (PI + PI) \end{cases}$$

$$\begin{cases} i^* = \dfrac{z^{-1}}{1 + z^{-3} \cdot H(z)} \cdot i_0^* - \dfrac{z^{-2} \cdot H(z)}{1 + z^{-3} \cdot H(z)} \cdot i_{err} \\ H(z) = (BP - filt) \cdot z^{-1} \cdot (PI + PI) \end{cases}$$

where *(BP-filt)* is a bandpass filter with the centre frequency ω

$$\frac{2 \cdot z \cdot \omega t_0 \cdot (1 - \omega t_0)(z - 1)}{(z - (1 - \omega t_0))^2}$$

and *PI* is an integrator with the gain $t_0 k_n$.

$$\frac{z \cdot t_0 k_n}{(z - 1)}$$

$$H(z) = \frac{2 \cdot z \cdot \omega t_0 \cdot (1 - \omega t_0) \cdot (z - 1)}{(z - (1 - \omega t_0))^2} \cdot z^{-1} \cdot \frac{z \cdot t_0 \cdot (k_\phi + k_A)}{(z - 1)} =$$

$$= \frac{2 \cdot z \cdot (k_\phi + k_A) \cdot t_0 \cdot \omega t_0 (1 - \omega t_0)}{(z - (1 - \omega t_0))^2}$$

To investigate how the current reference is affected by the error i_{error}, i_0^* in the transfer function is set to zero:

$$\frac{i^*}{i_{err}} = -\frac{z^{-2} \cdot H(z)}{1 + z^{-3} \cdot H(z)}$$

The characteristic equation is:

$$1 + z^{-3} \cdot H(z) = \frac{2 \cdot z \cdot (k_\phi + k_A) \cdot t_0 \cdot \omega t_0 (1 - \omega t_0)}{(z - (1 - \omega t_0))^2} \cdot z^{-3} + 1 = 0$$

$$z^4 - 2z^3 \cdot (1 - \omega t_0) + z^2 \cdot (1 - \omega t_0)^2 + 2 \cdot (k_\phi + k_A) \cdot t_0 \cdot \omega t_0 (1 - \omega t_0) = 0$$

If the roots of the characteristic equation, the poles of the transfer function, are located inside the unit circle the system is stable ([22] page 320). In the following investigations the gain stable gain $(k_{\phi}+k_A)$ is analysed at two frequencies, 6 and 40 Hz. At both 6 Hz and at 40 Hz stator frequency the system is stable for $0<(k_{\phi}+k_A)<2000$, see figure 5-20 and 5-21. The sampling time $t_0=0.1$ *ms*.

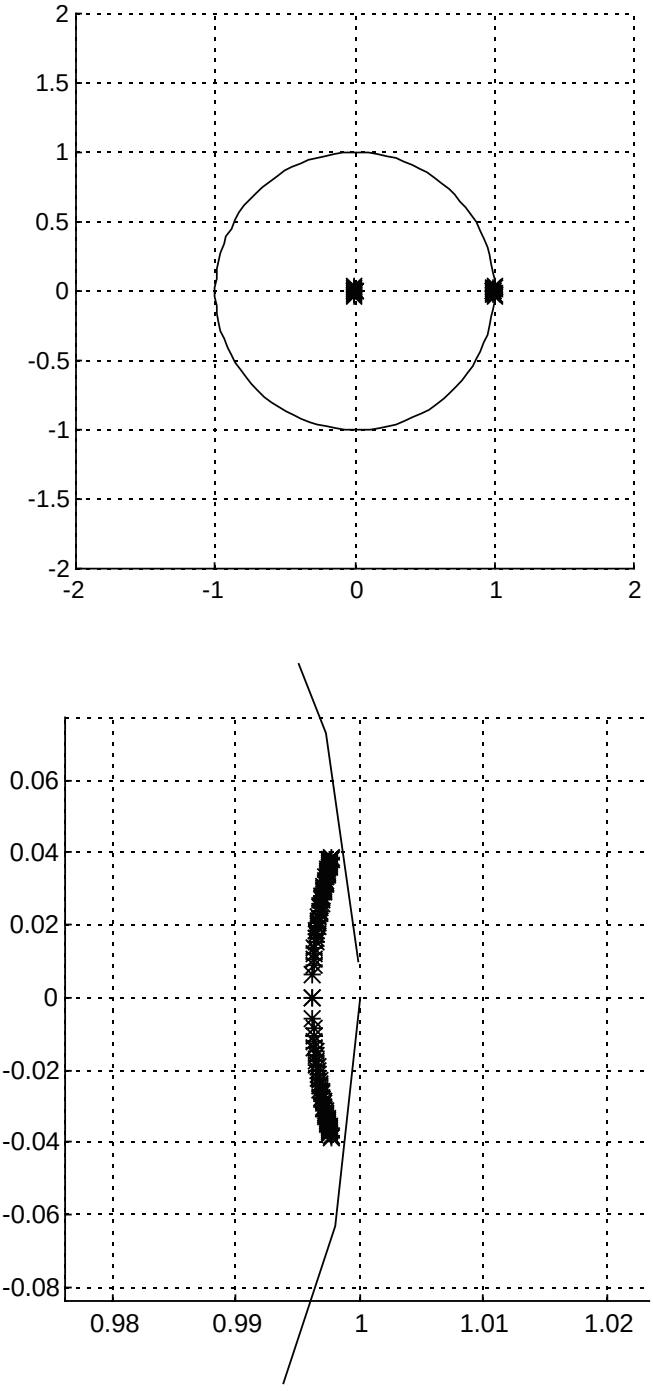

Figure 5-20 *fs=6, $0<(k_{\phi}+k_A)<2000$. All roots of the characteristic equation are located inside the unit circle (upper diagram). The region around (1,0) enlarged (lower diagram).*

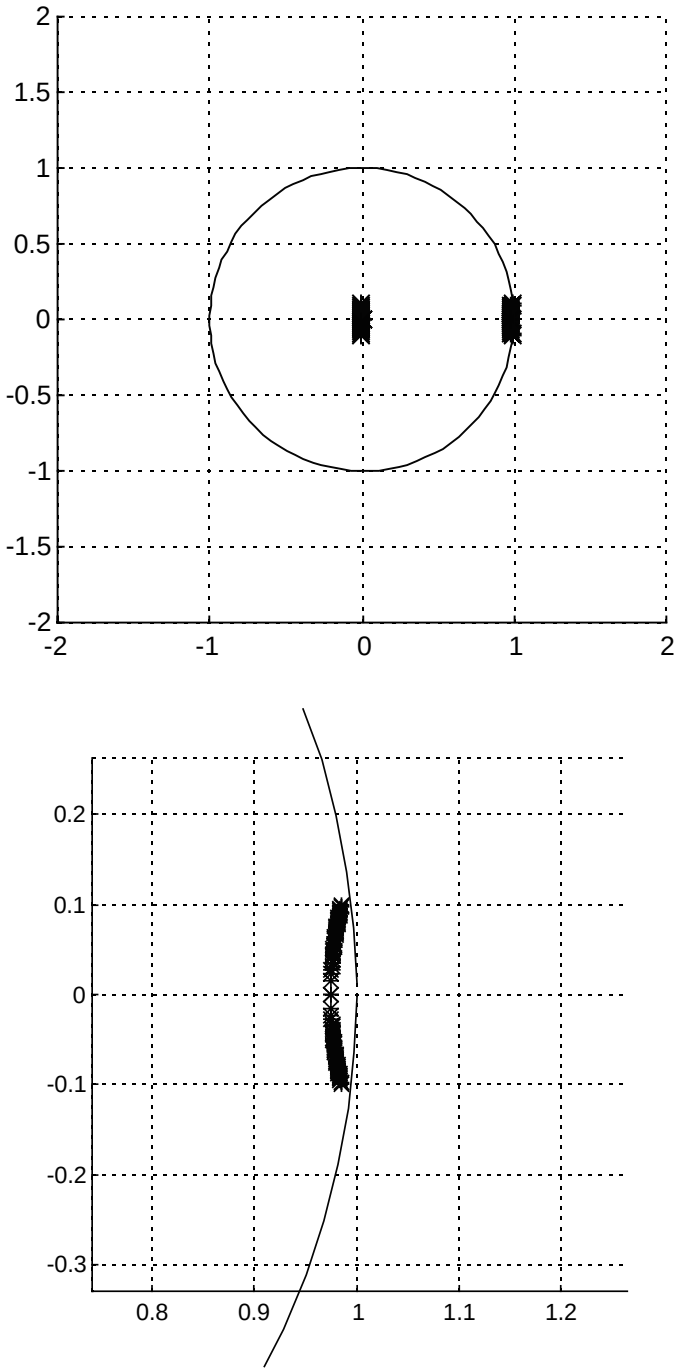

Figure 5-21 *fs=40 Hz, 0<(k_ϕ+k_A)<2000. All roots of the characteristic equation are located inside the unit circle (upper diagram). The region around (1,0) enlarged (lower diagram).*

Simulation

The system described in appendix C is simulated with the compensation method for current sensor offset included. The structure of the control system is according to figure 3-8 with the difference that the current sensor signal is subtracted with the estimated offset signal according to figure 5-19. Stationary

operation at two different frequencies are simulated, one at 6 Hz fundamental stator frequency and one at 40 Hz, with the gain $k_\phi=500$ and the gain $k_A=200$ referring to figure 5-19.

The 6 Hz simulation.

After the first 0.2 s the initial transient has vanished. At 0.4 s a transducer bias is added to the phase current signal in phase R. The bias is compensated after 0.2-0.3 s. We can see that the compensation phase angle equals $\pi/2$, which is the correct value for phase R, see figure 5-19 and figure 5-22a, b, c.

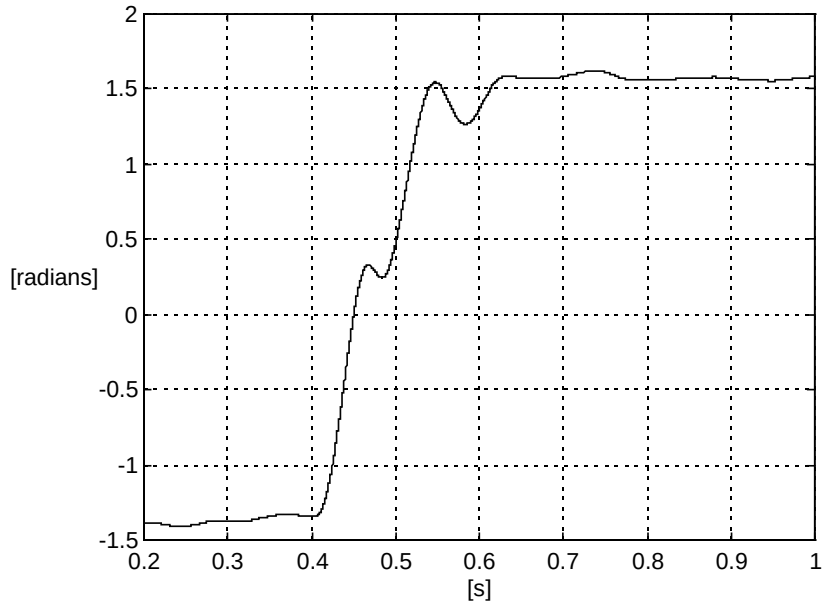

Figure 5-22a *The compensation phase angle ϕ*

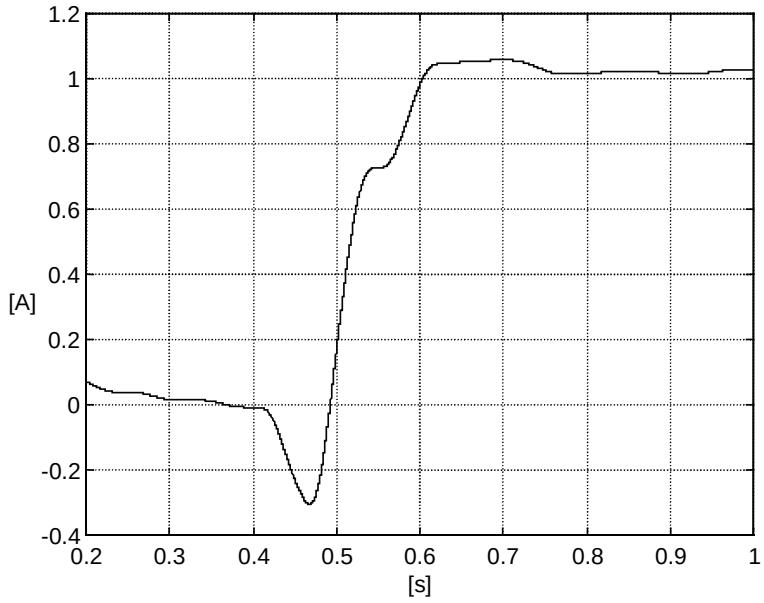

Figure 5-22b *The compensation amplitude*

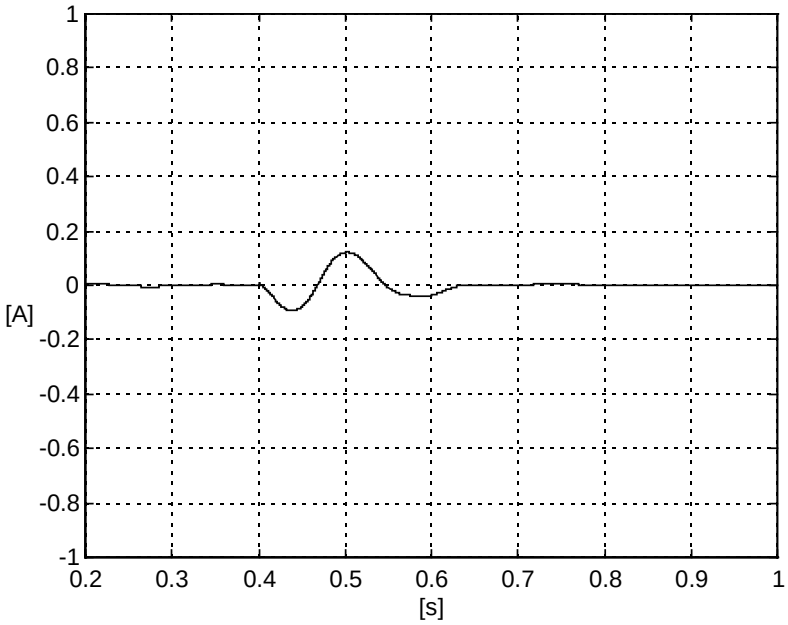

Figure 5-22c *The compensated and bandpassfiltered DC-link current.*

40 Hz stator frequency.

After the first 60 ms the initial transient has vanished. At 0.2 s a transducer bias is added to the phase current signal in phase R. The bias is compensated after 25 ms, We can see that the phase angle equals $\pi/2$, which is correct for phase R, see figure 5-19 and figure 5-23a, b, c.

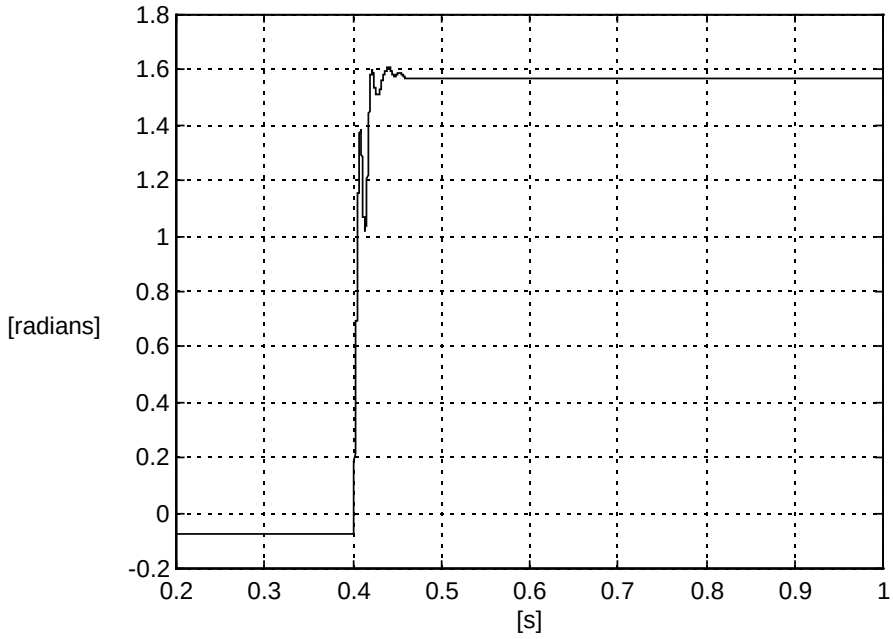

Figure 5-23a *The compensation phase angle ϕ.*

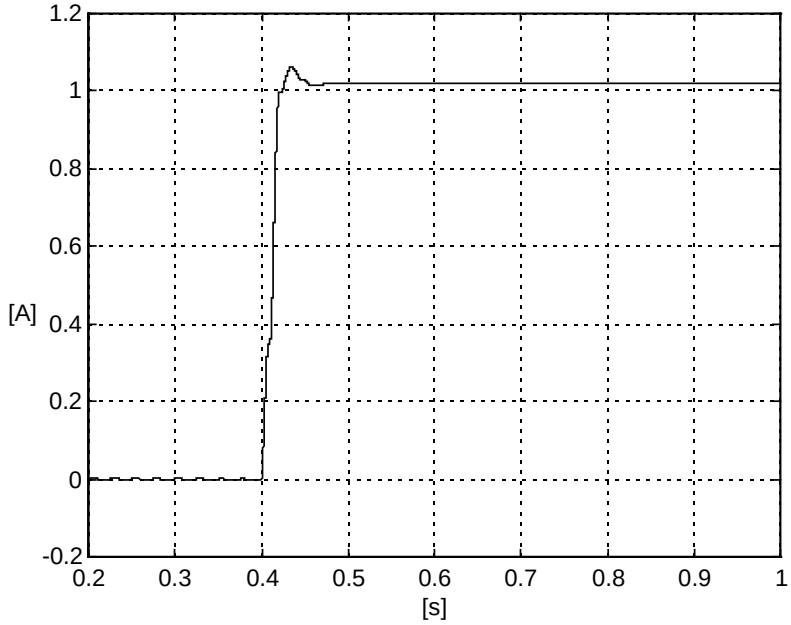

Figure 5-23b *The compensation amplitude*

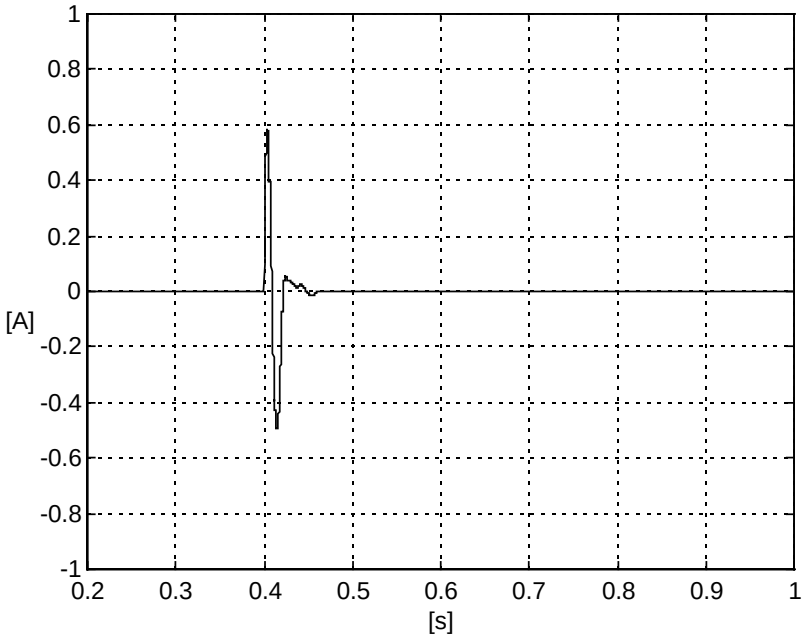

Figure 5-23c *The compensated and bandpass filtered DC-link current.*

5.4 Experimental results

A small industrial motor, rated 2.2 kW with data according to appendix C-1, was run from a transistor-based three phase machine converter. The current through the DC-link capacitor is measured with current transducers, both a Hall effect transducer and a Rogowski coil transducer are used. The remaining dc bias in a Hall effect transducer is not a problem in this case as we are measuring the ac components. The phase currents were measured with Hall effect

transducers, and the dc bias in one of the transducers is simulated by adding, in the software, a constant value to the measured value.

The experiment is a combined test where both the feed back part of the dead time compensation and the dc biased transducer compensation are tested. The results are found in four part diagrams, see figure 5-24 to 5-27, where the frequency domain DC-link current I_{dc} is presented.

- In the upper left diagram, the results without compensation is presented.
- In the lower left diagram, the result of the dead time compensation is presented.
- In the upper right diagram, the result of the dc biased transducer compensation is presented.
- In the lower right diagram the combined effect is found.

The tests in the real test run show that both systems are stable. The test where the dead time compensation is included reduces the sixth harmonic better than the ordinary flux control, see figure 5-24 to 5-27.

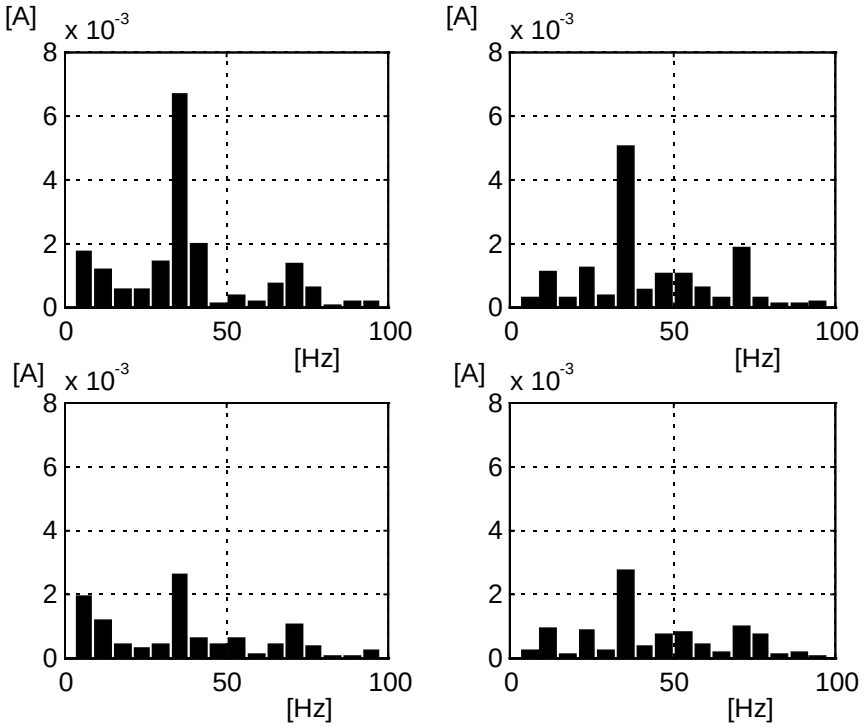

Figure 5-24. *No load, fs=6 Hz.*
Upper left no compensation
Upper right transducer offset compensation
Lower left dead time compensation
Lower right both dead time and transducer offset compensation

Comments to figure 5-24

Dead time compensation: About one third of the sixth harmonics remains. The fifth and the seventh harmonics are also reduced.

DC-biased current transducer compensation: The fundamental frequency current component is reduced by 80%. Also the fifth and the seventh harmonic are reduced, but the fourth is increased.

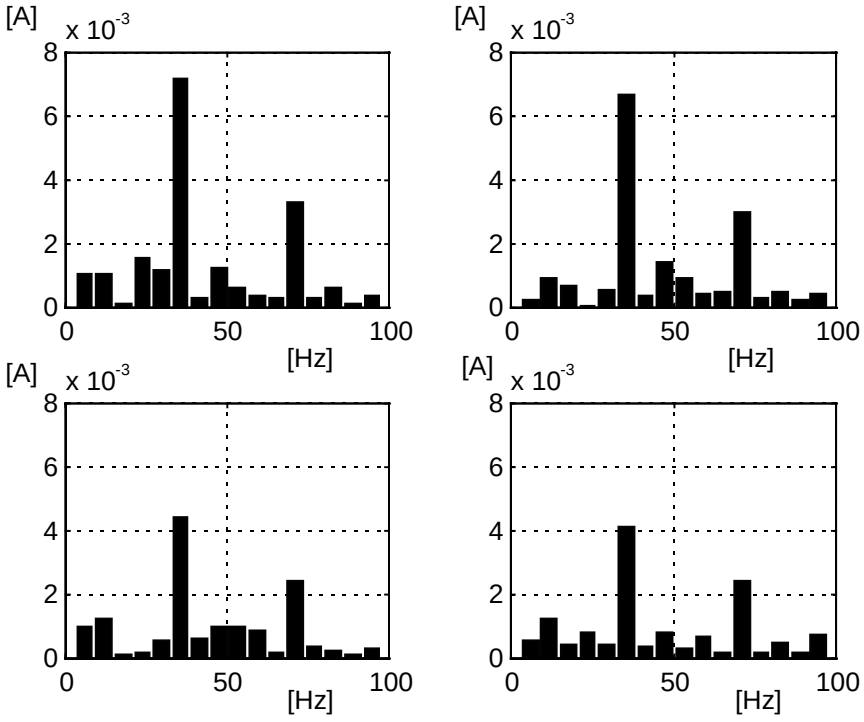

Figure 5-25. *High load, fs=6 Hz.*
Upper left no compensation
Upper right transducer offset compensation
Lower left dead time compensation
Lower right both dead time and transducer offset compensation

Comments to figure 5-25

Dead time compensation: The sixth harmonic is reduced by 40%. The fourth harmonic is also reduced.

Current transducer bias compensation: The fundamental frequency current component is reduced by two third. Also the fourth and the fifth harmonics are reduced, but the third one is slightly increased.

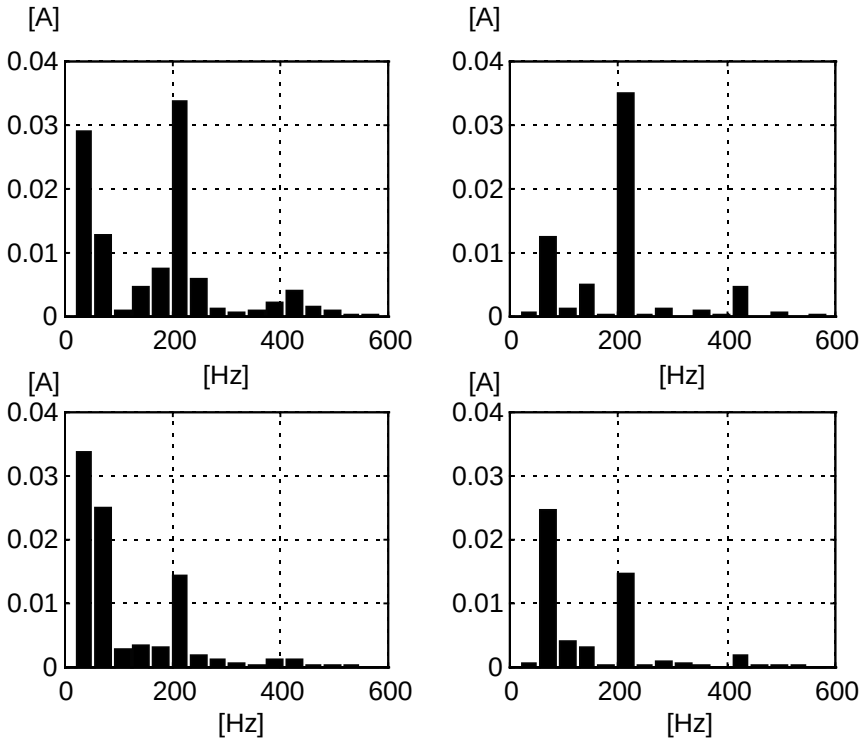

Figure 5-26. *No load, fs=40 Hz.*
Upper left no compensation
Upper right transducer offset compensation
Lower left dead time compensation
Lower right both dead time and transducer offset compensation

Comments to figure 5-26

Dead time compensation: Slightly more than one third of the sixth harmonic remains. However, the second harmonic amplitude is increased twice.

Current transducer bias compensation: The remaining part of the fundamental frequency current component is only some percent. The fifth harmonic is also reduced.

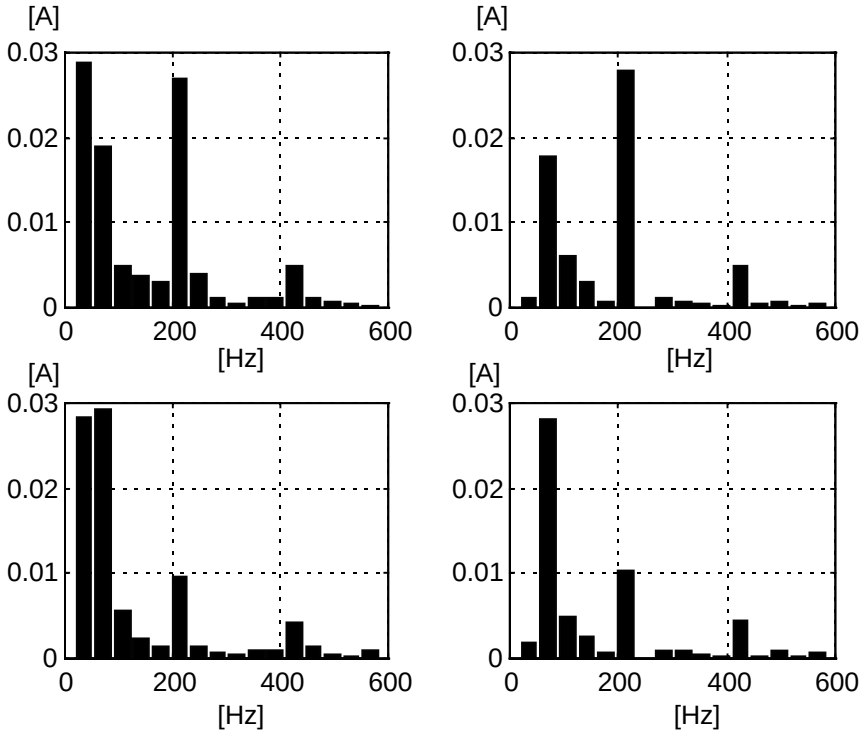

Figure 5-27. *High load, fs=40 Hz.*
Upper left no compensation
Upper right transducer offset compensation
Lower left dead time compensation
Lower right both dead time and transducer offset compensation

Comments to figure 5-27

Dead time compensation: slightly more than one third of the sixth harmonic remains. However, the second harmonic amplitude is increased with about 50%.

Current transducer bias compensation: The remaining part of the fundamental frequency current component is only some percent. The fifth and the seventh harmonics are also reduced.

Conclusion

- The effect of the feed back part of the dead time compensation is rather constant, independent of the fundamental frequency.
- The effect of compensation of the biased transducer is more effective at higher fundamental frequencies.
- At low fundamental frequencies the normal control system compensates effectively. Additional compensation methods are therefore only necessary at higher frequencies.

6 Conclusions and Future Work.

During the design stage of a traction drive system, especially at the design of line filters, it is necessary to be able to predict the line interference. One traditional way for such investigation is to use simulation programs, which are accurate but have the disadvantage of being slow. In this thesis, fast algorithms for calculation of the magnitude and frequency of the line harmonics, caused by both ideal and non-ideal commutations, have been presented. This method presumes steady state conditions and shall be used for receiving a rapid overview of the generation of line harmonics at a large number of operating points. The model predicts the current harmonic content in the phase currents and in the DC-link current, both in a machine converter and in a line converter.

Furthermore, it has been presented in this thesis how some of these non ideal commutation effects can be compensated. Following compensation methods is investigated and presented:

- Dead time compensation. The compensation method is a combination of a feed forward of the predicted deficiency of voltage time area based on transistor or diode commutation, and a feed back of the differential between the integral of the inverter output voltage, or rather the output flux, and the voltage time area reference.

- Position asymmetry compensation. The compensation method is based on feed back of the dc component in the inverter phase currents.

- Compensation of a remaining dc bias in Hall-effect current transducers (Adtranz Sweden ha s a patent pending for this compensation method). In the method, the fundamental current content in the DC-link current is fed back to the control system.

The compensation methods are found very effective for most operating conditions. With the use of the presented compensation methods, line filters and other components for reduction of line interference can be made much smaller, both concerning weight and volume.

6.1 Future work

One basic result of this study is that it is better to measure the information of non-ideal commutations in an AC signal rather than in a DC signal. Otherwise the remaining DC bias in a transducer can destroy the information.

Most asymmetries will generate characteristic harmonic current components in the DC-link, where they can be used as AC signals for compensation purpose. The disadvantage with this method is that it demands extra current transducers. A future work is to study if the AC current component can be found in the measured DC-link voltage ripple. If this is possible, the voltage transducer, which anyway is used to measure the DC-component of the DC-link voltage, can be used.

As we have found in Chapter 4 the different kinds of asymmetries will generate typical current harmonics in the DC-link. Another suggestion for future work is to check if other asymmetries can be compensated.

7 References

1) O.S. Nock, ”Railway Signalling”. A & C Black, 1995. London, UK.

2) Colin Bailey, ”European Railway Signalling”. A & C Black, 1995. London UK.

3) Maurice Leach, ”Railway Control System”. A & C Black, 1991. London UK.

4) R.J. Hill, ”Tutorial. Electric railway traction. Part 1.Electric traction and DC traction motor drives” Power Engineering Journal vol 8, no. 1, February 1994, page 47-56. UK.

5) R.J. Hill, ”Tutorial. Electric railway traction. Part 2 Traction drives with three-phase induction motors” Power Engineering Journal vol 8, no. 3, June 1994, page 143-152. UK.

6) R.J. Hill, ”Tutorial. Electric railway traction. Part 3. Traction power supplies”. Power Engineering Journal vol 8, no. 6, December 1994, page 275-286. UK.

7) ”Track circuit manual. A.C. Track Circuits - Planning and design principles”. Signal & Telecommunications Engineering Department, British Railways. No. TM51, issue 02, June 1991. London UK

8) ”Code of practice DC Track Circuits”. Railtrack, Safety & Standard Directorate. GK/RC 0755 Issue One August 1994. London UK.

9) ”Code of practice TI.21 Audio Frequency Track Circuits”. Railtrack, Safety & Standard Directorate. GK/RC 0761. June 1996. London UK

10) ”Code of practice HVI Track Circuits”. Railtrack, Safety & Standard Directorate. GK/RC 0756 Issue One August 1994. London UK.

11) ”Nordisk Familjebok”, volume 6, third edition, headword ”Elektriska järnvägar”. Aktiebolagets familjebokens förlag, 1927. Stockholm Sweden

12) Egid Schneider, ” Traction current return system and earthing in railway installations. I. Principles.” Elektrische Bahnen vol. 96 no. 4, page 85-90, April 1998, Germany

13) Peter Deutschmann, Egid Schneider, Markus Zachmeier, ” Traction current return system and earthing in railway installations. II. AC railway.” Elektrische Bahnen vol. 96 page 91-98, April 1998, Germany

14) Egid Schneider, Markus Zachmeier, ”Traction current return system and earthing in railway installations. III. DC railway.” Elektrische Bahnen vol. 96 no. 4, page 99-106, April 1998, Germany.

15) Svenska elverksföreningen, ”Störningsbok, Starkströmsanläggningar störande inverkan på andra anläggningar” Norstedts äTryckeri, 1981. Stockholm Sweden

16) Anders Svärdström, ”Tillämpad signalanalys”. Studentlitteratur,1996, Lund Sweden

17) Emil Alm, W.Borgquist, J Körner, H. Pleijel ”Elektroteknik, Band III. Elektromaskinlära del 2a:Transformatorns driftegenskaper och beräkning”. Albert Bonniers Boktryckeri, 1927. Stockholm Sweden.

18) Gustaf Olsson, Mats Alakula, Tore Svensson, Bo Petersson, Olof Samuelsson, Jari Valis”Elmasksinsystem”, Department of Industrial Electrical Engineering and Automation, Lund Institute of Technology, 1994. Lund Sweden.

19) Mats Alakula, Gustaf Olsson, Tore Svensson, ”Styrning av elektriska drivsystem”, Department of Industrial Electrical Engineering and Automation, Lund Institute of Technology, 1992. Lund Sweden.

20) Stefan Östlund m.fl. ”Elektrisk traktionsteknik”, Institutionen för Elkraftteknik, Royal Institute of Technology, 1996. Stockholm Sweden.

21) Bo Peterson, ”Induction Machine Speed Estimation Obervations on Observers”, Department of Industrial Electrical Engineering and Automation, Lund Institute of Technology 1996. Lund Sweden.

22) Bengt Schmidtbauer,”Reglerteknik”, Chalmers Tekniska Högskola, Institutionen för reglerteknik, 1987. Gothenburg Sweden.

23) Group standard GS/ES1914, British Rail Board. ”Electromagnetic Susceptibility Data for Track Circuits and AWS”. Issue 1, Revision A, Feb 94. London UK.

24) Lars Gertmar ”Beräkning av spårreläströmmar i SJ.s signalsystem orsakade av feltillstånd med osymmetriskt styrda bryggor i tyristorlok”. School of

electrical engineering, Chalmers University of Technology. 1976, Göteborg, Sweden.

25) Lars Gertmar ”Utredning beträffande förutsättningar för signalstörningar på SJ signalanläggningar, i första hand härrörande från tyristorlok”. Department of electrical machinery, Chalmers University of Technology. 1980, Göteborg, Sweden.

26) T. M. Undeland, F. Jenset, A. Steinbakk, T. Rogne and M. Hernes; ”A snubber configuration for Both Power Transistors and GTO PWM Converters,” Proc. of 1984 Power Electronics Specialists Conference, pp. 42-53.

A Appendix A. Commutation Delay Algorithm

A.1 Upper GTO-thyristor commutation.

The phase current is positive, i.e. its direction is out from the phase, see figure A-1. The current commutates from upper GTO-thyristor T_u to lower anti parallel diode, D_l.

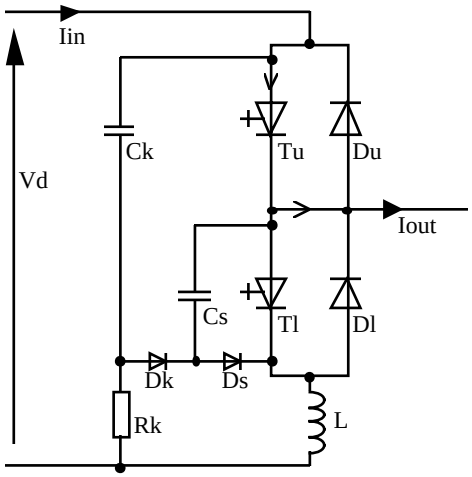

Figure A-1 *Turn off of upper thyristor*

The turn off of T_u. First the storage time is elapsing. The storage time is a linear function of the commutated current. During this time the output voltage equals the dc link high voltage. When the storage time has elapsed, the current through the GTO-thyristor decreases, and, simultaneously, the voltage drop over it starts to increase from zero to full DC-link voltage. The time for this process is the fall time t_f. The average time for full current turn off is half the fall time. The delay time for this part of the turn off is

$$t_1 = k_{st} \cdot I_{out} + l_{st} + \frac{t_f}{2}$$

where $k_{st}I_{out}+l_{st}$ is the storage time, assumed to be a linear function of the commutated current.

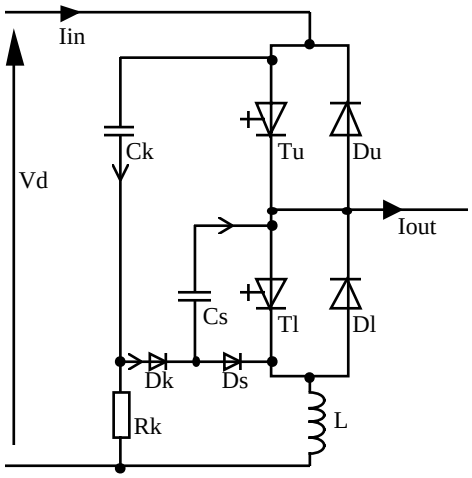

Figure A-2 *The current commutates to the snubber and clamping capacitor.*

When the current through the GTO-thyristor is turned off, it commutates over to the clamping capacitor C_k and the snubber capacitor C_S via the clamping diode D_k . At the beginning these capacitors are charged to V_d. The current discharges the snubber capacitor C_S, but continues to charge the clamping capacitor C_k. When C_S is completely discharged the current commutates over to the antiparallel diode D_l via the snubber diode D_S.

The delay time for discharging of C_S:

$$t_s = V_d \cdot \frac{C_s}{I_{out}}$$

The extra charging of the clamping capacitor leads to a negative output phase voltage U_k. At the calculation of the delay time t_k use the fact that the same current discharges Cs that charges C_k, i.e. the charges are the same:

$$U_k \cdot C_k = t \cdot I_{out} \text{ and } V_d \cdot C_s = t \cdot I_{out}$$

which gives:

$$U_k = V_d \frac{C_s}{C_k}$$

The voltage at the discharge of the snubber capacitor contributes to the voltage time area, i.e. to the delay. The negative voltage U_k at the continuous charge of the clamping capacitor decreases the voltage time area (and increases the delay).

The voltage time area of this part:

$$V_d t_2 = \frac{V_d}{2} t_s - \frac{U_k}{2} t_s = \frac{V_d}{2} \frac{C_s V_d}{I_{out}} - \frac{U_k}{2} \frac{C_s V_d}{I_{out}} =$$

$$= \frac{V_d}{2} \frac{C_s V_d}{I_{out}} - \frac{V_d}{2} \frac{C_s}{C_k} \frac{C_s V v_d}{I_{out}} = \frac{V_d}{2} \frac{C_s V_d}{I_{out}} (1 - \frac{C_s}{C_k})$$

And the time delay:

$$t_2 = \frac{C_s V_d}{2 I_{out}} (1 - \frac{C_s}{C_k})$$

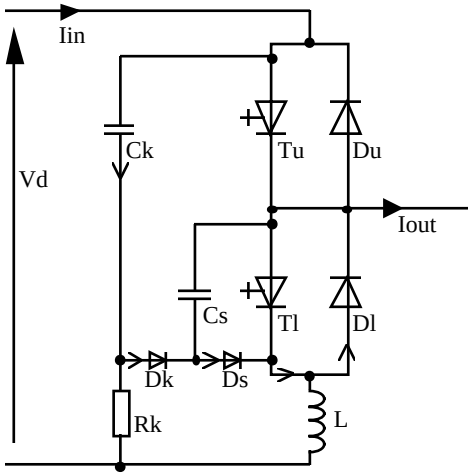

Figure A-3 *The current commutates to the lower anti parallel diode.*

Since the voltage drop over the clamping capacitor is greater than the DC-link voltage V_d, the di/dt-inductor L has a negative voltage drop and the current now commutates over to the inductor. At the negative voltage U_k the current commutates from clamping capacitor to the di/dt-inductor. At this time the voltage time area is further decreased:

$$\frac{U_k L I_{out}}{U_k} = L I_{out}$$

The time gain for this commutation:

$$t_3 = \frac{L \cdot I_{out}}{V_d}$$

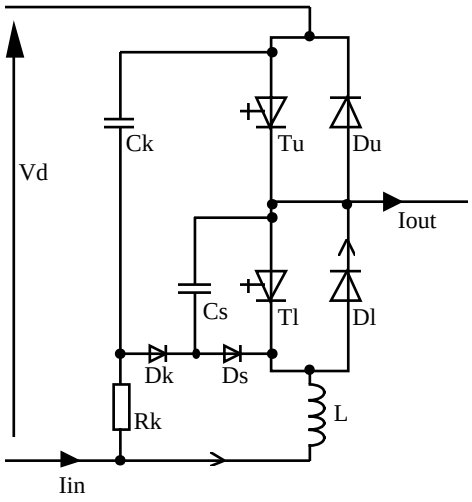

Figure A-4 *The commutation is complete.*

If the commutated current is so low that the time to discharge the snubber capacitor is longer than the dead time, the snubber capacitor will rapidly be discharged via the di/dt-inductor L and the lower GTO-thyristor, T_l, when it is turned on. The commutation delay:

$$t_4 = t_{dead} + t_d + \frac{t_f}{2}$$

The total commutation delay, see figure A-5:

$$t = MIN\left((k_{st} I_{out} + l_{st} + \frac{t_r}{2} + \frac{C_s}{2}(1 - \frac{C_s}{C_k})\frac{V_d}{I_{out}} - \frac{LI_{out}}{V_d}), (t_{dead} + t_d + \frac{t_f}{2})\right) \qquad (A1.1)$$

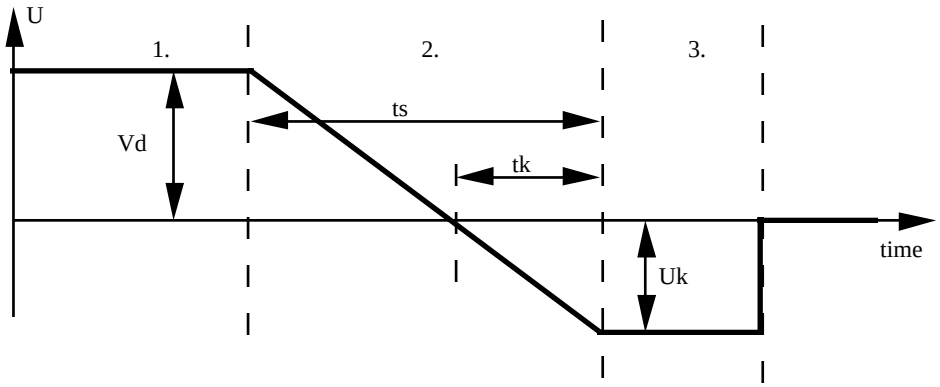

Figure A-5 *The output phase voltage, relative to the negative DC bar, during the commutation*

A.2 Lower diode commutation.

The phase current is positive, i.e. its direction is out from the phase, see figure A-6. The current commutates from lower anti parallel diode, D_l to upper GTO-thyristor T_u.

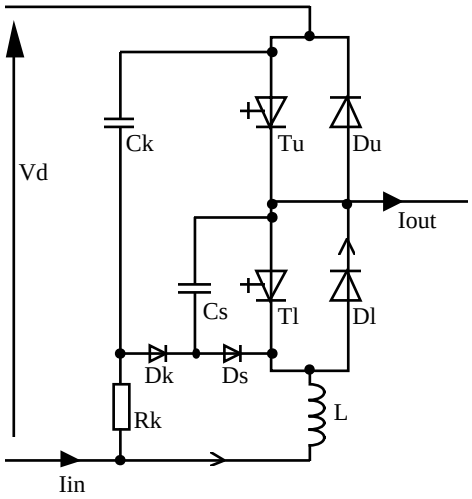

Figure A-6 *The current continuous through the diode at turn off of lower thyristor*

At start the lower GTO-thyristor, T_l, is turned off. Nothing happens with the output voltage, the current continues to flow through the lower diode D_l.

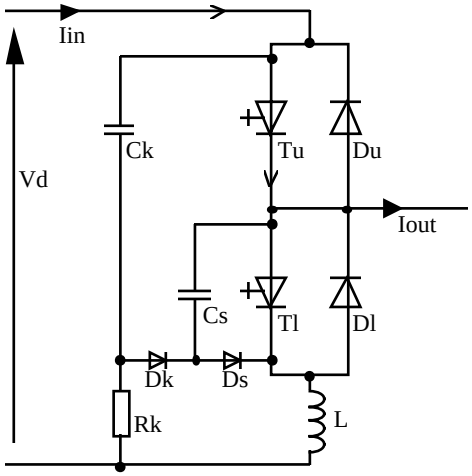

Figure A-7 *The phase output voltage becomes DC-link high voltage when the upper thyristor is turned on*

The dead time elapses and then the upper GTO-thyristor is turned on. After the delay time of the GTO-thyristor, the voltage over it drops during the fall time. After this moment, there is no voltage drop neither over the upper GTO-thyristor/diode nor the lower GTO-thyristor/diode, and the output voltage has reached the dc link

high voltage. The total DC-link voltage falls over the di/dt-inductor and the phase current starts to commutate from to the upper GTO-thyristor. When the current through the di/dt-inductor has become zero the voltage drop is moved from the inductor to the lower GTO-thyristor/diode and the output voltage remains unchanged. The total commutation delay, see figure A-8:

$$t = t_{dead} + t_d + \frac{t_f}{2} \qquad (A2.1)$$

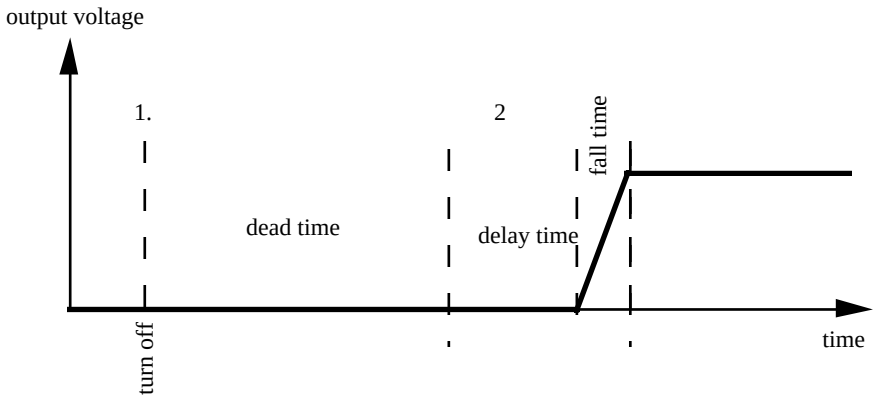

Figure A-8 *The output phase voltage, relative to the negative DC bar*

A.3 Lower GTO-thyristor commutation

The phase current is negative, i.e. its direction is in to the phase, see figure A-9.. The current commutates from lower GTO-thyristor *Tl*, to upper anti parallel diode *Du*.

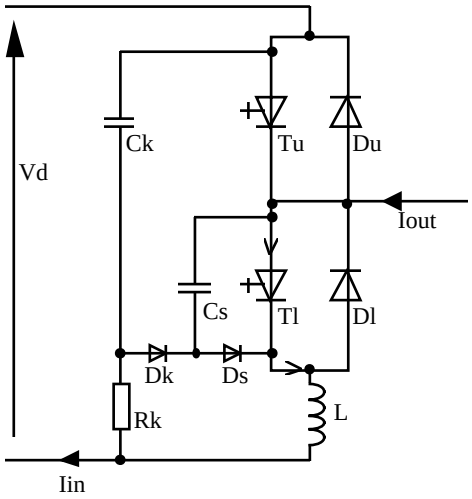

Figure A-9 *Turn off of the lower thyristor*

The turn off of *Tl*. First the storage time t_{st}, which is a linear function of commutated current, is elapsing. During this time the output voltage equals the DC-link low voltage. When the storage time has run out the current through T_u commutates to the snubber capacitor C_S. The time for this process is the rise time t_r. The average time for full voltage is half the rise time. The delay time for this part on the turn off (the minus sign because the current direction is defined negative):

$$t_1 = l_{st} - k_{st} I_{out} + \frac{t_r}{2}$$

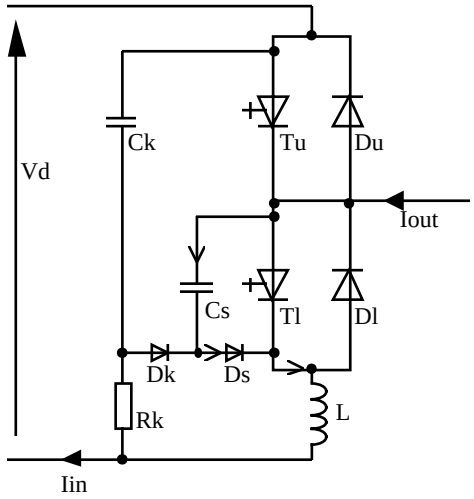

Figure A-10 *The current commutates to the snubber capacitor*

The snubber capacitor voltage increases to the dc link high voltage. Then the upper diode D_u, starts to conduct, and the output voltage reaches its end value, the DC-link high voltage. The delay time shall be multiplied with 0.5 as it is the voltage time area we are interested in. Due to the di/dt-inductor the current does not commutate immediately from the lower GTO-thyristor to the upper diode, but this does not affect the output voltage. The delay time for this part off the turn off (the minus sign because the current direction is defined negative):

$$t_2 = -\frac{1}{2} C_s \frac{V_d}{I_{out}}$$

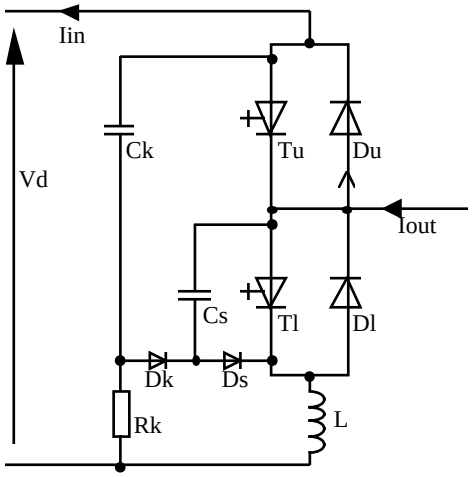

Figure A-11 *The current commutatest to upper anti parallel diode*

If the commutated current is too low the time to discharge the snubber capacitor may be longer than the dead time. If so the snubber capacitor will rapidly be discharged when the upper GTO-thyristor T_u, is turned on. The commutation delay for this part on the turn off is:

$$t_3 = t_{dead} + t_d + \frac{t_f}{2}$$

The total commutation delay, see figure A-12:

$$t = MIN\left((l_{st} - k_{st} I_{out} + \frac{t_r}{2} - \frac{1}{2} C_s \frac{V_d}{I_{out}}), (t_{dead} + t_d + \frac{t_f}{2}) \right) \qquad (A3.1)$$

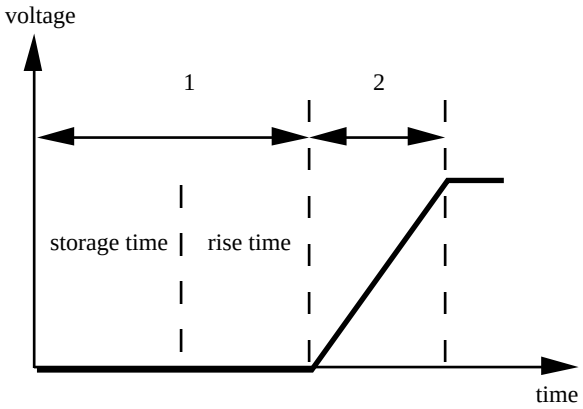

Figure A-12 *The output phase voltage, relative to the negative DC bar*

A.4 Upper diode commutation.

The phase current is negative, i.e. its direction is in to the phase, see figure A-13. The current commutates from upper anti parallel diode D_u, to lower GTO-thyristor Tl.

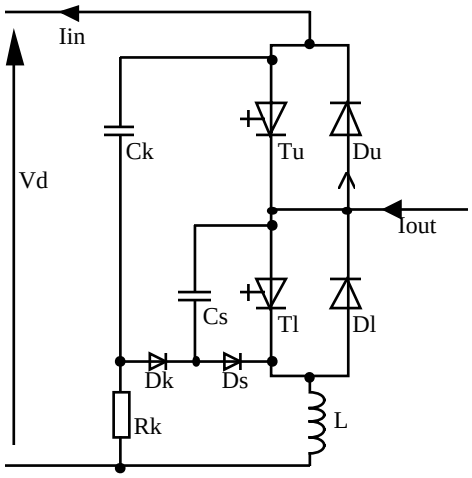

Figure A-13 *The current continuous to flow through upper anti parallel diode when the upper thyristor is turned off*

At start the upper GTO-thyristor T_u is turned off. Nothing happens, the output voltage remains unchanged, the current continuos to flow through the upper diode D_u.

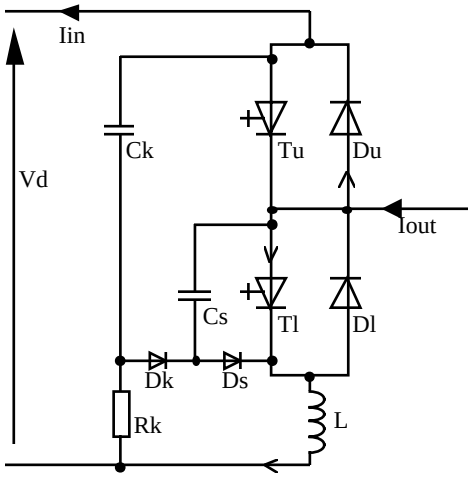

Figure A-14 *The current start to comuutate to the lower thyristor*

When the dead time, t_{dead}, has elapsed, the lower GTO-thyristor is turned on, and after the GTO-thyristor delay time plus half the fall time it starts conducting. Thereafter there is no voltage drop neither across the upper GTO-thyristor/diode nor the lower GTO-thyristor/diode. The total DC-link voltage is across the di/dt-

inductor and the phase current starts to commutate from upper diode to lower GTO-thyristor. When the current through the di/dt- inductor has become zero the voltage drop moves away from it to upper GTO-thyristor/diode. The commutation delay is

$$t_3 = t_{dead} + t_d + \frac{t_f}{2} - I_{out}\frac{L}{V_d}$$

When the voltage drop over the di/dt-inductor disappears the snubber capacitor starts to discharge via *Cs-Tl-L-Rk-Dk*. The output voltage decreases. The contribution to the delay time is the area at 3. in figure A-15.

When the capacitor is totally discharged, the current continues to flow through *L-Rk-Dk-Ds*. Because of the voltage drop across R_k the output voltage is lower than the DC-link low voltage, a "negative delay", the area under ”4”. in figure A-15. Since the energy in the snubber capacitor C_s is moved to the di/dt-inductor, the area at ”3”. equals the area at ”4”, and, therefore, these areas give no contribution to the delay time. The total commutation delay is

$$t_2 = t_{dead} + t_d + \frac{t_f}{2} - I_{out}\frac{L}{V_d} \qquad (A4.1)$$

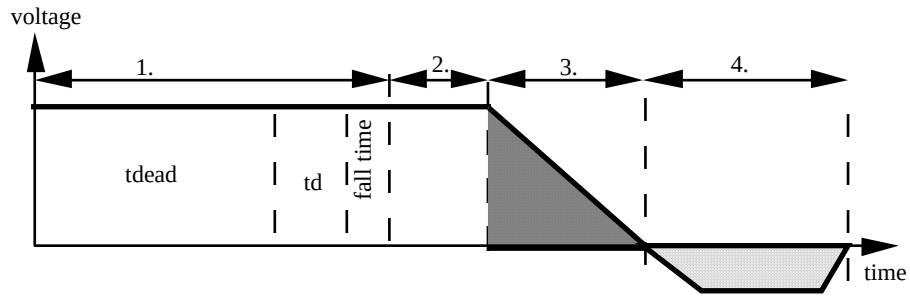

Figure A-15 *The output phase voltage, relative to the negative DC bar*

B Appendix B. ASCALP-Description

At Adtranz Sweden AB the author has written ASCALP (asynchronous motor drive calculation program), a general calculation tool, used when designing traction drive system based on three phase induction motors.

The main input data to ASCALP are the desired driving/braking effort, the vehicle speed, the line voltage and a large number of component parameters.

The program calculates:

- Magnitude of phase voltage, phase current, DC-link current and line current.
- Power loss and temperature in components. Components of interest are power semiconductors, DC-link capacitors, snubber components, transformers etc.
- The generation of phase current harmonics, DC-link current and line current harmonics. This part of ASCALP is described here.

Definitions

variables used in Ascalp:

u	voltage
i	current
S	modulation pattern
L	inductance
r	resistance
z	impedance
a	fourier cosinus coeffecients
b	fourier sinus coeffecients
c	fourier complex coeffecients
t	time
f	frequency
ω	angular frequency
s	slip
α	half of voltage stop vector duration
γ	control ratio

index:

M	machine inverter
R, S, T	machine converter phase R, S, T
H	”phase-to-phase”
L	line converter
b	line converter bridge
bn,1 bn,2	the two line converter phases connected to bridge n
B	brake chopper
B1, B2	brake chopper phases
D	dclink
n	commutations time points
k,l	frequecy components
s	stator
r	rotor
m	magnetic
tr	transformer

B.1 Calculation on the machine and its inverter

This chapter describes how the calculation of harmonics from the machine inverters is done. The calculation is done in following steps:

- Standard algorithm calculation of fundamental motor voltage and motor stator frequency needed to run the motors at desired speed and torque.
- Calculation of the modulation pattern in time domain. The calculation is based on the desired motor voltage, the stator frequnecy, the DC-link voltage, the maximum allowed switching frequency and t_{min}.
- Conversion of the modulation pattern to frequency domain.
- Calculation of the phase current in frequency domain.
- The phase current is there after converted back to time domain to be able to calculate the switching power loss.
- Calculation of the current from the dclink to the machine inverter, here called the dclink current. This is done both in time and in frequency domain.

Motor calculation model

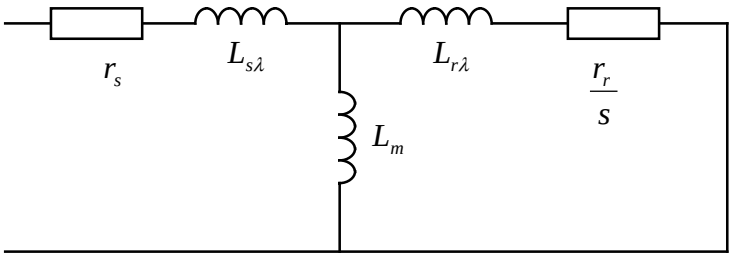

Figure B-1 *Ascalp uses this motor model, both for fundamental and harmonic calculations ([18] page 231).*

The parameters $r_s, L_{s\lambda}, r_r, L_{r\lambda}, L_m$ are together with the desired fundamental stator frequency f_s and the desired motor phase-to-phase voltage U_H received from a standard program, used at Adtranz, for fundamental frequency calculations of the motor.

The slip for the fundamental frequency

$$s = \frac{\omega_s - \omega}{\omega_s}$$

The slip for the k:th harmonic, where *k=4, 7, 10* etc

$$s_{k+} = \frac{k \cdot \omega_s - \omega}{k \cdot \omega_s}$$

This expression is also used for the k:th harmonic, where *k=3, 6, 9, etc. However, these harmonics have low impact to the calculated result, because they will be cancelled in a three phase inverter.*

The slip for the *k:th* harmonic, where *k=2, 5, 8* etc

$$s_{k-} = \frac{-k \cdot \omega_s - \omega}{-k \cdot \omega_s} = \frac{k \cdot \omega_s + \omega}{k \cdot \omega_s}$$

Calculation of the machine inverter modulation patterns

The modulation patterns here described are the modulation pattern used in chapter 4.

Sinusoidal-modulation. The sinusoidal modulation pattern is achieved by letting a triangular wave intersect the desired sinusoidal shaped voltage wave, see figure 4-5. The triangular wave frequency equals the maximum switching

frequency, and its peak-to-peak value equals +/-the dc-link dc voltage. The amplitude and the frequency of the sinusoidal wave equals the desired phase-voltage and the desired fundamental stator frequency of the motor. The intersection points between the sinusoidal wave and the triangular wave will determine the inverter commutation time points. When the triangular wave is less than the sinusoidal wave the modulation pattern is high, and when the triangular wave is larger the modulation pattern is low. The intersection points are found by iteration, and the iteration stops when the time resolution is less then 10 ns. (about 10 times shorter than the commutation precison of an IGBT.)

Iteration process. Find the points of time where the function, see figure B-2.

y(tn)=(sinusoidal wave - triangular wave)=0

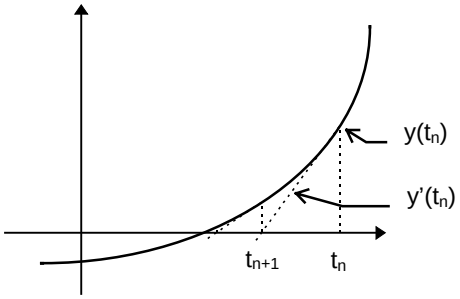

Figure B-2 *Iterative solving*

Start with t_n and find the next t_{n+1}:

$$t_{n+1} = t_n - \frac{y(t)}{y'(t)}$$

This iterations converges fast, four to five loops is normally enough to reach the precision of 10 ns. One condition for convergence is that the triangular wave has a frequency that is at least three times the frequency of the sinusoidal wave.

The maximum control ratio of the sinusoidal modulation can be increase from the normal 0.785 to 0.907 by adding a sinusoidal voltage with a frequency three times the fundamental frequency, and with an amplitude 25% of the fundamental voltage amplitude. A phase angle is used, which makes the sum of the two waves lower than the triangular wave peak value even with a larger fundamental voltage amplitude. This added third harmonic common mode voltage is cancelled in the three phase inverter.

At calculation of the sinusoidal-modulation it is checked that there will be no conflict with t_{min}, the minimum time between two commutation in the same phase of the inverter.

p18-modulation. This is a polar modulation with three voltage stop vectors per side in the hexagon. The longer the stops the lower the output voltage. The length of half the stop duration α, in radians, for a certain output voltage will be determined by Fourier series expansion.

$$\alpha = \arcsin\frac{1-\gamma}{4\cdot(\cos(\frac{\pi}{9})+0.5)})$$

The voltage control ratio:

$$\gamma = \frac{U_H}{\frac{\sqrt{6}}{\pi}\cdot U_D}$$

At calculation of the p18-modulation it is checked that there will be no conflict with t_{min}. The commutation frequency:

$$f_{com} = 7 \cdot f_s$$

where f_s is the motor stator frequency.

e6-modulation. This is a polar modulation with one voltage stop vector per side in the hexagon. The hexagon has ”folded corners”. The length α, in radians, of half the stop duration for a certain output voltage with a corner fold of $\frac{\pi}{18}$ will be determined by Fourier series expansion.

$$\alpha = \arcsin\left(\cos\left(\frac{\pi}{18}\right) - \frac{1+\gamma}{2}\right)$$

The voltage control ratio:

$$\gamma = \frac{U_H}{\frac{\sqrt{6}}{\pi}\cdot U_D}$$

At the calculation of the e6-modulation, it is checked that there will be no conflict with t_{min}. The commutation frequency:

$$f_{com} = 5 \cdot f_s$$

where f_s is the motor stator frequency.

p6-modulation. This is a polar modulation with one voltage stop per hexagon side. The length α, in radians, of half the stop duration for a certain output voltage will be determined by Fourier series expansion.

$$\alpha = \arcsin\left(\frac{1-\gamma}{2}\right)$$

The voltage control ratio:

$$\gamma = \frac{U_H}{\frac{\sqrt{6}}{\pi} \cdot U_D}$$

At calculation of the p12-modulation it is checked that there will be no conflict with t_{min}. The commutation frequency:

$$f_{com} = 3 \cdot f_s$$

where f_s is the motor stator frequency.

em-modulation. This is a polar modulation where a certain output voltage is achieved by ”folding the corners”. The length β, in radians, of the corner fold is determined by Fourier series expansion.

$$\beta = \arccos\left(\frac{1+\gamma}{2}\right)$$

The voltage control ratio:

$$\gamma = \frac{U_H}{\frac{\sqrt{6}}{\pi} \cdot U_D}$$

At calculation of the e6-modulation it is checked that there will be no conflict with t_{min}. The minimum output voltage for em modulation pattern is limited by the control system computer execution time. The commutation frequency:

$$f_{com} = 3 \cdot f_s$$

where f_s is the motor stator frequency.

hex-modulation (=square wave). This is a polar modulation where the output voltage, U_h, cannot be varied, it is only depending on the dc-link voltage.

$$U_H = \frac{\sqrt{6}}{\pi} \cdot U_D$$

The commutation frequency:

$$f_{com} = f_s$$

where f_s is the motor stator frequency.

Converting the modulation pattern to frequency domain

The modulation pattern in all three phases of the machine inverter are generated in time domain. The calculation can thereafter be done in one of two ways, either make the voltage and current calculations in the time domain and then convert the result to the frequency domain. The alternative is to converte the modulation pattern to the frequency domain and then make the calculations in frequency domain. If the calculations are done in the time domain a large number of points of time with very short time steps in between must be used in order to get full accuracy at the highest frequency of interest. If the modulation pattern instead is converted to the frequency domain by Fourier series expansion, the modulation pattern itself can be used as the time function in the Fourier integrals, which now are easily integrated, as the time function is constant and either equals one or equal zero. Therefore the number of calculation points equals the number of commutation points and are for most modulation patterns low.

The modulation pattern dc-component in phase R is ([16] page 31):

$$S_R a_0 = \frac{1}{T}\sum_n \left(\int_{t_{2n-1}}^{t_{2n}} f(t)dt \right) = \frac{1}{T}\sum_n \left(\int_{t_{2n-1}}^{t_{2n}} 1 \cdot dt + 0 \right) = \frac{1}{T}\sum_n \left(t_{2n} - t_{2n-1} \right)$$

The modulation pattern cosines coefficients in phase R for the k:th harmonic are ([16] page 31):

$$S_R a_k = \frac{2}{T} \cdot \sum_n \left(\int_{t_{2n-1}}^{t_{2n}} f(t) \cdot \cos(k\omega t)dt \right) = \frac{2}{T} \cdot \sum_n \left(\int_{t_{2n-1}}^{t_{2n}} \left(1 \cdot \cos(k\omega t) + 0\right) \cdot dt \right) =$$

$$= \frac{1}{k\pi} \cdot \sum_n \left(\sin\left(k\omega t_{2n}\right) - \sin\left(k\omega t_{2n-1}\right) \right)$$

The modulation pattern sinus coefficients in phase R for the k:th harmonic are ([16] page 31):

$$S_R b_k = \frac{2}{T} \cdot \sum_n \left(\int_{t_{2n-1}}^{t_{2n}} f(t) \cdot \sin(k\omega t)dt \right) = \frac{2}{T} \cdot \sum_n \left(\int_{t_{2n-1}}^{t_{2n}} \left(1 \cdot \sin(k\omega t) + 0\right) \cdot dt \right) =$$

$$= \frac{1}{k\pi} \cdot \sum_n \left(\cos\left(k\omega t_{2n-1}\right) - \cos\left(k\omega t_{2n}\right) \right)$$

Calculation of the machine inverter phase voltage with a pure dc-link voltage without harmonics

The phase voltage of an inverter is calculated by multiplying the dc-link voltage with the phase modulation pattern.

In the frequency domain this can easily be done as long as the dc-link voltage can be regarded as a pure dc-voltage U_D.

The voltage dc component in phase R:

$$U_R a_0 = U_D \cdot S_R a_0$$

The voltage cosine coefficient in phase R:

$$U_R a_k = U_D \cdot S_R a_k$$

The voltage sine coefficient in phase R:

$$U_R b_k = U_D \cdot S_R b_k$$

Calculation of the machine inverter phase voltage with a dc-link voltage containing harmonics

When the DC-link voltage also contain harmonics, we must first make a Fourier expansion of both the dc-link voltage and the phase modulation pattern, and then multiply these two expressions. This will end up in a large number of multiplication since each frequency component in the dc-link voltage must be multiplied by all frequency components in the modulation pattern. Frequency components with both frequency sum and the frequency difference are produced.

The R-phase voltage:

$$U_R = \left(U_D a_0 + \sum_k U_D a_k \cdot \cos(k\omega_k t) + U_D b_k \cdot \sin(k\omega_k t) \right) \cdot$$

$$\cdot \left(S_R a_0 + \sum_l S_R a_l \cdot \cos(l\omega_l t) + S_R b_l \cdot \sin(l\omega_l t) \right)$$

$$U_R = U_D a_0 \cdot S_R a_0 + U_d a_0 \cdot \sum_l \left(S_R a_l \cdot \cos(l\omega_l t) + S_R b_n \cdot \sin(l\omega_l t) \right) +$$

$$+ S_R a_0 \cdot \sum_k U_d a_k \cdot \cos(k\omega_k t) + U_d b_k \cdot \sin(k\omega_k t) +$$

$$+\sum_l\sum_k \frac{U_D a_k \cdot S_R a_l}{2}\left(\cos\left(\left(l\omega_l + k\omega_k\right)\cdot t\right) + \cos\left(\left(l\omega_l - k\omega_k\right)\cdot t\right)\right) +$$

$$+\sum_l\sum_k \frac{U_D a_k \cdot S_R b_l}{2}\left(\sin\left(\left(l\omega_l + k\omega_k\right)\cdot t\right) - \sin\left(\left(l\omega_l - k\omega_k\right)\cdot t\right)\right) +$$

$$+\sum_l\sum_k \frac{U_D b_k \cdot S_R a_l}{2}\left(\sin\left(\left(l\omega_l + k\omega_k\right)\cdot t\right) + \sin\left(\left(l\omega_l - k\omega_k\right)\cdot t\right)\right) +$$

$$+\sum_l\sum_k \frac{U_D b_k \cdot S_R b_l}{2}\left(\cos\left(\left(l\omega_l + k\omega_k\right)\cdot t\right) - \cos\left(\left(l\omega_l - k\omega_k\right)\cdot t\right)\right)$$

The following trigonometric expressions are used:

$$A\sin\left(l\omega_l t\right)\cdot B\cos\left(k\omega_k t\right) = \frac{AB}{2}\sin\left(\left(l\omega_l + k\omega_k\right)\cdot t\right) + \frac{AB}{2}\sin\left(\left(l\omega_l - k\omega_k\right)\cdot t\right)$$

$$A\cos\left(l\omega_l t\right)\cdot B\sin\left(k\omega_k t\right) = \frac{AB}{2}\sin\left(\left(l\omega_l + k\omega_k\right)\cdot t\right) - \frac{AB}{2}\sin\left(\left(l\omega_l - k\omega_k\right)\cdot t\right)$$

$$A\cos\left(l\omega_l t\right)\cdot B\cos\left(k\omega_k t\right) = \frac{AB}{2}\cos\left(\left(l\omega_l + k\omega_k\right)\cdot t\right) + \frac{AB}{2}\cos\left(\left(l\omega_l - k\omega_k\right)\cdot t\right)$$

$$A\sin\left(l\omega_l t\right)\cdot B\sin\left(k\omega_k t\right) = \frac{AB}{2}\cos\left(\left(l\omega_l + k\omega_k\right)\cdot t\right) - \frac{AB}{2}\cos\left(\left(l\omega_l - k\omega_k\right)\cdot t\right)$$

The product of $U_D a_0$ and $S_{MR} a_0$ and the cosine terms where

$$\left(l\omega_l - k\omega_k\right) = 0$$

contributes to the dc component. Ascalp uses this way to cross modulate the phase voltage with the dclink voltage ripple, e.g. when the brake chopper dc-link voltage ripple is modulated by the machine inverter.

Calculation of the machine inverter phase to phase voltage

The phase to phase voltage is recieved by subtracting one phase voltage from the other, both in time domain and in frequency domain.

The complex phase voltage

Conversion from the Fourier expansion series coefficients a_k and b_k to a complex voltage amplitude.

The fourier expansion series (definition):

$$x(t) = a_0 + \sum_{k=1}^{\infty} a_k \cos(k\omega t) + \sum_{k=1}^{\infty} b_k \sin(k\omega t)$$

where

$$a_k = \frac{2}{T}\int_0^T x(t)\cdot\cos(k\omega t)dt$$

$$b_k = \frac{2}{T}\int_0^T x(t)\cdot\sin(k\omega t)dt$$

The complex fourier expansion series (definition) ([16] page 39):

$$x(t) = \sum_{k=-\infty}^{\infty} c_k e^{jk\omega t} = c_0 + \sum_{k=1}^{\infty} c_k e^{jk\omega t} + \sum_{k=1}^{\infty} c_{-k} e^{-jk\omega t} =$$

$$= c_0 + \sum_{k=1}^{\infty} c_k \left(\cos(k\omega t) + j\cdot\sin(k\omega t)\right) + \sum_{k=1}^{\infty} c_{-k}\left(\cos(-k\omega t) + j\cdot\sin(-k\omega t)\right)$$

$$= c_0 + \sum_{k=1}^{\infty} \left(c_k + c_{-k}\right)\cdot\cos(k\omega t) + j\cdot\left(c_k - c_{-k}\right)\cdot\sin(k\omega t)$$

The complex coefficients:

$$c_k = \frac{1}{T}\int_0^T x(t)\cdot e^{-jk\omega t}dt = \frac{1}{T}\int_0^T x(t)\cdot\left(\cos(-k\omega t) + j\cdot\sin(-k\omega t)\right)dt =$$

$$\frac{1}{2}\cdot\frac{2}{T}\int_0^T x(t)\cdot\cos(k\omega t)dt - j\cdot\frac{1}{2}\cdot\frac{2}{T}\int_0^T x(t)\cdot\sin(k\omega t)dt = \frac{a_k}{2} - j\cdot\frac{b_k}{2}$$

In the same way for c_{-k}:

$$c_{-k} = \frac{a_k}{2} + j\cdot\frac{b_k}{2}$$

And:

$$c_k + c_{-k} = a_k$$

$$c_k - c_{-k} = -j\cdot b_k$$

finally the complex amplitude for the k:th harmonic:

$$\left(a_k - j\cdot b_k\right)$$

Calculation of the motor phase impedance

See figure B-1.

The complex stator impedance is

$$Z_s = r_s + j\omega L_{s\lambda}$$

The complex rotor impedance is

$$Z_r = r_r + j\omega L_{r\lambda}$$

The complex magnetizing impedance is

$$Z_m = j\omega L_m$$

The complex motor phase impedance is

$$Z = Z_s + \frac{Z_r \cdot Z_m}{Z_r + Z_m}$$

Calculation of the machine inverter phase current

The phase impedances are connected in a star configuration with the junction point not connected to zero.

The voltage in the junction point is U_0. The three complex phase voltages are U_R, U_S, U_T and the three complex phase currents are I_R, I_S, I_T. Following equation:

$$\begin{cases} I_R \cdot Z = U_R - U_0 \\ I_S \cdot Z = U_S - U_0 \\ I_T \cdot Z = U_T - U_0 \end{cases}$$

after elimination of U_0 the phase-currents of the motor are received:

$$\begin{cases} I_R = \dfrac{2 \cdot U_R - U_S - U_T}{3Z} \\ I_S = \dfrac{2 \cdot U_S - U_T - U_R}{3Z} \\ I_T = \dfrac{2 \cdot U_T - U_R - U_S}{3Z} \end{cases}$$

By multiplication with the number of motors per machine inverter, the machine inverter phase currents are received.

Conversion of the phase current from the frequency domain to the time domain

When the inverter component losses are calculated, the time domain phase current and the time domain modulation pattern is used. The time domain modulation pattern is already known, and, now, only the frequency domain phase current shall be converted to time domain by using the inverse Fourier series expansion:

Phase *R* time domain current is.

$$i_R(t) = i_R a_0 + \sum_{k=1}^{n} i_R a_k \cdot \cos(k\omega t) + \sum_{k=1}^{n} i_R b_k \cdot \sin(k\omega t)$$

The precision, but also the calculation time increases with the number of harmonics used.

Calculation of the commutation delay

Until now ideal commutations have been assumed. After the calculation of the time domain phase current, the actual commutation delay can be calculated at each commutation, see appendix A. The effect of commutation delay can then be found, if the modulation pattern is corrected with this delay. Then all the calculations shall be done once again.

Calculation of the current from the DC-link to the machine inverter

When the modulation pattern is”one”, the phase current is going through the upper GTO or through the upper free wheel diode, and when the modulation pattern is “zero” the current will go through the lower GTO/free wheel diode pair. Thus the current through the component in the upper position, in time domain, is equal to the modulation pattern times the phase current. The total DC-link current, in time domain, is the sum of the contribution from all three phases.

$$i_D(t) = S_R i_R(t) + S_S i_S(t) + S_T i_T(t)$$

If the time domain functions are expressed in Fourier coefficients the frequency content of the dclink current will easily be found. The phase currents, i_R, and the modulation pattern, S_R, are for phase *R*:

$$S_R(t) = S_R a_0 + \sum_{k=1}^{\infty} S_R a_k \cdot \cos(k\omega_k t) + \sum_{k=1}^{\infty} S_R b_k \cdot \sin(k\omega_k t)$$

and the phase current:

$$i_R(t) = i_R a_0 + \sum_{l=1}^{\infty} i_R a_l \cdot \cos(l\omega_l t) + \sum_{k=1}^{\infty} i_R b_l \cdot \sin(l\omega_l t)$$

By multiplication of these two expressions, we recieve the contribution from phase *R* to the total dc-link current. By doing the same actions for phase S and for phase T and then add the results we get the total DC-link current in time domain. As the time domain expression is expressed in fourier coefficients, the frequency domain dclink current will easily be found.

$$i_D(t) = i_R a_0 \cdot S_R a_0 + i_R a_0 \cdot \sum_k \left(S_R a_k \cos(k\omega t) + S_R b_k \sin(k\omega t)\right) +$$

$$+ S_R a_0 \cdot \sum_l I_R a_l \left(\cos(l\omega_l t) + I_R b_l \sin(l\omega_l t)\right) +$$

$$+ \sum_l \sum_k \frac{I_R a_k \cdot S_R a_l}{2} \left(\cos\left(\left(l\omega_l + k\omega_k\right) \cdot t\right) + \cos\left(\left(l\omega_l - k\omega_k\right) \cdot t\right)\right) +$$

$$+ \sum_l \sum_k \frac{I_R a_k \cdot S_R b_l}{2} \left(\sin\left(\left(l\omega_l + k\omega_k\right) \cdot t\right) - \sin\left(\left(l\omega_l - k\omega_k\right) \cdot t\right)\right) +$$

$$+ \sum_l \sum_k \frac{I_R b_k \cdot S_R a_l}{2} \left(\sin\left(\left(l\omega_l + k\omega_k\right) \cdot t\right) + \sin\left(\left(l\omega_l - k\omega_k\right) \cdot t\right)\right) +$$

$$+ \sum_l \sum_k \frac{I_R b_k \cdot S_R b_l}{2} \left(\cos\left(\left(l\omega_l + k\omega_k\right) \cdot t\right) - \cos\left(\left(l\omega_l - k\omega_k\right) \cdot t\right)\right)$$

B.2 Calculation of the brake chopper

This chapter describes the calculation of harmonics produced by the brake chopper. The brake chopper consists normally of two brake chopper phases in parallel with the dclink capacitor.

Calculation of the total brake chopper current

First it is checked that the vehicle is in braking mode and that the machine inverter regenerates power. If there is an auxiliary inverter on the same dc-link it is also checked that more power is regenerated than is consumed by the auxiliary inverter. If so, the amount of the regenerated power that shall be consumed by the brake chopper is calculated.

Calculation of the brake chopper control ratio and the brake chopper pulse time

The total brake chopper current:

$$I_B = \frac{P_B}{U_D}$$

where P_B is the brake power through the brake chopper.

The brake chopper current per phase:

$$I_{Bp} = \frac{I_B}{m_B}$$

where m_B is the number of brake chopper phases per machine inverter.

The maximum current per brake chopper phase:

$$I_{Bp\_\max} = \frac{U_D}{r_B}$$

where r_B is the brake resistor resistance.

The brake chopper control ratio:

$$\gamma = \frac{I_{\mathrm{Bp}}}{\mathrm{I}_{\mathrm{Bp\_max}}}$$

The brake chopper modulation pattern in the time domain

The brake chopper period time:

$$T_B = \frac{1}{f_B}$$

The brake chopper phase pulse time:

$$t_{pulse} = \gamma \cdot T_B$$

It is checked that the pulse time point has duration longer than t_{min}.

The pulse turn on time for the *m:th* phase:

$$t_m(n) = \frac{m-1}{m_B} \cdot T_B$$

The pulse turn off time point for the *m:th* phase:

$$t_m(n+1) = t_m(n) + t_{pulse}$$

$$1 \le m \le m_B$$

The turn on delay:

$$t_{delay} + \frac{t_{rise}}{2} + \tau_B$$

The turn off delay:

$$t_{storage} + \frac{t_{fall}}{2} + \tau_B$$

Where the brake resistor time constant τ_B is the brake resistor inductance divided by its resistance.

The brake chopper modulation pattern in the frequency domain

The modulation pattern for *m:th* phase, the DC-component:

$$a_0(m) = \frac{t_{pulse}}{T_B}$$

The cosine coefficients ([16] page 31):

$$a_k(m) = \frac{2}{T_B} \int_{t_m(n)}^{t_m(n+1)} \cos(k\omega t)dt$$

The sine coefficients ([16] page 31):

$$b_k(m) = \frac{2}{T_B} \int_{t_m(n)}^{t_m(n+1)} \sin(k\omega t)dt$$

$$\omega = 2\pi \cdot f_B$$

The *m:th* phase current DC-component:

$$ia_0(m) = \frac{a_0(m) \cdot U_D}{r_B}$$

The *m:th* phase current cosine coefficient:

$$ia_k(m) = \frac{a_k(m) \cdot U_D}{r_B}$$

The *m:th* phase current sine coefficient:

$$ib_k(m) = \frac{b_k(m) \cdot U_D}{r_B}$$

The total current from the dc-link to the brake chopper. The DC-component:

$$ia_0 = \sum_m ia_0(m)$$

The cosine-coefficient:

$$ia_k = \sum_m ia_k(m)$$

The sine-coefficient:

$$ib_k = \sum_m ib_k(m)$$

The total modulation pattern:

$$s_B a_0 = \frac{ia_0 \cdot r_B}{U_D}$$

The current cosine component:

$$s_B a_k = \frac{ia_k \cdot r_B}{U_D}$$

The current sine component:

$$s_B b_k = \frac{ib_k \cdot r_B}{U_D}$$

B.3 The line converter calculations

In this chapter the generation of phase current from the line converter will be calculated. The calculation will be done in the following steps:

- Calculation of the DC current to the DC-link, based on the power needed for the machine inverter, the brake choppers and the auxiliary inverter.

- Calculation of the fundamental frequency phase-to-phase voltage, the bridge voltage U_b that the line converter shall apply to the transformer secondary winding in order to control the power.
- Calculation of the modulation pattern in time domain. The calculation is based on the desired line converter bridge voltage, the line frequnecy, the dclink voltage, the maximum allowed switching frequency and t_{min}. It is also taken into account if the phase currents shall be interlaced.
- Conversion of the modulation pattern to the frequency domain.
- Calculation of all phase currents in the frequency domain.
- The phase current is thereafter converted back to time domain, to be able to calculate the switching power loss.
- Calculation of the current from the line converter to the dclink, here called the DC-link current. This is done both in time and in frequency domain.

Calculation of the dc component of the current from the line converter to the dc-link.

The power from the line converter :

$$U_D \cdot I_{Ldc} = U_D \cdot I_{Mdc} + U_D \cdot I_{Bdc} + U_D \cdot I_{Adc}$$

where:

- $U_D \cdot I_{Mdc}$ is the power to the machine inverter
- $U_D \cdot I_{Bdc}$ is the power to the brake choppers, if any
- $U_D \cdot I_{Adc}$ is the power to the auxiliary inverter, if any

Calculation of the fundamental line converter bridge voltage, the phase current and the phase angle

The power from the line converter to the DC-link(or backwards in braking mode)

$$P = I_{Ldc} \cdot U_D$$

To this power, the estimated transformer loss is added:

$$P_{tot} = P + P_{tr}$$

The calculations are done at the transformer primary side.

The phase angle between the line voltage and the line current is assumed to be zero (*cos(ϕ)=1*).

$$I_{line} = \frac{P_{tot}}{U_{line}}$$

The line converter phase current I_b is found by dividing I_{line} by the number of transformer secondary windings, i.e. the number of bridges:

$$I_b = \frac{I_{line}}{tr_{\sec}}$$

The phase current and the line voltage are converted to complex numbers. The transformer average impedance per phase is z_{tr}. The fundamental voltage U_b:

$$U_{line} - U_b = I_b \cdot z_{tr}$$

$$U_b = U_{line} - I_b \cdot z_{tr}$$

It is now checked that $U_b \le U_{b\_\max}$, the maximum output phase to phase voltage from the line converter. If it is not possible to handle the phase current amount by displacing the line voltage and the line current a certain phase angle. Arctan for the phase angle (=*x*) is found by solving the equation:

$$x^2 ABS\left(U_{line} - U_b\right)^2 + xI_{line}\left(\mathrm{Im}\left(z_{tr}\right)\mathrm{Re}\left(U_b\right) - \mathrm{Re}\left(z_{tr}\right)\mathrm{Im}\left(U_b\right)\right) + ABS\left(U_b\right)^2 - {U_{b\_\max}}^2 = 0$$

The imaginary part, caused by the non zero phase angle, shall be added to the complex phase current. Once again the line converter bridge voltage shall be calculated:

$$U_b = U_{line} - I_b \cdot z_{tr}$$

The phase angle of the line converter voltage

$$\Phi_{Ub} = \arctan\left(\frac{\mathrm{Im}(U_b)}{\mathrm{Re}(U_b)}\right)$$

Calculation of the modulation pattern for each line converter

The modulation patterns for the two phases in a line converter bridge are found by letting one triangular wave intersect two fundamental sinusoidal waves, one for each phase. The amplitude for the fundamental phase voltages is $\frac{\mathrm{U_b} \cdot \sqrt{2}}{2}$ and

they are displaced 180 degrees. The phase angle for both phases is ϕ_{Ub}. Regarding the mathematical aspects of how the intersect points of time etc are found, see the machine inverter sinusoidal modulation description.

The triangular wave in the different bridge voltages are interlaced, and are chosen in a way that generates the lowest interference, both taking the line current and the DC-link voltage into account. I.e. if there are two line converters bridges in one traction module the phase shift between the two triangular waves is 90°. If there is another traction module with two line converter bridges the phase shift between the two phase in that traction module will also be 90°. The phase shift between one phase in the first traction module and the same inverter in the second traction module is 45°. If there are three traction modules the phase shift is 30°, etc.

The modulation patterns for each phase are converted to the frequency domain, see ”Converting the modulation pattern to the frequency domain” in the machine inverter modulation pattern description.

Calculation of the line converter phase voltage with a pure dc-link voltage without harmonics

The phase voltage of a line converter is found by multiplication of the DC-link voltage by the phase modulation pattern

The modulation pattern DC-component in a phase is ([16] page 31):

$$S_b a_0 = \frac{1}{T}\sum_n \left(\int_{t_{2n-1}}^{t_{2n}} f(t)dt \right) = \frac{1}{T}\sum_n \left(\int_{t_{2n-1}}^{t_{2n}} 1 \cdot dt + 0 \right) = \frac{1}{T}\sum_n \left(t_{2n} - t_{2n-1} \right)$$

The modulation pattern cosines coefficients in a phase are ([16] page 31):

$$S_b a_k = \frac{2}{T} \cdot \sum_n \left(\int_{t_{2n-1}}^{t_{2n}} f(t) \cdot \cos(k\omega t)dt \right) = \frac{2}{T} \cdot \sum_n \left(\int_{t_{2n-1}}^{t_{2n}} \left(1 \cdot \cos(k\omega t) + 0\right) \cdot dt \right) =$$

$$= \frac{1}{k\pi} \cdot \sum_n \left(\sin\left(k\omega t_{2n}\right) - \sin\left(k\omega t_{2n-1}\right) \right)$$

The modulation pattern sinus coefficients in a phase are ([16] page 31):

$$S_b b_k = \frac{2}{T} \cdot \sum_n \left(\int_{t_{2n-1}}^{t_{2n}} f(t) \cdot \sin(k\omega t)dt \right) = \frac{2}{T} \cdot \sum_n \left(\int_{t_{2n-1}}^{t_{2n}} \left(1 \cdot \sin(k\omega t) + 0\right) \cdot dt \right) =$$

$$= \frac{1}{k\pi} \cdot \sum_n \left(\cos\left(k\omega t_{2n-1}\right) - \cos\left(k\omega t_{2n}\right) \right)$$

The phase voltage DC-component:

$$U_b a_0 = U_D \cdot S_b a_0$$

The phase voltage cosine coefficient:

$$U_b a_k = U_D \cdot S_b a_k$$

The phase voltage sine coefficient:

$$U_b b_k = U_D \cdot S_b b_k$$

Calculation of the line converter phase voltage with a DC-link voltage containing harmonics

When the dc-link voltage also contains harmonics, we must first make fourier series expansions of both the DC-link voltage and the phase modulation pattern, and then multiply these two expressions. This will end up in a large number of multiplication since each frequency component in the DC-link voltage must be multiplied with all frequency components in the modulation pattern. The resulting frequency components will contain both the frequency sum and the frequency difference.

The voltage in a phase is found by multiplying the DC-link voltage harmonics with the phase modulation pattern harmonics:

$$U_b = \left(U_D a_0 + \sum_k U_D a_k \cdot \cos\left(k\omega_k t\right) + \sum_k U_D b_k \cdot \sin\left(k\omega_k t\right) \right) \cdot \left(S_b a_0 + \sum_l S_b a_l \cdot \cos\left(l\omega_l t\right) + \sum_l S_b b_l \cdot \sin\left(l\omega_l t\right) \right)$$

$$U_b = U_D a_0 \cdot S_b a_0 + U_D a_0 \cdot \sum_l \left(S_b a_l \cos\left(l\omega_l t\right) + S_b b_l \sin\left(l\omega_l t\right) \right) +$$

$$+ S_b a_0 \cdot \sum_k U_D a_k \left(\cos\left(k\omega_k t\right) + U_D b_k \sin\left(k\omega_k t\right) \right) +$$

$$+ \sum_l \sum_k \frac{U_D a_k \cdot S_b a_l}{2} \left(\cos\left(\left(l\omega_l + k\omega_k\right) \cdot t \right) + \cos\left(\left(l\omega_l - k\omega_k\right) \cdot t \right) \right) +$$

$$+ \sum_l \sum_k \frac{U_D a_k \cdot S_b b_l}{2} \left(\sin\left(\left(l\omega_l + k\omega_k\right) \cdot t \right) - \sin\left(\left(l\omega_l - k\omega_k\right) \cdot t \right) \right) +$$

$$+ \sum_l \sum_k \frac{U_D b_k \cdot S_b a_l}{2} \left(\sin\left(\left(l\omega_l + k\omega_l\right) \cdot t \right) + \sin\left(\left(l\omega_l - k\omega_k\right) \cdot t \right) \right) +$$

$$+\sum_{l}\sum_{k}\frac{U_D b_k \cdot S_b b_l}{2}\left(\cos\left(\left(l\omega_l + k\omega_k\right)\cdot t\right) - \cos\left(\left(l\omega_l - k\omega_k\right)\cdot t\right)\right)$$

Contributions to the DC-component is recieved from the product of $U_D a_o$ and $s_b a_o$ but also from those cosine terms where

$(l\omega_l - k\omega_k) = 0$

Ascalp uses this way to calculate the phase voltage in the cross modulation interference frequency calculations, e.g. when the machine inverter dc-link voltage ripple is modulated by the line converter. The voltage of the other phase, connected to the same bridge is calculated in a similar way, and the bridge voltage is found by taking the difference between the two phase voltages.

Calculation of the line converter bridge current

The fundamental frequency phase current and the phase current for each harmonics will be found by solving the complex equation system:

$$\begin{cases} U_{s1} = \omega_k L_{11}\cdot I_1 + \omega_k M_{12}\cdot I_2 + \omega_k M_{13}\cdot I_3 + \ldots + \omega_k M_{1n}\cdot I_n + \left(u_{b1,1} - u_{b1,2}\right) \\ U_{s2} = \omega_k L_{21}\cdot I_1 + \omega_k M_{22}\cdot I_2 + \omega_k M_{23}\cdot I_3 + \ldots + \omega_k M_{2n}\cdot I_n + \left(u_{b2,1} - u_{b2,2}\right) \\ U_{s3} = \omega_k L_{31}\cdot I_1 + \omega_k M_{32}\cdot I_2 + \omega_k M_{33}\cdot I_3 + \ldots + \omega_k vM_{3n}\cdot I_n + \left(u_{b3,1} - u_{b3,2}\right) \\ \vdots \\ U_{sn} = \omega_k L_{n1}\cdot I_1 + \omega_k M_{n2}\cdot I_2 + \omega_k M_{n3}\cdot I_3 + \ldots + \omega_k M_{nn}\cdot I_n + \left(u_{bn,1} - u_{bn,2}\right) \end{cases}$$

L_{nn} is the inductance between the primary winding and secondary winding *n*.

M_{mn} is the mutual inductance between the secondary winding *m* and secondary winding *n*.

The calculation is done in the frequency domain. U_{sn} is the transformer n:th winding output voltage. Normally $U_{sn} = 0$ for all frequencies except the fundamental, but Ascalp can, if needed, also calculate the effects of harmonics in the supply line voltage.

$\left(U_{bn,1} - U_{bn,2}\right)$ is the line converter bridge voltage connected to bridge *n*.

Calculation of the line current

The phase currents I_1, I_2, I_3, I_4 etc are not all identical, mainly due to the interlaced modulation pattern for each bridge. The harmonic content and

especially the harmonic phase angle differs between the phase current in the different line converters. When adding all phase currents each phase's switching frequency will be cancelled and the current will have a resulting harmonic content with higher frequency and lower amplitude.

Calculation of the current from the line converter to the dc-link

When the modulation pattern is "one" the phase current is flowing through the upper IGBT (or GTO/diode), and when the modulation pattern is "zero", the current will flow through the lower IGBT. Thus the current through the component in the upper position, in the time domain, equals the modulation pattern times the phase current. This amount is the contribution from each phase current to the total current from the line converter to the dc-link. The current in the two phase connected to same bridge is equal but with opposite sign. *m* is the number of bridges connected to one dclink.

$$i_D(t) = \sum_{n=1}^{m} \left(s_{bn,1}(t) - s_{bn,2}(t) \right) \cdot i_n(t)$$

When the time domain functions are expressed as Fourier coefficients, the DC-link current will easily be transferred to the frequency domain. The time domain expression of the frequency domain phase currents and the frequency domain modulation pattern are for phase *n,1*:

The modulation pattern

$$s_{n,1}(t) = s_{n,1}a_0 + \sum_{k=1}^{\infty} s_{n,1}a_k \cdot \cos(k\omega_k t) + \sum_{k=1}^{\infty} s_{n,1}b_k \cdot \sin(k\omega_k t)$$

and the phase current

$$i_n(t) = i_n a_0 + \sum_{l=1}^{\infty} i_n a_l \cdot \cos(l\omega_l t) + \sum_{l=1}^{\infty} i_n b_l \cdot \sin(l\omega_l t)$$

By multiplying these two expressions we get the contribution from bridge n to the total current from the line converter to the dc-link

$$i_{Dn,1}(t) = s_{n,1}(t) \cdot i_{n,1}(t) = I_{n,1}a_0 \cdot S_{n,1}a_0 + I_{n,1}a_0 \cdot \sum_k \left(S_{n,1}a_k \cos\left(k\omega_k t\right) + S_{n,1}b_k \sin\left(k\omega_k t\right) \right) +$$

$$+ S_{n,1}a_0 \cdot \sum_l U_D a_l \left(\cos\left(l\omega_l t\right) + U_D b_l \sin\left(l\omega_l \omega t\right) \right) +$$

$$+ \sum_l \sum_k \frac{S_{n,1}a_k \cdot I_{n,1}a_l}{2} \left(\cos\left(\left(l\omega_l + k\omega_k \right) \cdot t \right) + \cos\left(\left(l\omega_l - k\omega_k \right) \cdot t \right) \right) +$$

$$+\sum_l\sum_k \frac{S_{n,1}a_k \cdot I_{n,1}b_l}{2}\left(\sin\left(\left(l\omega_l + k\omega_k\right)\cdot t\right) - \sin\left(\left(l\omega_l - k\omega_k\right)\cdot t\right)\right) +$$

$$+\sum_l\sum_k \frac{S_{n,1}b_k \cdot I_{n,1}a_l}{2}\left(\sin\left(\left(l\omega_l + k\omega_k\right)\cdot t\right) + \sin\left(\left(l\omega_l - k\omega_k\right)\cdot t\right)\right) +$$

$$+\sum_l\sum_k \frac{S_{n,1}b_k \cdot I_{n,1}b_l}{2}\left(\cos\left(\left(l\omega_l + k\omega_k\right)\cdot t\right) - \cos\left(\left(l\omega_l - k\omega_k\right)\cdot t\right)\right)$$

B.4 Calculations on the transformer

Converting the short circuit reactance matrix to the complex impedance matrix

The inductance matrix diagonal elements:

The short circuit reactance that is received, when the secondary winding *n* is short circuited and the primary winding voltage at rated current is measured:

$$X_{pn}$$

The diagonal element in the inductance matrix, L_{nn} is found by dividing the short circuit reactance by ω.

$$L_{nn} = \frac{X_{pn}}{\omega}$$

The inductance matrix non-diagonal elements:

The short circuit reactance that is received when the secondary winding *n* is short circuited and the voltage of secondary winding *m* is measured at rated current, is

$$X_{nn}\,.$$

The non diagonal element in the inductance matrix is ([17] page 369-370):

$$L_{nm} = \frac{X_{pn} + X_{pm} - X_{nm}}{2 \cdot \omega}$$

$$L_{mn} = L_{nm}$$

If the transformer resistance can not be neglected, the resistance matrix can be treated in the same way. The resistance matrix together with the inductance matrix forms the complex impedance matrix.

Calculation of the total inductance

The average transformer inductance, L_{tr}, is derived from the short circuit reactance, which is received when all secondary winding are connected in series and the terminal of the last secondary winding is connected back to the terminal of the first secondary winding, and the primary winding voltage at rated current is measured.

If this total short circuit reactance is not measured, it can be calculated by means of the short circuit reactance matrix elements:

$$L_{tr} = \frac{\sum_{n=1}^{n_s} X_{pn} + 2 \cdot \sum_{n=1}^{n_s-1} \sum_{m=n+1}^{n_s} \left(X_{pn} + X_{pm} - X_{nm} \right)}{n_s^{\,2} \cdot \omega}$$

where n_s is the number of transformer secondary windings.

C Appendix C. Drive system data

C.1 Data for the dead time compensation and the dc biased transducer compensation.

Transistorised voltage source three phase inverter

DC-link voltage	250 V
Switching frequency (synchronised with the sampling)	9.756 kHz
Dead time	0.5 μs

DSP Controller

Modulation	triangular wave carrier PWM
Sample time	102.5 μs

Motor (Δ-connected) ABB MT 100LA28-4, serial# MK110022-S

Nominal motor voltager	220 V
Nominal motor current	9 A
Nominal motor frequency	50 Hz
Nominal motor power	2.2 kW, cos(ϕ)= 0.76

C.2 Data for position asymmetry compensation.

Voltage source three phase inverter with GTO thyristors

DC-link voltage	1650 V
Maximum commutation frequency	400 Hz
Dead time	40 μs

Motor	**MJA350-2**
Nominal rating	420 kW
Nominal phase-to-phase voltage	1287 V
Nominal phase current	235 A
Nominal frequency	80.8 Hz

C.3 Data for calculation of harmonics generation due to asymmetries.

Voltage source three phase inverter with IGBT-transistors

DC-link voltage	750 V
Maximum commutation frequency	1 kHz
Dead time	5 μs

Motor	**MJA220-1**
Nominal rating	125 kW
Nominal phase-to-phase voltage	465 V
Nominal phase current	210 A
Nominal frequency	67 Hz

Appendix D. List of Symbols

Variables

u	voltage
i	current
p	power
y	voltage time area
ψ	flux linkage
R	resistance
L	inductance
C	capacitance
t	time
T	torque
J	inertia
k	gain
z	z-transform operator
f	frekvens
ϕ, θ, φ,γ,ξ	angle
ω	angular speed
s	general quantity, modulation signal
AP	search variable

Subscripts

s	stator
r	rotor
c	commutation frequency
α,β	stator oriented reference frame
d,q	flux oriented reference frame

x,y	general reference frame
error	error signal
offset	offset level
ϕ	phase angle
A	amplitude

Superscripts

*	reference value
α,β	stator oriented reference frame
d,q	flux oriented reference frame
x,y	general reference frame
-n	delay n samples in the z-transform

Other symbols

Arrow on top of symbol means vector