Evaluation of a DSP for power electronic applications

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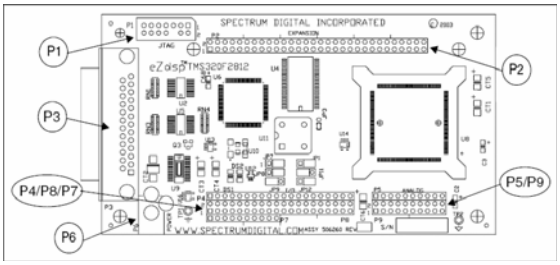
The complexity of the power grid increases with its continuous expansion and the addition of various software-controlled applications. These applications can be found in both loads and generators – as well as surveillance units. In most cases strict demands regarding performance and speed has to be fulfilled by the control scripts of these software applications.

To develop the control scripts, a user-friendly platform uniting a graphical user interface, host-target communication and C-debugging, with the performance demands, is of great interest. The prospect of the development platform being able to communicate with well-established software tools such as Simulink and MATLAB is even better.

A lot of solutions are available that facilitate the road from idea to working application, the eZdsp F2812 from Spectrum Digital is a system that seem to fit our needs very well and is thus worth a closer investigation.

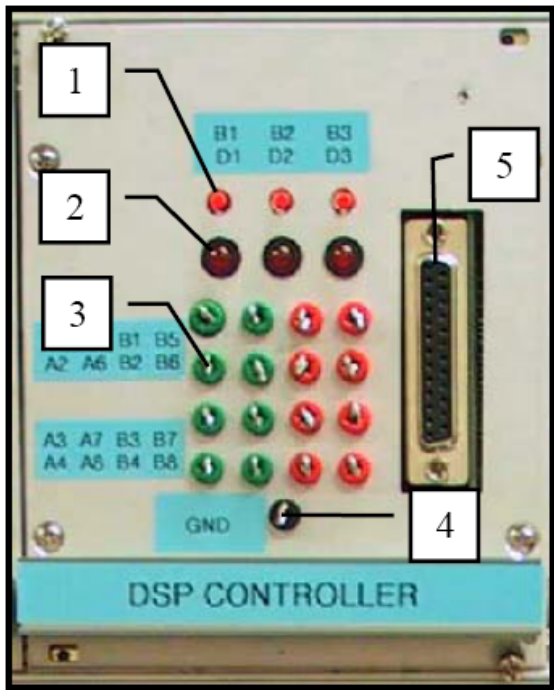
The obvious reasons for choosing the eZdsp is the price and versatile nature of the chip, should one like to mass produce a product – the DSP-chip from Texas Instruments is available at a cost that few other alternatives can hope to rival.



Schematic of the eZdsp F2812 board

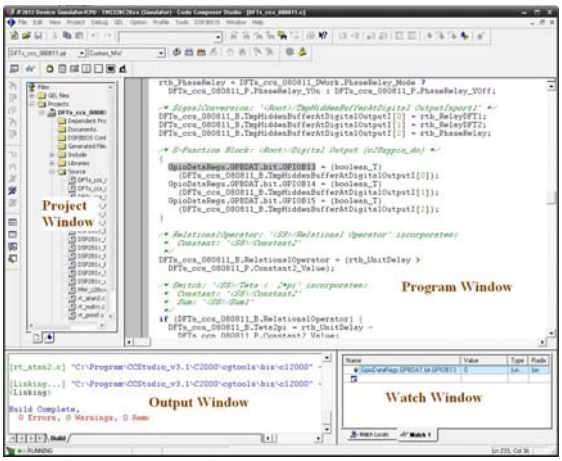
The DSP-chip comes from the TMS320F281x family of controllers and has a clock speed of 150 MHz. It comes equipped with 256 Kb – though this is expandable up to 1Mb. Furthermore, it has 16 analog inputs and 16 ports for pulse width modulated output. The signal levels are the systems main flaw – since they're configured to operate in the 0-3 V range – rather than the more common spectrum of 0-10 V.

The development board is encased in a metal frame together with an interface card constructed as part of a previous master thesis. The interface card emulates the signal levels of DSpace– and thus rectifies the problem mentioned earlier. This is of minor importance to this thesis however, since it is the capabilities and behaviour of the DSP that is of primary concern. Mounted on the front plate are three LEDs, three buttons and the 16 analog inputs mentioned earlier.



The front plate of the encased system

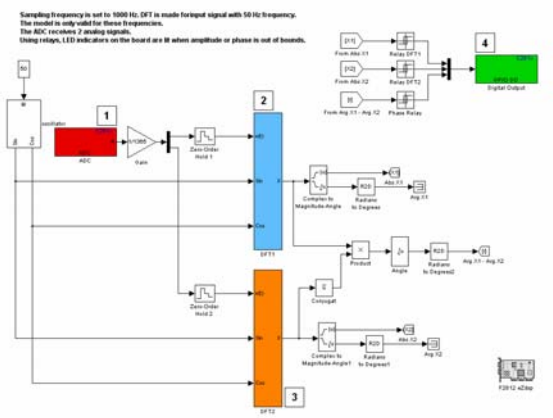
The eZdsp is shipped with Code Composer Studio (CCS), a suite of development tools to be used when creating, building and uploading programs to the DSP. Though CCS is great for conventional programming – this process is far more tedious and time-consuming than would be desired. Though thanks to the *Embedded IDE Link* and *Target Support* packages for MATLAB™ - the intuitive building-block based GUI of Simulink™ can be used to swiftly translate an idea to an automatically generated C-program uploaded to the DSP.



CCS v3.1 main interface

Digital relaying is a field of power electronics that has seen a constant increase since the 1980's. Therefore it is fitting to test the suitability of the DSP by implementing a simple digital relaying algorithm, using the chosen platform.

The model relies on DFT-algorithms for signal analysis, which is sufficient for detecting both phase anomalies and amplitude changes.

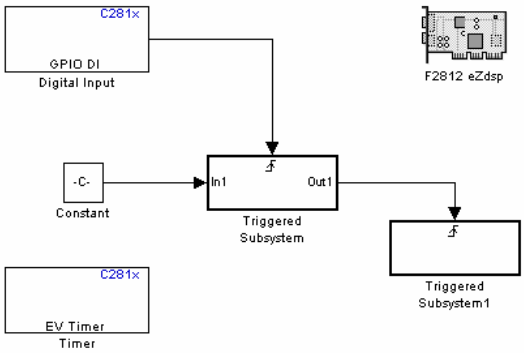


The model of the implemented relay

To be able to properly handle three-phase currents, a third DFT should be added – but since the really important question is if the software is capable, or not, of reproducing the model in functional C-code only two DFTs are displayed for improved clarity.

The model was built with no warnings or errors and was successfully uploaded to the DSP.

Considering that relays and circuit breakers demand short response times between the actual error and the moment when the signal has been analysed, a benchmark is of great interest.



The model used for benchmarking

To test the system performance the model above was implemented. A random number is run through a 1000th order FIR-filter and Timer values before and after the operation are compared, resulting in a

timer-difference of 540 steps. By examining the generated code the measured performance equals roughly 1.1 MFLOPS.

According to Texas Instruments, the DSP should be capable of 150 MMACS, Million Multiply Accumulate Cycles per Second.

In light of this, the measured performance of 1.1 MFLOPS seems a bit low, and the system should be able to perform a lot better. It should be noted that the 150 MMACS is a peak value and MMACS shouldn't be confused with MFLOPS. Also, it cannot be ruled out that a hardware interrupt interferes with the obtained value. Nonetheless should 1.1 MFLOPS be more than adequate for some power electronic applications which depend on a 50 Hz signal.

Overall, the platform performs very well – greatly reducing the time and effort needed to implement various applications. Thanks to the ingenious additions to MATLAB – any user familiar with building models in Simulink, may test and upload their ideas with little or no experience of C. To sum up, the platform should prove to be a valuable tool in exploring new areas in the field of power electronic applications.