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Industrial Electrical Engineering and Automation

Commissioning and Evaluation of an Inverter Prototype

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Abstract

This master thesis aims to commissioning and evaluate a construction of a DC/AC inverter. The purpose of the inverter is to run a fan motor in a military vehicle.

A plan of commissioning the inverter is described and accomplished. The individual parts in the inverter box were tested to assure correct behaviour. Necessary adjustments on the electronic layout were performed.

Simulations were made to study switching behaviour with different gate resistances and snubber circuit solutions. Simulations show that snubber circuits could be useful to reduce switching losses and voltage overshoot.

In the final part of the thesis measurements were accomplished. To understand how the output signal on the phases depends on the value of the gate resistances, measurements were done. Snubber circuits were constructed, evaluated and compared to the simulation results.

From the simulations and measurements it is clearly shown that the RCD clamp snubber circuit had a favourable affect on transients and oscillations and also the possibility to reduce the power losses in the IGBT module. An experience of importance is that laboratory work is very time consuming.

Keywords: Commissioning, Inverter, Power electronics, Snubber circuit.

Preface

This report is a result of our master thesis project carried out at BAE Systems Hägglunds in Örnsköldsvik with supervision of the department of Industrial Electrical Engineering and Automation (IEA) at Lund Institute of Technology.

We would like to thank the staff at IEA, our supervisors Per Karlsson and Gunnar Lindstedt and our examinator Mats Alaküla. Per, for his valuable ideas and guiding in the beginning of our project. Gunnar for his fast responses on all questions about our thesis. The busy man, Mats, who introduced this project for us. He has also given us time and inspiration when we really needed it.

The people that we have been in contact to more frequently are our supervisor Nils Lundström and our skilful mentor Stefan Englund at BAE systems Hägglunds. We really want to thank them because they have supported us in the problems that arose during the project and given us new angles of incidence. The environment at the office at Hägglunds have given us wellbeing and many laughs, thanks to our colleagues in Hulda. They have made our time in Örnsköldsvik marvellous with many baths and karaoke (thank you Bengan).

Finally we want to give a special thanks to Kalle Saarvanto for proofreading our thesis. We will of course also give our families the most hearty thanks for supporting and encouraging our studies through the years.

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Martin Gårdman, Andreas Johansson

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Abbreviations

AVR	A family of RISC microcontrollers from Atmel
BJT	Bipolar Junction Transistor
CPU	Central Processing Unit
CTR	Current Transfer Ratio
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
IGBT	Insulated Gate Bipolar Transistor
IO	Input Output
LED	Light Emitting Diode
LTH	Lund Institute of Technology
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PMSM	Permanent Magnetized Synchronous Machine
RCD	Resistance Capacitor Diode
RISC	Reduced Instruction Set Computer
SEP	Splitterskyddad Enhetsplattform or Modular Armoured Tactical System
SOA	Safe Operating Area

Chapter 1

Introduction

In a world where the interest for environmentally friendly, so called hybrid vehicles is growing the technology of power electronics is becoming an important part of vehicle construction. For future technologies for propulsion of vehicles, power electronics will play an important role when fuel cells and an increasing use of batteries will become reality. This technology will give the opportunity to reduce the need for fossil fuels and make countries less dependent of oil producing states.

1.1 Objective

This master thesis aims to commissioning and evaluate a construction of a DC/AC inverter. The function of the inverter is to supply a fan motor located in a newly developed armoured military vehicle called SEP. The fan motor is 3-phase Permanent magnetized synchronous machine (PMSM). Measurements and testing will be done on a prototype of the inverter which is not supposed to be in all considerations like the final construction. The temperature aspects in the material and in the ambient will for example not be considered. The most important aim of the thesis is to investigate how the power electronic devices act and cooperate. The outcome is to improve knowledge in the area of power electronics for the client, BAE Systems Hägglunds.

1.2 Background

SEP (Splitterskyddad Enhetsplattform or Modular Armoured Tactical System) is a newly developed armoured vehicle by BAE Systems Hägglunds and Sweden's defence material administration. The vehicle is based on a modular concept where it will meet demand for different purposes such as troop transport, working as a radar station or as a weapon equipped tank. One of the advanced feature of SEP is the electrical drive [8]. Instead of conventional mechanical

propulsion an electrical motor is integrated in each wheel, or in the front in the rubber band version. Electrical propulsion has many advantages such as less weight and volume and a more flexible manoeuvring of each wheel independently.

SEP is designed to easy implement future technologies like fuel cell or battery drive, electrical weapons and remote controlling.

In the first generation of the vehicle two diesel engines will provide energy to a generator transforming it to 700V on a DC bus. The DC bus provides enough energy for both propulsion and the auxiliary equipment. The now existing prototypes are, to a large extent, equipped with hydraulic systems for energy conversion. It is desirable to replace the hydraulic system with an electrical one. As a part of the development this master thesis will evaluate a prototype of an inverter for the cooling fan motor.

1.3 Problems

The most critical problem to solve is how to design and tune the power electronic components in the inverter to cooperate in the best manner possible. How can voltage transients, oscillations and losses be reduced to a minimum? Could this be done with help of snubber circuits?

1.4 Research method

- Literature study
- Commissioning the equipment
- Resolve and correct the problems that arise
- Simulation in Pspice on the power electronic devices
- Perform measurements and adjustments on different parameters
- Evaluate different snubber circuit solutions
- Present future improvements

1.5 Delimitations

The thesis will not cover the areas of the cooling aspects or the packing layout in the inverter box. Neither programming the control circuit will be covered. The EMC (Electromagnetic Compatibility) and EMI (Electromagnetic Interference) affects are not within this master thesis extent.

1.6 Structure of the report

The report is divided into eight chapters. Below is a short description of each chapter.

1 Introduction -

2 Theory - The most important components in the hardware are discussed. That includes IGBT module, the driver circuit and snubber circuits. Also how the losses occur and how it can be minimized is discussed as well as protection features.

3 Hardware description - In this chapter the hardware in the prototype will be described in more detail. Explanations why the components in the prototype were chosen and what to think about when choosing components are discussed.

4 Evaluation of hardware - During the commissioning part many problems arose. The problems are described in this chapter and the actions that were taken to correct them are explained.

5 Simulations - Describes what kinds of simulations are done and their results.

6 Test results - The measurements of the inverter and the results of these are presented. The different switching behaviour with and without snubber circuits are visualized and explained.

7 Improvements of the construction and future work - The chapter treats the improvements that have to be done in considerations to component selection and their cooperation. The problems that arose during the commissioning and suggestions how to avoid them will be explained.

8 Conclusions - Presents the conclusion of the work and answers the questions asked in the problems section.

Chapter 2

Theory

2.1 IGBT

IGBTs were first introduced as a combination of the bipolar junction transistor (BJT) and the metal oxide semiconductor field effect transistor (MOSFET) technology. The IGBT is to prefer in medium high voltage segments (600-3000V) rather than the MOSFET because it proved to have several good features like ruggedness and operation at higher frequencies [1, ch. 1.9]. The construction of the IGBT combines the low conduction losses of a BJT with the advantage of the short switching times of the MOSFET.

An IGBT can be simplified as in Figure 2.1, were C_{GE} and C_{GC} symbolises stray capacitances. When dimensioning the driver circuit stray capacitances could be a good starting point [3]. But there are different opinions whether this is the best way to design it. The reason for this is that the values of the capacitances are non-linear and vary depending on the voltage across them. Typical values of the stray capacitances are often presented in the data sheets of the component but the most accurate values can be read in the graph of how the capacitances vary. A graph of this type is also often found in the data sheets [7]. The value of C_{GC} has the largest change and decreases with increasing voltage. Another and probably better way to calculate the gate circuit properties is to use the gate charge specifications available in data sheets [2]. This will be discussed more in section 2.2.2.

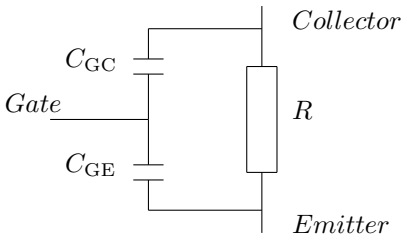

Figure 2.1: Internal stray capacitances in the IGBT.

The understanding of the switching procedure of an IGBT requires a more detailed description. It is very similar to a MOSFET. The main difference occurs at turn-off when a current tail appears, see Figure 2.2 [5]. When turning on, a positive voltage is applied on the gate circuit (V_{GE}), which results in a constant current on the gate (I_{G}), see Figure 2.3. When the gate voltage increases above the threshold (V_{GEth}), a current will start to flow from the collector to the emitter (I_{D}), with a derivative of di/dt. The value of the current derivative is determined by the semiconductor structure and the external circuit [3, p.22]. The gate current will mainly charge the gate-emitter capacitance (C_{GE}), seen as the first voltage rise (V_{GE}) in Figure 2.3.

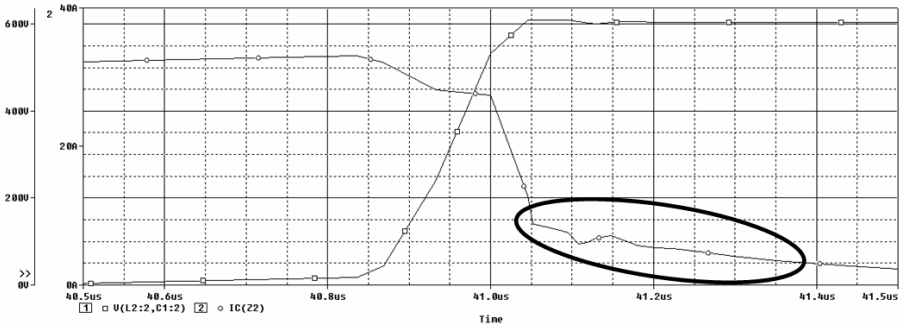

Figure 2.2: The encircled part of the graph shows the current tail that occurs at turn-off.

When the gate-emitter capacitance is fully charged the collector current I_{D} has reached the same value as the external circuit. The gate-emitter voltage, (V_{GE}), will then remain constant because no current changes will now occur. The gate-collector capacitance (C_{GC}) will at this time begin the same procedure as C_{GE} and get charged of the gate current. During this phase the so called Miller plateau occurs, the flat part in Figure 2.3. The collector-emitter voltage is turning to its minimum at this point. When C_{GE}, also called the Miller capacitance, is fully charged the gate-emitter voltage increases to the voltage of control. The minimum charge for turning the semiconductor on occurs when the Miller capacitance is saturated. The Miller's effect influences the switching speed at turn-on among others. This affects losses and electromagnetic interference, EMI.

At turn-off, the gate voltage turns to zero. The stray capacitances C_{GE} and C_{CE} are discharging until the Miller plateau is reached. At this time the collector voltage starts to rise until it reaches the bus voltage. At the Miller plateau the charge of C_{GE} is not affected, only the C_{GC} capacitance is changing its charge. The gate-emitter voltage continues to fall exponentially and when it is below the threshold the IGBT can be considered as turned off. As a consequence of the bipolar part of the IGBT a current tail appears at turn-off, see Figure 2.2. The current tail is unwanted because it increases losses, but it is hard to affect and today impossible to eliminate.

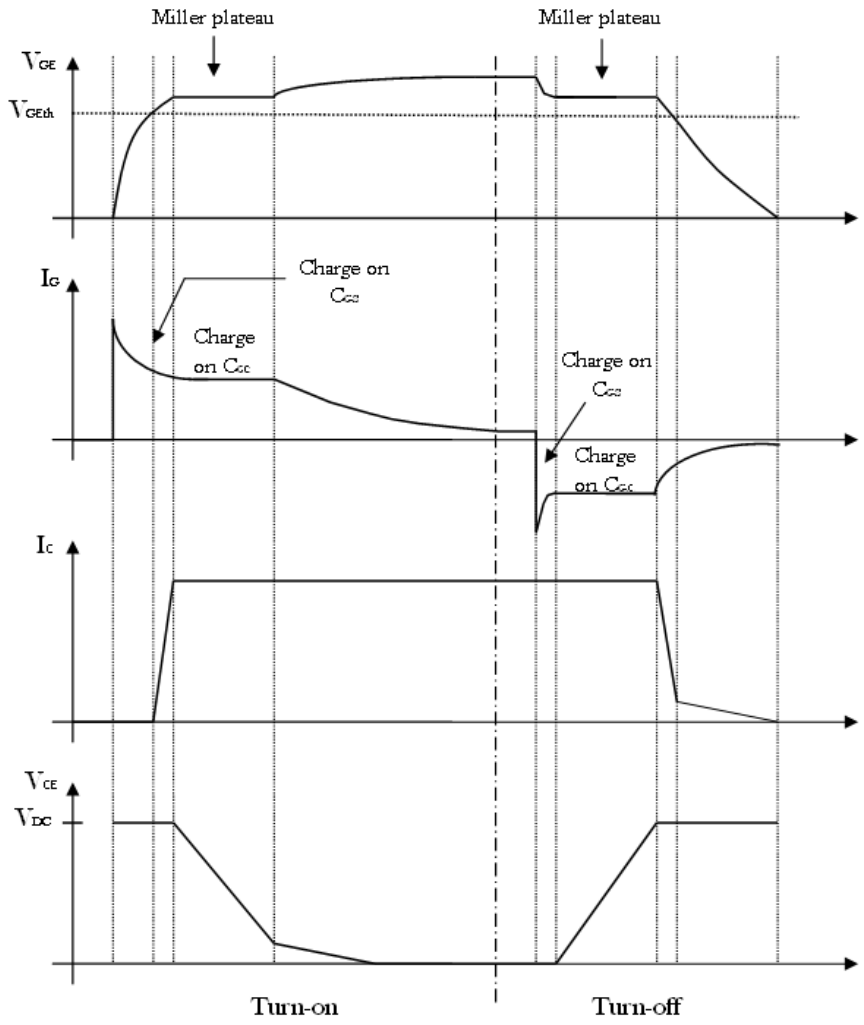

Figure 2.3: Voltage and current behaviour in an IGBT circuit.

2.1.1 Reverse recovery

One important factor to take into account when designing an inverter is the current contribution of the diode reverse recovery. This phenomenon occurs due to the free wheeling diode together with an inductive clamped load. When the diode is in blocking mode, charge is fed into the diode. At turn-on the current is switched to the opposite direction and the diode will contribute to the load current with an additional current. The contribution has the effect of generating an overshoot of the load current which could generate oscillation on the DC bus and in the worst case cause damage to the IGBT. The large current spike increases the switching losses and is therefore very important to damp as much as possible [4].

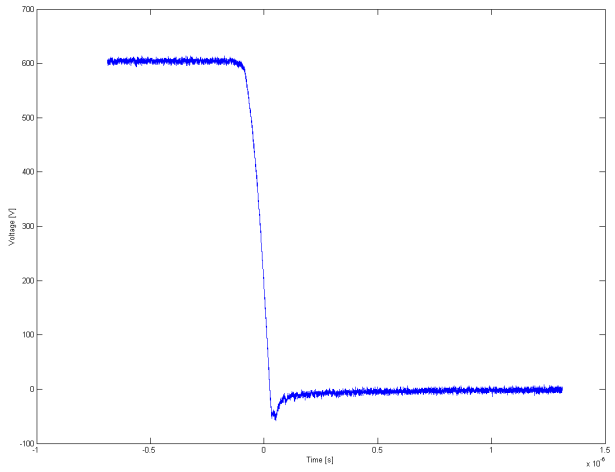

Figure 2.4: The dip at turn-on is a phenomenon of reverse recovery.

2.2 Gate driver

Basically a gate driver consists of a voltage supply, an amplifier and a gate resistor, see Figure 2.5. The main task of a gate driver is to provide the gate of the IGBT with enough current to conduct. The size of the current is depending on the gate resistance and mainly the required threshold voltage across the gate-emitter. The voltage range is specified in the data sheets for an IGBT, usually between 10V to 20V. Voltage controlled switches such as MOSFET and IGBT have a capacitive input which makes the requirements of current handling quite small, even logic gates are often enough to provide the necessary current [6, p.89].

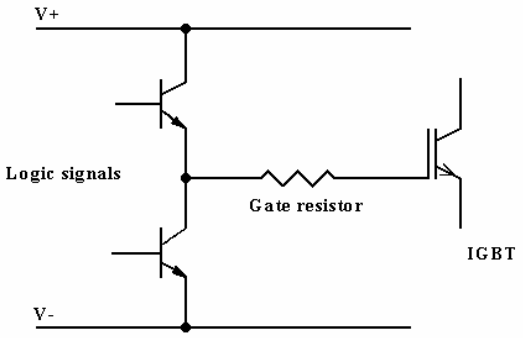

Figure 2.5: Simple model of a gate driver circuit.

The design of the driver depends on its purpose of use. Many commercial drivers have some protection features by measuring among others di/dt and dv/dt and if the value is too high it turns off the device. Large voltage transients and large

current peaks have to be reduced for preventing short circuiting and damage on the power module.

2.2.1 Gate Resistance

The gate resistor is utilized both at turn-on and turn-off. The simplest circuits use just one passive resistor for both operations. More complex gate circuits imply one resistor for each operation. The latter can be a good solution when efforts are made to optimize both turn-on and turn-off characteristics. To choose a proper value is a trade off. Advantages of a smaller value of the gate resistor are to improve current derivative (di/dt), limit switching losses in the IGBT and to avoid cross conduction. Cross conduction implies that two transistors on the same inverter leg are turned on and cause a short circuit [3, p.29]. Switching losses are reduced because a smaller value makes the transition change faster i.e. the period when both the current and voltage are at a high level is minimized. The drawbacks with a faster transition change are high voltage transients and oscillations on the DC bus as well as increased EMI contributions. A larger value of the gate resistance limits voltage transients and reduces the oscillation together with a limitation of diode recovery voltage [3, p.30].

2.2.2 Power requirements

For further design of the gate driver the power level control signal has to be defined. The necessary power is a function of total gate charge (Q_{G}), bias control voltage ($V_{\mathrm{G+}}$ and $V_{\mathrm{G\text{-}}}$) and operating frequency (f_{sw}). The average gate power can be determined by the equations below [9].

$$I_{\mathrm{s}} = Q_{\mathrm{G}} \cdot f_{\mathrm{sw}} \tag{2.1}$$

$$P = I_{\mathrm{s}} \cdot (V_{\mathrm{G+}} - V_{\mathrm{G\text{-}}}) \tag{2.2}$$

The total gate charge can be found in the data sheets for the IGBT, as mentioned in the previous section. The required peak gate current is defined as follows:

$$I_{\mathrm{Gon}} = \frac{(V_{\mathrm{G+}} - V_{\mathrm{G\text{-}}})}{R_{\mathrm{Gon}}} \tag{2.3}$$

$$I_{\mathrm{Goff}} = \frac{(V_{\mathrm{G+}} - V_{\mathrm{G\text{-}}})}{R_{\mathrm{Goff}}} \tag{2.4}$$

In equations (2.3-2.4) a system with different gate resistances for turn-on and turn-off is shown. Most common is that these are the same ($R_{\mathrm{Gon}} = R_{\mathrm{Goff}}$).

2.3 Opto coupler

An opto coupler consists of a infrared light-emitting diode (LED), a photo diode and a transistor, see Figure 2.6. The opto coupler is used to divide different levels of potentials with respect to the ground level. The difference in potential between the input and the output could in power electronic applications be hundreds of volts.

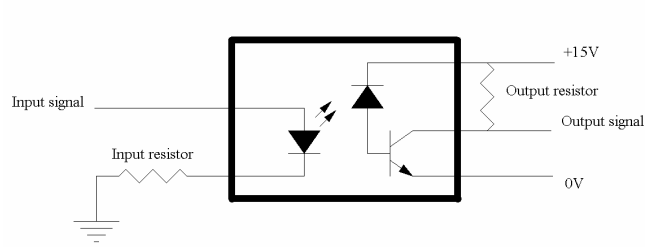

Figure 2.6: A schematic sketch of the location of the resistor pair due to the opto coupler.

The input signal in combination with the input resistance contribute to a current in the LED. The light emitted from the diode is received by the photo diode connected to the base of the transistor which starts to conduct and transfer the signal. Note that the output signal is inverted in the connection shown in Figure 2.6.

When opto couplers are used in power electronic applications the delay time is an important factor. For this reason a fast transfer from the input to the output is essential. Since the transfered signal usually is a square wave pulse, fast rise and fall times are important. It is important to know that an opto coupler introduce a delay time to the system.

The input capacitance of the LED needs to be charged before it starts to emit light. An input current as close to the rated maximum current as possible is for this reason wanted if fast transitions are required. To determine the input current an input resistance is used. On the output the capacitance of the photo diode and the transistor contribute to a delay in the circuit [15].

The coupling efficiency, also called current transfer ratio, (CTR) is defined as the output current divided by the input current. A low CTR has the tendency to deteriorate the signal. To not consume more current than necessary the CTR can be in the lower region of the allowed level. The CTR is found in the data sheets of the component. A high output current reduces the delay time in the opto coupler. A trade of between delay time, current and power consumption has to be made from case to case [16].

2.4 Snubber circuits

A transistor has to work in the safe operating area (SOA) not to get damaged, see Figure 2.7. During turn-on and turn-off, the transient effects can make the transistor work outside the SOA. This has to be avoided and is strongly dependent upon the energy stored in stray inductance of the circuit but also upon the IGBT switching performance as di/dt and dv/dt. The size of the switching voltage transient is proportional to the stray inductance but also to the current that occurs during turn-off. To minimize the stray inductance in a circuit a good layout is of big importance. It is desirable not to use snubber circuits if not necessary because of economic reasons and volume aspects, but sometimes it is necessary. Before introducing snubber circuits the stray inductance has to be optimized to get satisfying performance.

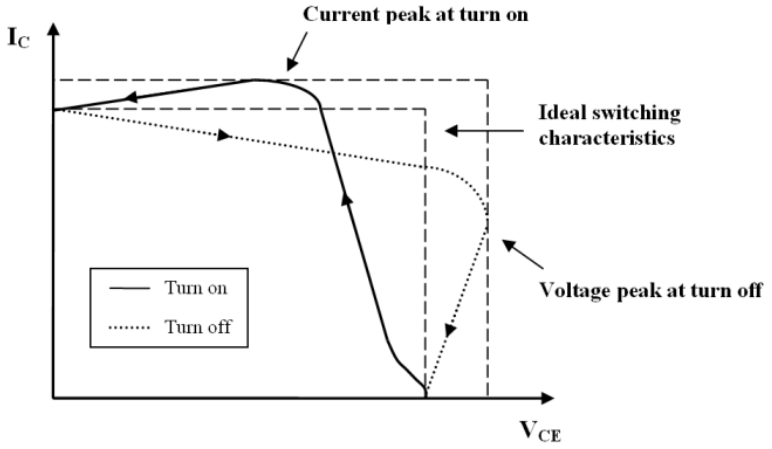

Figure 2.7: Switching characteristics at turn-on and turn-off.

To reduce the derivative of the current and the voltage, the value of the gate resistor can be increased to slow down the switching. This has other side effects like increased switching losses. Therefore a trade off is, as always, important.

The DC bus is one of the main sources of stray inductance, but the connections between all components are also contributing. The best way is to use IGBT modules instead of separate transistors because the stray inductance is minimized when all connections are inside a module. A common value of the stray inductance in a module is 10-20nH [3, p.31]. Figure 2.8 shows a schematic layout of an IGBT module.

The most common solution to the problem with stray inductance is to use a decoupling capacitor across the entire inverter leg providing a non inductive path for current transition [11]. To further decrease the inductance these capacitors should be mounted directly to the terminals of the IGBT module.

Introducing a snubber circuit could be a good solution, but not always. For an IGBT, which has capacitive input, a turn-on snubber circuit is seldom needed [7]. A turn-on snubber circuit could be used to limit the di/dt at turn-on and protect

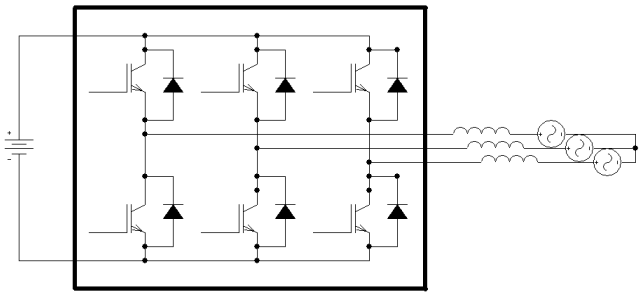

Figure 2.8: The squared part shows an IGBT module including six transistors.

components from hazardous voltage. Snubber circuits at turn-off are sometimes useful. The turn-off snubber circuit would be used mainly for limiting the voltage overshoot and to minimize the resonance. Another advantage with a turn-off snubber circuit could be to reduce the temperature in the semiconductor. A snubber circuit with a proper design will decrease the switching losses and also remove the losses to passive components in the snubber circuit, which are able to work during higher temperatures than an active switch.

2.4.1 Component selection

When selecting components, stray inductance is of big importance. As discussed before, modules are preferred. Special snubber capacitors managing high voltage derivative and large currents are available for this purpose. Direct mounted snubber capacitors with integrated snubber diode for RCD snubber solutions are available on the market [10]. A snubber resistor made of carbon composite or metal film is a common choice for minimizing the stray inductance [3, p.167]. The snubber diode experiences high peak current, but it is low in average. The rated voltage in the diode has to have the same value as the snubber capacitor. The blocking action of snubber diodes has to be faster than the transistor to contribute with protective functionality.

2.4.2 Decoupling capacitor

A common choice when introducing a snubber in an IGBT application is decoupling capacitor connected directly to the IGBT module. The intention with the decoupling capacitor is to take care of harmful voltage transients.

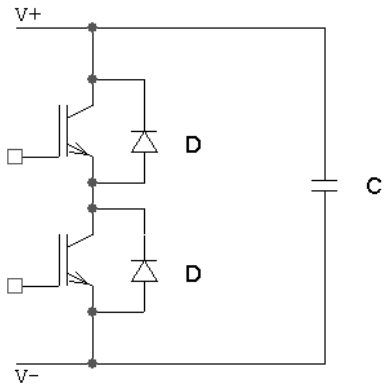

Figure 2.9: Schematic layout of a decoupling capacitor.

2.4.3 RCD snubber circuits

There are three main versions of RCD snubber circuits for high current applications, discharge restricted decoupling capacitor, the clamp snubber circuit and the snubber circuit for charge and discharge, see Figures (2.10-2.12). The circuits have characteristics of reducing transients across the switching device while the purpose of the charge discharge version also is to reduce the turn-off losses of the IGBT. The difference between the three types can simply be described that the RCD clamp and the discharge restricted decoupling capacitor are activated first when a voltage overshoot occurs. The charge discharge RCD is active the entire time and smooths the last part of the voltage rise at turn-off. To get a better understanding see the plots in section 5.3.

Discharge restricted decoupling capacitor

A discharged restricted decoupling capacitor operates in the same way as the ordinary decoupling capacitor but is restricted to operate only at turn-off. As the IGBT is turned off the energy trapped in stray inductance in the DC loop is transferred to the capacitor. In this phase oscillations easily occur. To prevent this behaviour a diode in parallel with a resistor is introduced to block the current in one direction and damp any oscillations. The disadvantage with this type of circuit is an additional source of stray inductance which increases the voltage overshoot.

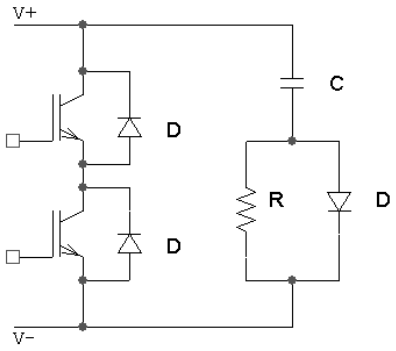

Figure 2.10: Schematic layout of a discharged restricted decoupling capacitor.

RCD clamp

The behaviour during turn-on and turn-off is described separately below.

Turn-off: During the time when the IGBT is conducting the snubber capacitors are charged to the bus voltage. When the IGBT is turned off the voltage across the terminals will rise rapidly. If the voltage rises above the bus voltage the snubber is activated. The energy trapped in is now moved to the snubber capacitor which absorbs this energy. The energy is at turn-on then discharged in the snubber resistor.

Turn-on: As the collector current raise a voltage drop affected by $L_\mathrm{s} \cdot di/dt$ causes the voltage over the terminals to drop by the same amount. The charged snubber capacitor now discharges through the forward biased free wheeling diode, the IGBT and the snubber capacitors. This has a favourable effect on the reverse recovery voltage transient.

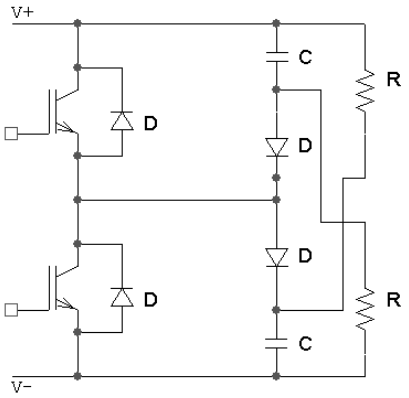

Figure 2.11: Schematic layout of an RCD clamp snubber circuit.

Charge discharge RCD

The reason for introducing a charge discharge snubber is mainly to reduce power dissipation in the IGBT at turn-off by slowing down the rate of rise of voltage across the IGBT. The intention is to make the snubber capacitor fully discharged when the IGBT is turned on and fully charged at turn-off. This circuit reduces the rate of voltage rise across the IGBT. The disadvantage with this snubber circuit is large power losses in the snubber components.

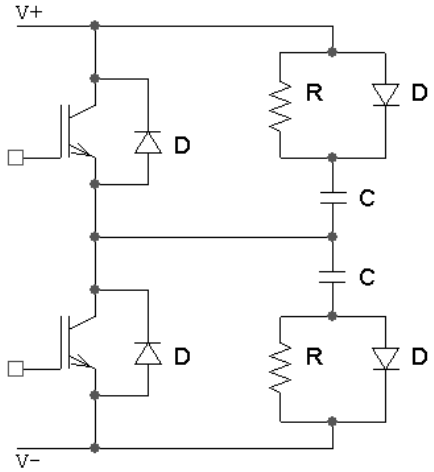

Figure 2.12: Schematic layout of an RCD snubber circuit for charge and discharge.

2.5 Losses

The instantaneous switching losses can be calculated by multiplication of the instantaneous voltage across the transistor (V_{DS}) and the instantaneous current through the transistor (I_{D}). The total amount of losses can be separated into two different parts, conduction losses and switching losses.

The thermal characteristics of the inverter are very important to assure a proper function. For this reason it is essential to be able to do an estimation of the losses. These calculations are not always straight forward and can be further complicated when snubber circuits, that change the switching characteristics, are implemented. For this reason it is of importance to notice that the method for estimation of losses presented in this section assumes a theoretical switching behaviour and does not take the reverse recovery current into account. The reverse recovery behaviour was discussed in section 2.1.1. More precise calculations and methods can be found in the literature[7].

In Figure 2.13 a simplified switching behaviour during one period can be seen. The dotted area symbolises the switching losses and the grey shows the conduction losses during the switching process.

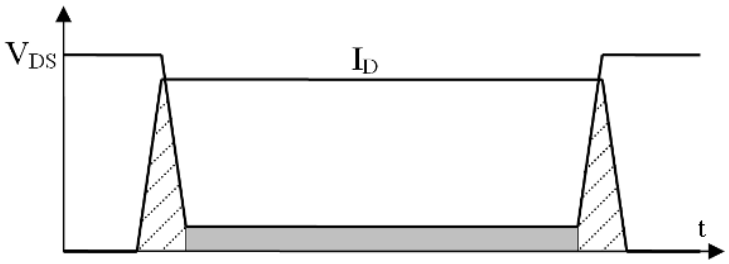

Figure 2.13: Simplified sketch of switching behaviour at turn-on and turn-off.

The instantaneous values of voltage and current are multiplied to get a value of the power loss instantaneously, see equation (2.5) [6].

$$p_{\mathrm{s}}(t) = v_{\mathrm{s}}(t) \cdot i_{\mathrm{s}}(t) \tag{2.5}$$

The instantaneous values are integrated for one switching period (T_{sw}) which gives the total energy loss during one switching period. The switching period is divided into three parts; turn-on (on), conduction (cond) and turn-off (off). The parameter D_{s} is the duty cycle for the component (2.6-2.9).

$$E_{\mathrm{s}}(T_{\mathrm{sw}}) = \int_{T_{\mathrm{sw}}} p_{\mathrm{S}}(\tau)d\tau = E_{\mathrm{S,on}}(T_{\mathrm{sw}}) + E_{\mathrm{S,cond}}(T_{\mathrm{sw}}) + E_{\mathrm{S,off}}(T_{\mathrm{sw}}) \tag{2.6}$$

$$E_{\mathrm{s,on}}(T_{\mathrm{sw}}) = \int_{t_{\mathrm{on}}} p_{\mathrm{S}}(\tau)d\tau = V_{\mathrm{DC}} \cdot I_0 \cdot \frac{t_{\mathrm{on}}}{2} \tag{2.7}$$

$$E_{\mathrm{s,cond}}(T_{\mathrm{sw}}) = \int_{t_{\mathrm{cond}}} p_{\mathrm{S}}(\tau)d\tau = V_{\mathrm{DC}} \cdot I_0 \cdot t_{\mathrm{cond}} \tag{2.8}$$

$$E_{\mathrm{s,off}}(T_{\mathrm{sw}}) = \int_{t_{\mathrm{off}}} p_{\mathrm{S}}(\tau)d\tau = V_{\mathrm{DC}} \cdot I_0 \cdot \frac{t_{\mathrm{off}}}{2} \tag{2.9}$$

The next step is to divide the energy loss with the switching period to get the power losses, see equation (2.10-2.13)[6].

$$P_{\mathrm{S}}(T_{\mathrm{sw}}) = \frac{E_{\mathrm{S}}(T_{\mathrm{sw}})}{(T_{\mathrm{sw}})} = P_{\mathrm{S,on}}(T_{\mathrm{sw}}) + P_{\mathrm{S,cond}}(T_{\mathrm{sw}}) + P_{\mathrm{S,off}}(T_{\mathrm{sw}}) \tag{2.10}$$

$$P_{\mathrm{S,on}}(T_{\mathrm{sw}}) = \frac{E_{\mathrm{S,on}}(T_{\mathrm{sw}})}{(T_{\mathrm{sw}})} = E_{\mathrm{S,on}}(T_{\mathrm{sw}}) \cdot f_{\mathrm{sw}} = \frac{V_{\mathrm{DC}} \cdot I_0 \cdot t_{\mathrm{on}}}{2} \cdot f_{\mathrm{sw}} \tag{2.11}$$

$$P_{\mathrm{S,cond}}(T_{\mathrm{sw}}) = \frac{E_{\mathrm{S,cond}}(T_{\mathrm{sw}})}{(T_{\mathrm{sw}})} = V_{\mathrm{S(on)}} \cdot I_0 \cdot \frac{t_{\mathrm{cond}}}{T_{\mathrm{sw}}} = V_{\mathrm{S(on)}} \cdot I_0 \cdot D_{\mathrm{S}} \tag{2.12}$$

$$P_{\mathrm{S,off}}(T_{\mathrm{sw}}) = \frac{E_{\mathrm{S,off}}(T_{\mathrm{sw}})}{(T_{\mathrm{sw}})} = E_{\mathrm{S,off}}(T_{\mathrm{sw}}) \cdot f_{\mathrm{sw}} = \frac{V_{\mathrm{DC}} \cdot I_0 \cdot t_{\mathrm{off}}}{2} \cdot f_{\mathrm{sw}} \tag{2.13}$$

To perform the calculations above, the rise and fall time (t_{on}, t_{off}) are needed. These parameters are supplier dependent but are not always presented in the

data sheets of the component. On the other hand, the turn-on and turn-off energies, E_{on} and E_{off} are usually presented, also these parameters differ between different suppliers and different components. If these energies are presented, equation (2.14-2.15) can be used to estimate the switching losses. Low values of the rise and fall times and also of the energies are very important to keep the switching losses at a low level.

$$E_{\text{s,on}}(T_{\text{sw}}) = \frac{E_{\text{on,0}}}{V_{\text{DC,n}} \cdot I_{\text{0,n}}} \cdot V_{\text{DC}} \cdot I_0 \tag{2.14}$$

$$E_{\text{s,off}}(T_{\text{sw}}) = \frac{E_{\text{off,0}}}{V_{\text{DC,n}} \cdot I_{\text{0,n}}} \cdot V_{\text{DC}} \cdot I_0 \tag{2.15}$$

2.6 Disturbances

In a compact design it is likely that conductors disturb the surrounding equipment. It is therefore of great importance to know about the phenomenon and to have the knowledge how to reduce it. The following section shortly describes two different types of disturbances [14].

Inductive disturbances
A voltage measurement is affected by the electromagnetic field in the surroundings. The disturbance level depends on the area of the loop of the cables that are affected of the disturbance, see Figure 2.14. If the cables are twisted the area of the loop is minimized, resulting in much less disturbance. This is the easiest way to reduce it. Providing a shield connected to ground could be a solution but an ordinary cable shield is not enough. To eliminate the magnetic field a thick and heavy one is required.

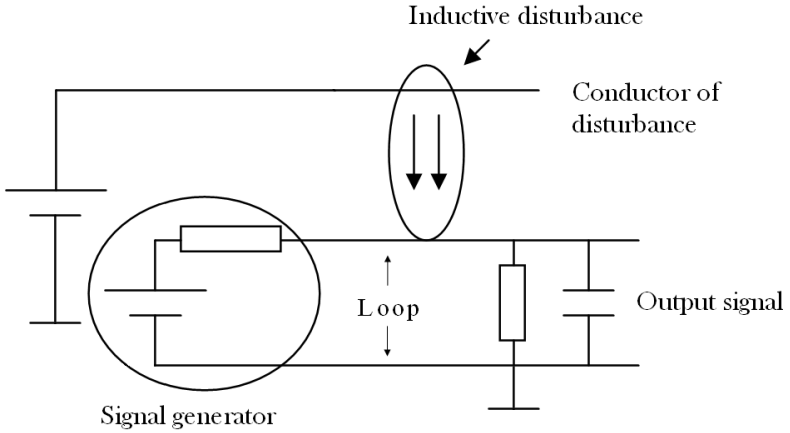

Figure 2.14: Schematic view of inductive disturbance.

Capacitive disturbances
A signal with a current output is not affected of the electromagnetic field, because no loop is present. Instead capacitive disturbance is a problem. These

originate from capacitive coupling from a near by conductor. The Figure 2.15 shows the capacitance of interest and the current originated from the capacitive disturbance.

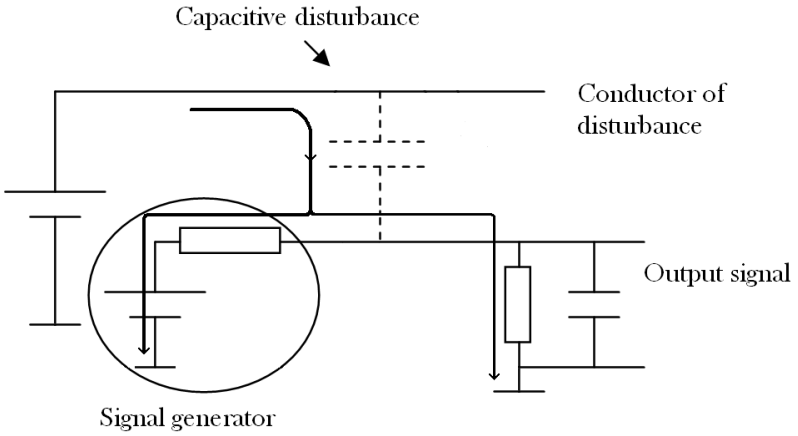

Figure 2.15: Schematic view of capacitive disturbance.

The unwanted current at the measurement point is depending on the resistance in the signal generator. A low ohmic resistance in the signal generator makes the current to pass through it rather than to through the measuring instrument.

To avoid the disturbances the most effective way is to shield the cables and connect the shield to a low ohmic ground. The current of disturbance will be conducted through the shield to ground without affecting the measuring signal. In practise this could be a problem when for example contacts could be hard to shield. Capacitive disturbance increases with increasing frequency because the impedance in the stray capacitance decreases, resulting in a larger current.

Chapter 3

Hardware description

3.1 Overview of system

The main components of the overarching system are shown in Figure 3.1. It consists of the interface box where the maneuvering of pulse lengths, blanking time and activation of the pulses are done. The interface box does also contain outputs for measurements of currents and voltages. The outputs are connected to the inverter box. In the standard setup there are three multimeters connected to the outputs of the interface box, this for measuring the DC bus positive and negative voltage and the mid potential. Indication light for ground fault is also implemented. The inverter box contains the prototype of an inverter, this will be further discussed in section 3.2.

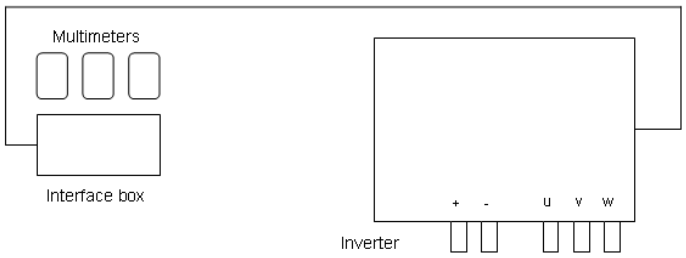

Figure 3.1: Overarching layout of the system.

3.1.1 Interface

To have total control of the testing, an interface for inputs and outputs of the inverter was designed, see Figure 3.2. The interface was made flexible to be able to use it through the entire testing process. It consists of several points of

measurements for instance to measure current on the input and on the phases. Diodes to detect ground fault or capacitor fault are also implemented. The interface has a thumb wheel switch and a button to control and activate the program on the control circuit card. The potentiometer can be used for many different purposes, for example to change pulse length or to change switching frequency depending on implemented program. The voltage pointing indicator is used for supervision of the DC voltage.

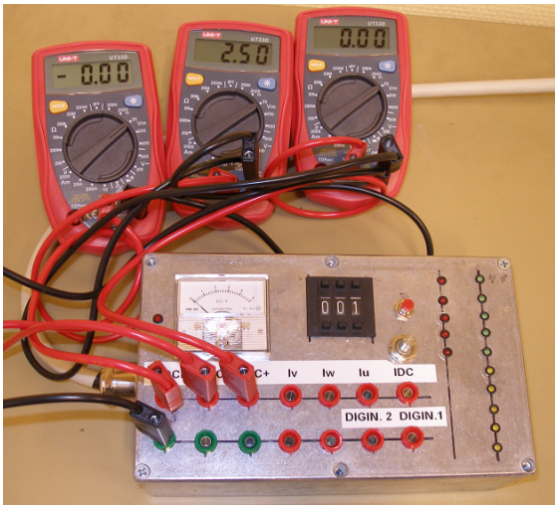

Figure 3.2: The interface box.

3.2 Overview of the inverter

The inverter box contains all power electronics, and logics. The main components seen in Figures 3.3-3.5 are listed and described below.

1. Liquid cooling plate.
2. IGBT module, Mitsubishi Electric CM50TL-24NF.
3. Current transducer, LEM HAL50.
4. DC bus capacitors, RIFA 2200μF 450V.
5. Voltage supply, Traco power 800mA $\pm$15V .
6. DC bus (Two Copper plates with plastic isolation layer in between).
7. Resistors, 27kΩ.
8. Control circuit card.
9. Driver circuit card (underneath the control circuit card).

Figure 3.3: Layout of the inverter box.

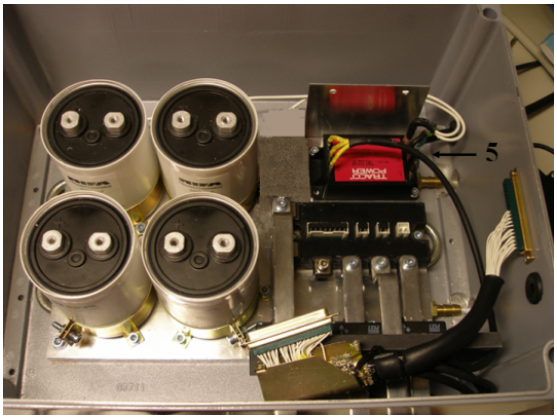

Figure 3.4: Layout of the inverter box.

Figure 3.5: Layout of the inverter box.

The components in the inverter box are mounted on a liquid cooling plate. The cooling plate is not in use during the commissioning process because no long

switching periods are activated. In operation mode the inverter is dependent on a cooling plate because of high temperature.

The IGBT module chosen is a 1200V, 50A full bridge module (six transistors) with a rise time of 50ns and a fall time of 300ns. This prototype of the inverter is not designed for a power larger than 10kW, which gives a safety margin not to overload the components.

To be able to control the torque when the inverter is running an electric machine control of the current is necessary. For this reason three current transducers are implemented, one for measuring the current consumed from the DC bus and two for measuring the current in the different phases. For economic reasons and volume aspects the current in the third phase is calculated by the CPU, implemented on the control circuit card, see section 3.2.1. As the sum of the currents in a three phase system equals to zero the calculations are done by the information from the two other transducers. It is important to notice that it is not possible to use the transducers for fault detection, like a short circuit. That is because the current in the third phase are calculated and is not measured.

It is of great importance to keep the DC voltage level stable so the rest of the system is not influenced when consuming power from the DC source. For this reason large DC bus capacitors are needed. The capacitors used in the inverter box are rated for up to 450V and connected in series not to exceed the allowed voltage level.

The Hall transducers, the control circuit card (section 3.2.1) and the driver circuit card (section 3.2.2) require voltage supply. A Traco power DC/DC 800mA voltage supply is implemented, enough to supply all unities in the inverter box.

For low inductive supply of DC voltage a DC bus of two copper plates is used. To reduce the capacitance of the DC bus the copper plates are mounted close together. To assure that a short circuit between the plates does not occur an isolating layer between the plates is necessary, see section 4.1.1. Stray inductance is minimized by tinning the electric connection areas of the copper plates.

Four resistances are mounted across the DC bus capacitors, from the positive and the negative side of the DC bus to the mid potential respectively. The functions of these are to stabilize the DC potential and also to assure that the DC capacitors are discharged when the inverter is turned off.

3.2.1 Control circuit card

1. Input resistances to opto coupler, 180Ω (the opto couplers are located on the driver circuit card).
2. Voltage dividers for measuring the DC bus voltage.
3. Micro processor, ATMEGA8 AVR, ATMEL.

The functions of the inverter are controlled by a microprocessor called ATMEGA8, a RISC processor with 8kb of integrated program memory from the

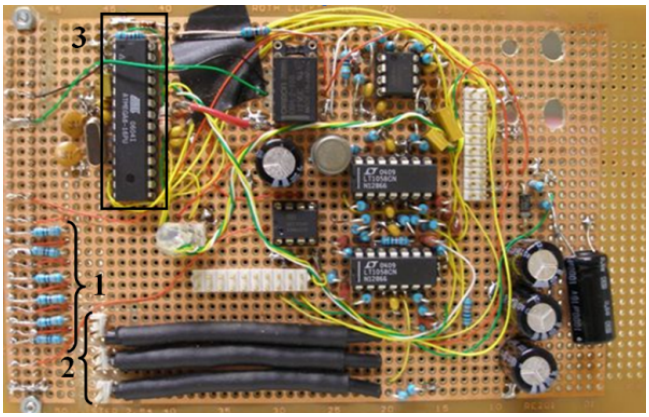

Figure 3.6: Photo of the control circuit card.

AVR family of ATMEL. The program implemented during the commissioning and testing is coded in assembler and can be found in appendix E.

The control circuit card is able to turn on and shut down different circuits of the inverter in proper order to avoid hazardous situations in case of a voltage supply drop below an acceptable level. These features will be further discussed in section 4.1.4. The control circuit card also contains three voltage dividers for scaling down the DC bus voltage ten times to be able to use the signals for measurements in the interface box. The layout of the control circuit card can be seen in Figure 3.6.

3.2.2 Driver circuit card

1. Opto coupler, Agilent Technologies HCPL-4503.
2. Voltage supply to low side, Traco power 15V.
3. Voltage supply to high side, Traco power 15V.
4. Driver circuit module (The module includes two driver circuits), International Rectifier IR2213.
5. Potentiometer (Gate resistance).
6. Test pin, measuring gate resistance.
7. Pin for output signal to IGBT.
8. Output resistance for opto coupler, 3.9kΩ.

To provide the gate of the IGBT with enough power to switch, a gate driver is needed. The driver circuit used in the inverter prototype is a IR2213 from International Rectifier. The circuit is designed for floating potentials and is fully operational up to 1200V. Each module has two output channels, one low

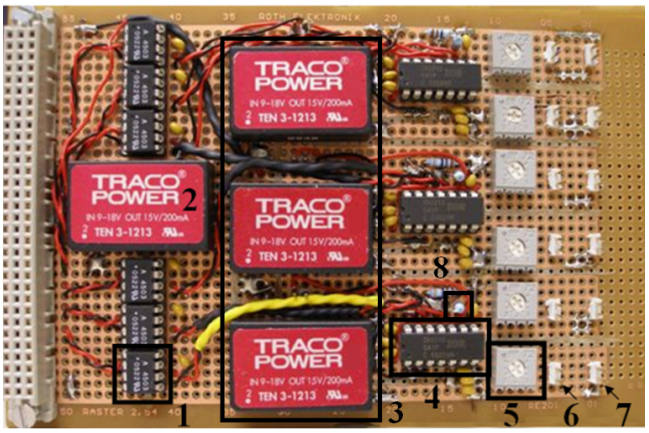

Figure 3.7: Photo of the driver circuit card.

respectively one high side. Reference to the data sheets of the driver circuit can be seen in appendix A. The inverter is equipped with a full bridge IGBT package (six transistors) and for this reason three driver circuit modules are required, one for each leg of the IGBT module.

Since the potential on the high levels are floating relative the ground level during switching, each of the high channels needs to have separate voltage supplies. For this reason the driver circuit card is equipped with four DC/DC converters, one for each high side driver channel and one common for the three low side channels. Because of the floating potentials the outputs of the control circuit card need to be galvanically isolated from driver circuit card. For this reason opto couplers are needed, one for each channel. The opto couplers chosen for the inverter prototype are HCPL 4503, a high speed opto coupler from Agilent Technologies. It has a propagation delay time to logic high at output of 0.6-1μs. All the mentioned components are mounted on a printed circuit card. A photo of the driver circuit card can be seen in Figure 3.7 and a circuit diagram can be seen in appendix C.

One of the main purposes with the inverter prototype is to study the turn-on and turn-off behaviours of the IGBT with different gate resistances. For this reason the gate resistances are implemented as potentiometers for simple adjustment between 0-40Ω. For each potentiometer, a pin for measurements is available when calibrating the gate resistance.

Chapter 4

Evaluation of hardware

4.1 Commissioning

During the commissioning phase it is of utmost importance to have full control of the entire system. A plan for commissioning was developed to be able to test all important properties in a structured way without risk of hazardous situations. The plan is chronologically written and the subsections of section 4.1 follow the steps of the plan. Each subsection separately explains the procedure and the outcome of the tests.

1. Test the DC bus with the other components disconnected. Apply a voltage to the DC bus and investigate if partial discharge occurs. Start with a voltage of 100V to verify that no short circuit occurs. If no short circuit is detected, increase the voltage stepwise up to 2.5kV. Switch between different thicknesses of the plastic layer between the copper plates and study the discharge on an oscilloscope.

2. Examine that individual pulses and pulse trains from the control circuit card behave like expected. Do this using the oscilloscope. The functions of the interface box have to be tested as well.

3. Each of the outputs from the driver circuit card have to be tested. Disconnect the power supply and connect an external power supply instead. Feed the input on the driver circuit with a square wave from a generator. To assure that the driver circuit card is able to supply enough power to the IGBT at turn-on a dummy load of 22μF is connected simulating the input properties of the IGBT.

4. To assure that the outputs on the driver circuit card are not affected in an unexpected manner when turning on and off the power supply these are tested. This is done with the same dummy load as in previous section to prevent that the IGBTs are damaged in case of a failure. The test is necessary to assure that the IGBTs always are in blocked mode when the

power supply connects or disconnects. If the demand is not met, modify the electronics and do the testing once again until a satisfying result is achieved.

5. When the functionality of the two cards is validated separately they are connected. The IGBT module is connected, a 10μF capacitor is added to the DC bus and a load of 5kΩ. Because of the floating potential of the high side it is necessary to use a differential probe when measuring pulses from the inverter. This to avoid connection to the ground potential. Apply a DC voltage of 50V. Study single pulses and check for hazardous voltage transients.

6. Repeat the test in section 5 with connected IGBT module, a 10μF capacitor to the DC bus but with a load of 50kΩ instead. Apply a DC voltage of 600V. Check for hazardous voltage transients.

7. Repeat the test in section 5 but with connected IGBT module. Connect the capacitors (4 x 2200μF) that are supposed to be used during the test procedure. Add a load of 5kΩ and a DC voltage of 50V. Check for hazardous voltage transients.

8. Repeat the test in section 7 but replace the load to 50kΩ and apply a DC voltage of 600V. Check for hazardous voltage transients.

4.1.1 Partial discharge

Procedure
The DC bus feeding the inverter consists of two copper plates with layers of isolation plastics in between. To ensure that there is enough isolation and no partial discharge occurs the hardware has to be tested. To get a realistic setup i.e. the correct distance between copper plates the DC bus has to be mounted in the inverter during the test procedure. The DC capacitors in the setup have to be isolated during the test to avoid damage. Those are rated for only 450V and a charging of them is unwanted. The IGBT module is isolated for the same reason. The screws, in connection between the DC bus and the capacitors, were changed to plastic ones for isolation reasons. A thick plastic layer was also put between the DC bus and the DC capacitors for extra safety.

The copper plates were connected to an "ISO tester", a voltage source able to provide up to 5kV at a low current. One of the copper plates was connected to ground through one resistor (5.6kΩ) in parallel with two diodes connected in series. The discharges were measured with an oscilloscope across the resistor and the diodes, see the setup in Figure 4.1. The applied voltage across the DC bus during operation in the vehicle is set to 700V. During the evaluation of the plastic layer between the copper plates a margin of a more than three times higher voltage is applied (2.5kV).

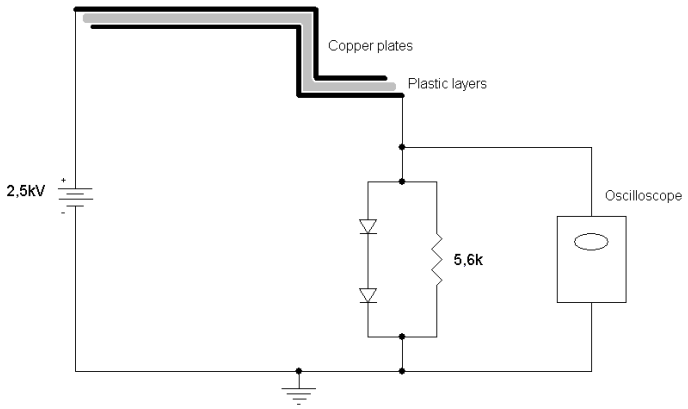

Figure 4.1: Hardware description of the partial discharge test.

Outcome

The partial discharge arose first at 2.5kV when only one thin layer of plastic (0.1 mm) was used between the copper plates, seen in Figure 4.2. The phenomenon was expected since materials are rarely totally homogeneous.

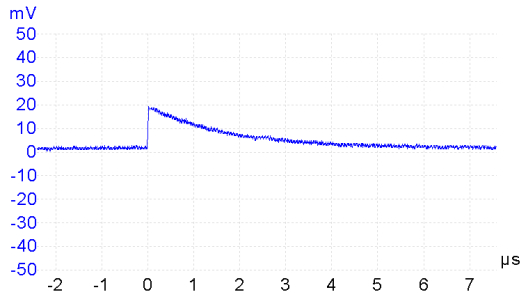

Figure 4.2: A partial discharge between the copper plates.

The outcome of the discharge can be explained as a RC-circuit defined by the capacitance between the copper plates and the resistor connected to ground, see equation (4.2).

The probe capacitance on the oscilloscope does not affect the measurement because of its small value (13pF). The capacitance of the copper plates is estimated in equation 4.1. The value of the relative permittivity, ϵ_r, for the plastic used in the setup is around 2.5 and ϵ_0 is a constant for permittivity in vacuum.

$$C = \epsilon_0 \cdot \epsilon_r \cdot \frac{A}{d} = \frac{10^{-9}}{36\pi} \cdot 2.5 \cdot \frac{3 \cdot 10^{-2}}{10^{-3}} \approx 1nF \tag{4.1}$$

$$\tau = R \cdot C = 5.6k\Omega \cdot 1nF \approx 5.6\mu s \tag{4.2}$$

The time constant, τ, calculated to 5.6μs seems to be realistic due to the shape of the curve in Figure 4.2.

The phenomenon arose even if the thin layer was replaced with a thicker one (0.3mm). When two thin layers of plastics were added the discharge still appeared at 2.5kV. Two thick layers replaced the thinner ones and now no discharges were detected at 2.5kV. To be sure that no discharge will occur later in the testing procedure, two of each thickness of the plastics were mounted between the copper plates.

4.1.2 Evaluation of the control circuit card and the interface box

Procedure
To evaluate that the function of the control circuit card, described in section 3.2.1, square wave pulses from the AVR processor have to be examined to assure correct voltage level and pulse length. The assembler code can be seen in appendix E. Together with the control circuit card, functions of the interface box were tested such as the pulse firing button and the thumb wheel switch.

Outcome
The button firing the pulses did not work as expected. Fault detection showed that the button did not work properly due to a floating potential on the input of the processor. To solve the problem the thumb wheel switch and the button were connected to ground in series with one resistor of 1kΩ for each device.

The square wave pulses from the AVR processor had correct voltage level, 5V, and the pulse lengths agreed with the determined.

4.1.3 Evaluation of driver circuit

As described in section 3.2.2 the driver circuit card consists mainly of six opto couplers, three driver modules and six gate resistances. The components have to be tested and evaluated to assure that a proper function can be guaranteed. This section is divided into four different test procedures, the opto couplers, the driver circuits, the gate resistances and blanking time. An external voltage supply is used and the signals are generated of a pulse generator.

Opto couplers

Procedure
The output signals from the opto couplers were measured to get a view of how the delay time in the device were affected by the input and output resistor pair. The location of the resistor pair can be seen in Figure 2.6 in section 2.3. A resistor pair of 820Ω on the input and 22kΩ on the output was first tested. This gave a relatively large time delay. The values of the resistor pair were decreased to 180Ω/5.6kΩ and then further on to 180Ω/3.9kΩ.

Outcome
A rise time in the opto coupler as fast as possible is desirable. The resistor pair of 180Ω/3.9kΩ was selected as the most adapted values because of its fast behaviour, see Figure 4.3. The values of the resistor pair were not decreased further to get an even faster rise time. This because the control circuit card would not then be able to deliver enough power. According to the data sheets for the AVR the maximum DC per IO pin is 40mA and the current transfer ratio in the data sheets for the opto coupler specified to a range between 19 and 50, reference to data sheets can be found in appendix A.

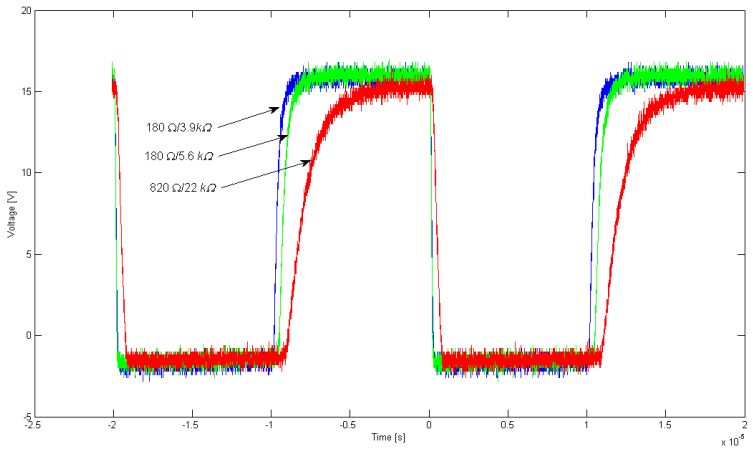

Figure 4.3: Delay time in opto coupler with three different resistor pairs (820Ω/22kΩ, 180Ω/5.6kΩ, 180Ω/3.9kΩ).

The output voltage from the AVR is 5V i.e. the input signal to the opto coupler. Due to Ohm's law it results in a delivered current of 28mA from the processor for the chosen resistor pair. This gives a safety margin of the consumed current from the processor of approximately 25%. The voltage supply to the opto coupler is 15V this results in a current on the output of 3.85mA. The output divided by input current of the opto coupler results in a transfer ratio of 13%. The value is less than the minimal of 19%. A too low transfer ratio can result in a poor signal quality. The signal is measured and for this application it is satisfying.

Driver module

Procedure
The output signal from the six driver circuits was tested each with a load to assure that all channels on the driver circuit card behaved in the same manner. The load was simulated by a capacitance of 22nF, a value two and half times as the input capacitance of the IGBT, to test the capability of the driver circuit to supply current.

Outcome

During the test procedure of the driver circuit no output signal was detected. It was discovered in the data sheets that the potential for the high side voltage supply level (V_B) has to have equal or higher potential than the low side voltage supply (V_{CC}) on the driver circuit to work properly. This was not considered in the first design. The solution was simple, a diode was implemented to get the proper potentials.

The signals on the outputs of the driver modules behaved like expected and similar to each other. By this test the conclusion that the six channels act in the same manner could be drawn.

Gate resistances

Procedure

To get a feeling of how different values of the gate resistance affect the rise and fall time at turn-on and turn-off the value of each potentiometer was varied between 0-40Ω in intervals of 10Ω.

Outcome

In Figure 4.4 it can be seen that the rise time is as expected strongly dependent on the value of the gate resistance. A lower value of the gate resistance gives a faster rise time and vice versa.

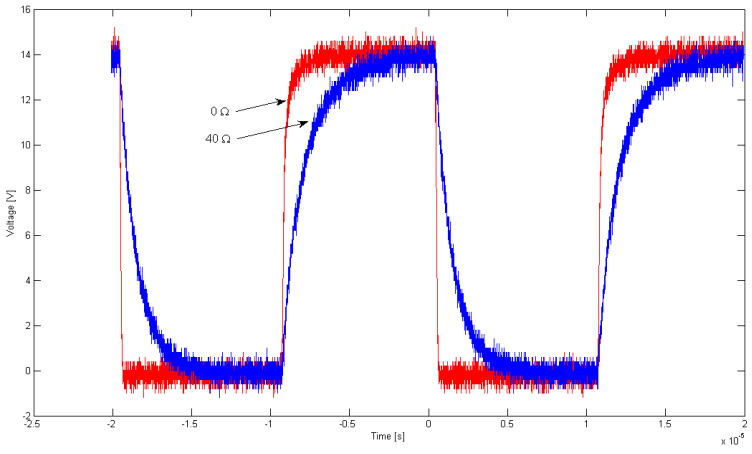

Figure 4.4: Rise and fall time depending on different gate resistances.

Delay time

Procedure

The time delay from the input of the opto coupler to the output of the driver circuit was measured to be able to calculate the value of the blanking time. A blanking time between the signals is needed to avoid that two IGBTs in the

same phase leg are active at the same time. A too short blanking time could result in a short circuit and must of course be avoided.

Outcome
The measurements of the delay time resulted in a value of 0.8μs from the input of the opto coupler to the output of the driver circuit card. The obtained graphs can be seen in Figure 4.5. To understand the figure it has to be mentioned that the opto coupler inverts the signal. The delay time is different depending on turn-on or turn-off, but the longest time has to be taken into account.

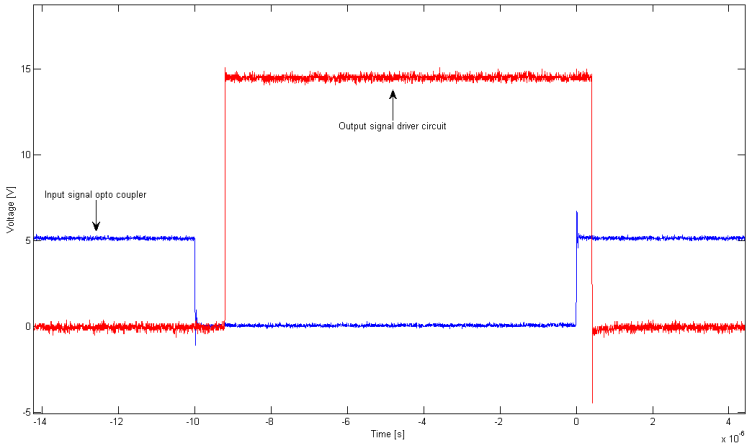

Figure 4.5: Time delay from the input to the output of the driver circuit card.

4.1.4 Evaluation of disconnected power supply

Procedure
It is important to investigate if the different parts of the driver circuit are shut down in a proper order in a possible failure of the power supply. The IGBTs have to be blocked for signals and be turned off to prevent cross conduction. The components of interest are the voltage supply to the high and low side of the driver circuit (V_{B}, V_{CC}) and the supply to the logic (V_{DD}), see circuit diagrams in appendix C and D. At an abrupt supply failure the supply to the high side has to be shut down first, then the low side and finally the logic voltage supply. When the power is reconnected it is important that V_{DD} has to be active first, to be able to control the outputs.

Outcome
A test was done when the power supply was disconnected and the system behaved satisfying. The process is shown in Figure 4.6.

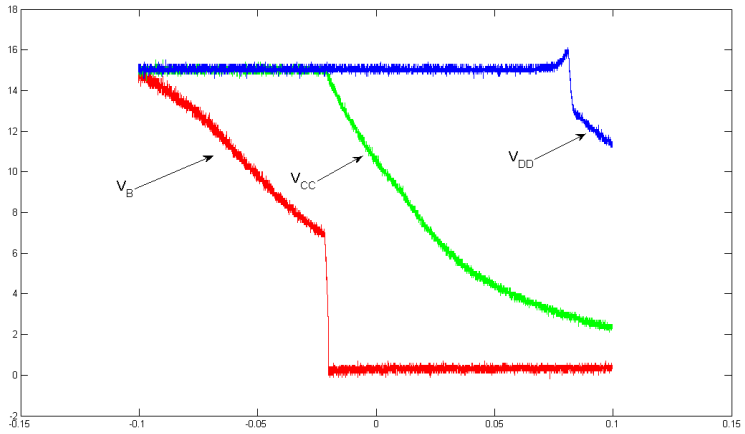

Figure 4.6: Shut down of V_{B}, V_{CC} and V_{DD} in proper succession.

4.1.5 Evaluation with the individual parts connected together (expect the DC bus capacitors)

Procedure
To ensure the functionality of the control circuit card and the driver circuit card together with IGBT module the system has to be tested. The evaluation was realized with a small DC capacitor (10μF) to avoid a hazardous situation. The system was tested with single pulses controlled by the interface box and a DC bus voltage of 50V. The pulses were measured with a differential probe. A relatively large load of 5kΩ was used to avoid large currents.

Outcome
Problem arose when the control circuit card and the driver circuit card were tested together. It was shown that a relay for the driver voltage supply on the control circuit card was not able to keep the voltage of demand. The voltage decreased under the allowed level and increased again which gave rise to oscillations, location can be seen in appendix D. When measuring the signals in connection to the relay a dip on the voltage supply was discovered. The most probable reason for this behaviour was that the driver circuit consumes a too large current momentarily when it was turned on. The DC/DC converter was unable to provide enough current and the consequence was a voltage drop of approximately 1V during 10 μs. To solve the problem a capacitor was mounted to support the voltage supply. A theoretical value of the needed capacitor is approximately 8uF, the calculations are shown in equation (4.3).

$$dU/dT = i/c = 1V/10\mu s = 0.8/c \Rightarrow c = 0.8/10^5 = 8\mu F \tag{4.3}$$

The problem was solved after the capacitor was mounted. The setup worked as expected and an applied voltage of 50V was not a problem, see Figure 4.7.

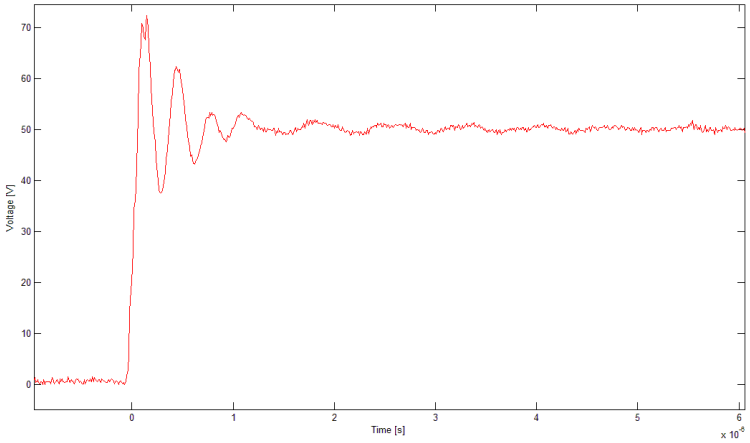

Figure 4.7: Output of the inverter at 50V DC voltage

4.1.6 Increased DC bus voltage to 600V

After examining that the systems worked satisfying at a low voltage (50V) the DC voltage was increased in steps of 100V to 600V. The load was changed to 50kΩ to avoid hazardous currents at high voltage. No unexpected behaviour occurred, see Figure 4.8.

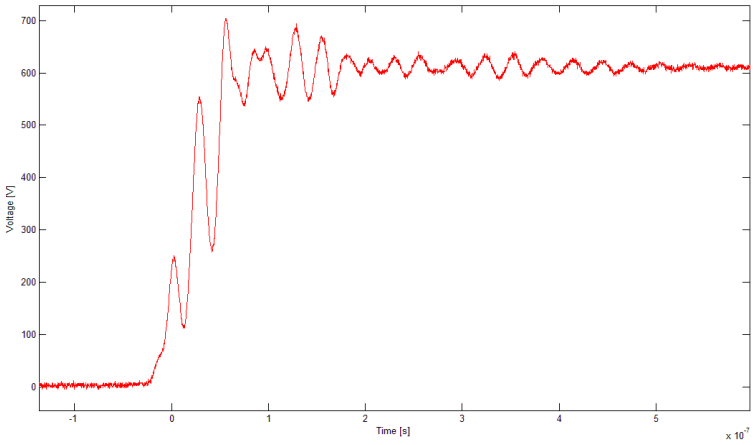

Figure 4.8: Output of the inverter at 600V DC voltage

4.1.7 Evaluation with the individual parts connected together including the DC bus capacitors

After examining that the systems worked satisfying at a high voltage and with a small DC capacitor without too much oscillations the proper capacitors of (4 x 2200μF) were implemented. The value of the load was set to 5kΩ and the DC bus voltage was 50V. No unexpected behaviour occurred.

4.1.8 Increased DC bus voltage to 600V including DC bus capacitors

After examining that the systems worked satisfying at a low voltage (50V) and proper DC capacitors (4 x 2200μF) the DC voltage was increased in steps of 100V to 600V. The load was changed to 50kΩ to avoid hazardous currents at high voltage. No unexpected behaviour occurred.

Chapter 5

Simulations

The idea of using a simulation tool for analyzing a circuit is to be able to study behaviour and make corrections fast and easy. The tool used for simulations in this thesis is Pspice. The program applies the text based simulation tool, Spice. The advantage of Spice based simulation tools is that Spice models of real components are quiet easy to obtain. Pspice have the possibility to convert text based Spice models to graphic components.

At the beginning the idea was to create a simulation environment as similar to the inverter prototype as possible. The component suppliers were contacted and asked for Spice models. Spice models similar to almost all components were possible to obtain except a model of the IGBT module. The IGBT module was for this reason approximated with another model from the same supplier with similar characteristics. The simulation model of the inverter was built in Pspice, see Figure B.1.

It was shown that the Spice models based on complex modules are a major problem in Pspice simulations. The model of the driver circuit caused problems due to internal overflow. The problem is hard to solve because no measurement inside the module is possible to perform. Large efforts were made to solve the overflow problem but without success.

5.1 Simulation setup

Due to the problem with internal overflow in the simulations a decision was taken to build a model of one phase of the inverter as simple as possible. This to evaluate if simulations could be useful in the process of developing and testing the inverter. The simulations were made with inspiration from examples in the course of power electronics at LTH. The simulation examples in the course are made in LTspice SwitcherCad III, a freeware simulation tool similar in many aspects to Pspice but with less advanced features.

With the LTspice model in mind a simple Pspice model was developed excluding opto couplers and driver circuit seen in Figure 5.1.

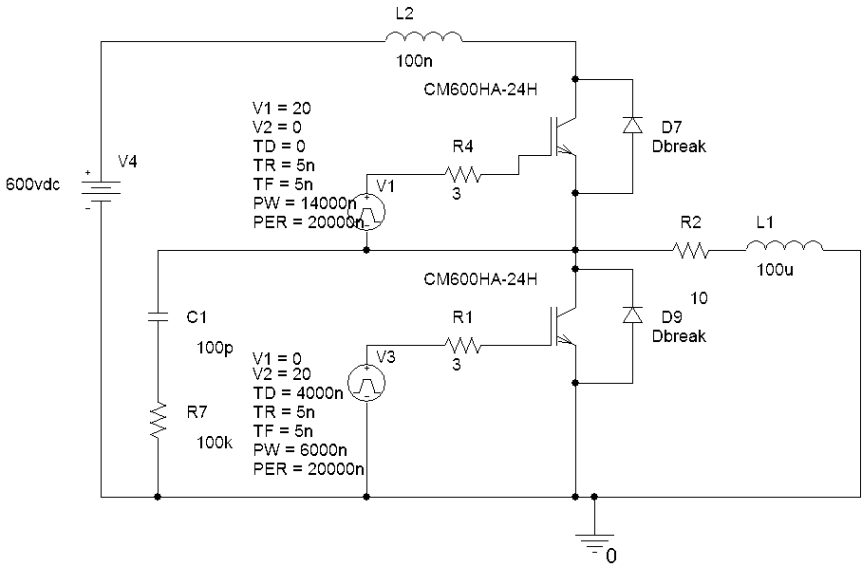

Figure 5.1: Simple Pspice model of a half bridge.

The idea with the simplified model is to study the switching behaviour with and without snubber circuits. The same DC level as in the laboratory, 600V, is used in the simulations. When the simulations were done with a relatively large stray inductance of 100nH, L2 in Figure 5.1, it was shown that the simulations in Pspice presented realistic results, such as overshoots and oscillations. The oscillations are wanted to be able to evaluate snubber circuit design. A simulation of the voltage across the load (R2+L1) is done and the switching behaviour is shown in Figure 5.2. The overshoot at turn-off is more than 300V and depending on the large stray inductance.

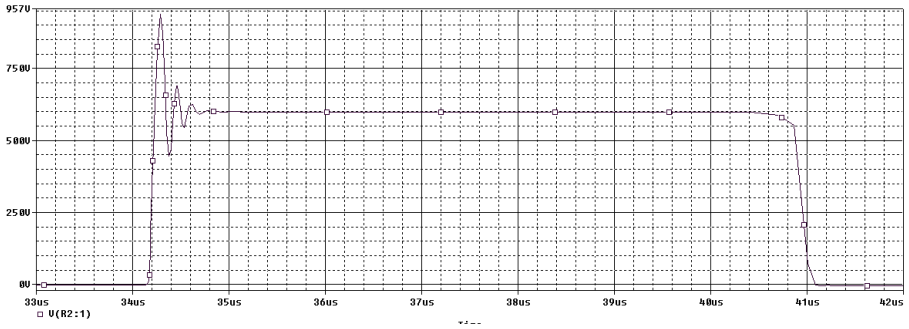

Figure 5.2: Switching behaviour of the circuit in Figure 5.1.

Because a different IGBT is used in the simulation than the one in the inverter box some characteristics differ. The rise and fall times are slower for the simulations than for the real inverter. With this in mind the simulations will only

be used for studying the switching behaviour when snubber circuits are implemented. The turn-on behaviour is neglected since turn-on snubber circuits are seldom needed for IGBTs because of its capacitive input [6].

5.2 Snubber design

Three different snubber circuits will be evaluated in this section. The ones of interest are charge discharge RCD, RCD clamp and restricted decoupling capacitor circuit, these are described in section 2.4. A solution with a decoupling capacitor will also be included in the evaluation. Simulation of the power losses in the passive components for the three snubber circuits will be done to show the characteristics differ between different solutions.

To be able to determine the values of the components in a snubber circuit an estimation of the stray inductance in the circuit has to be done first. If a waveform of the switching process is possible to measure, as the one in Figure 5.3, the stray inductance can be calculated. The frequency (f_0) of the waveform is generated by a LC circuit [13], where the capacitance (C) is equal to the output capacitance of the IGBT. The value can be found in the data sheets for the IGBT module, see appendix A. In equation (5.1) the calculation of the stray inductance (L) is shown.

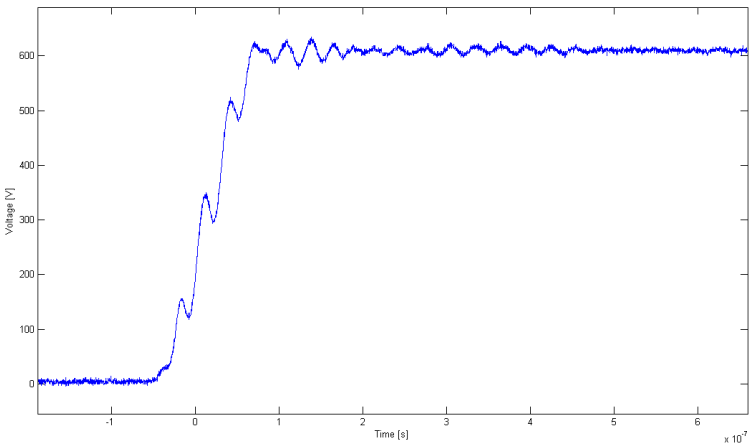

Figure 5.3: The resonance frequency generated by stray inductance and the output capacitance of the IGBT.

$$f_0 = \frac{1}{2 \cdot \pi \cdot \sqrt{L \cdot C}} \Longrightarrow L = \frac{1}{C \cdot (2\pi \cdot f_0)^2} = \tag{5.1}$$

$$= \frac{1}{7.5 \cdot 10^{-8} \cdot (2\pi \cdot 37 \cdot 10^6)^2} \approx 25nH$$

A peak voltage limit, V_{pk}, is set to 630 V, which corresponds to 5% of the DC bus level and can be considered as an acceptable overshoot voltage level.

The starting point when designing a snubber circuit is to calculate the stray inductance in the circuit. The energy stored in the stray inductance should be absorbed in a snubber capacitor, this not to influence the switching behaviour, see equation (5.2). The energy stored in the snubber capacitor has to be discharged, this through a snubber resistor. As described in section 2.4 this can be accomplished by different snubber circuits working by the same principal. The value of the resistance can be chosen in different ways depending on how fast the snubber capacitor should be discharged. In equation (5.4) a resistance is calculated so that the snubber capacitor is discharged by 0.25% of the DC bus voltage in one switching period [6]. The value of the resistance affects the withstanding of power, required of the resistor. A smaller value of the resistance require a better withstanding of power but gives a faster discharge course and a more effective snubber circuit. A trade of between these properties have to be done.

$$\frac{1}{2}Li^2 = \frac{1}{2}Cv^2 \tag{5.2}$$

The assumptions made above give following equations

$$C_{\mathrm{sn}} = \frac{L_{\mathrm{S}} \cdot I_0^2}{(V_{\mathrm{pk}} - V_{\mathrm{CC}})^2} = \frac{100 \cdot 10^{-9} \cdot 40^2}{(630 - 600)^2} = 0.18\mu F \tag{5.3}$$

$$R_{\mathrm{sn}} = \frac{1}{6 \cdot C_{\mathrm{sn}} \cdot f_{\mathrm{sw}}} = \frac{1}{6 \cdot 0.18 \cdot 10^{-6} \cdot 5 \cdot 10^3} = 188\Omega \tag{5.4}$$

The calculated value of the snubber capacitance is reasonable according to the literature [11].

There is a major difference in consideration of losses in the passive components between different snubber circuits. To show the differences, the losses in the passive components are compared. Equation (5.5) is valid for the restricted decoupling capacitor and the RCD clamp snubber circuit. In equation (5.6) the power losses in the charge discharge RCD is calculated.

$$P_{\mathrm{R}} = \frac{C_{\mathrm{sn}} \cdot (V_{\mathrm{pk}}^2 - V_{\mathrm{CC}}^2) \cdot f_{\mathrm{sw}}}{2} =$$

$$= \frac{0.18 \cdot 10^{-6} \cdot (630^2 - 600^2) \cdot 5 \cdot 10^3}{2} = 16.4W \tag{5.5}$$

$$P_{\mathrm{R}} = \frac{C_{\mathrm{sn}} \cdot (V_{\mathrm{pk}}^2) \cdot f_{\mathrm{sw}}}{2} =$$

$$= \frac{0.18 \cdot 10^{-6} \cdot (630^2) \cdot 5 \cdot 10^3}{2} = 178.6W \tag{5.6}$$

It is shown that the requirements of withstanding power in the passive components are really high for the charge discharge RCD, resulting in high cost and demanding a large volume of the components.

5.3 Simulation of switching behaviour and losses in snubber circuits

To make the model as realistic as possible a stray inductance of 25nH (L2) is implemented in the Pspice model, Figure 5.1, according to equation (5.1). All the simulations are based on the model in Figure 5.1 with the configuration of a snubber capacitor of 0.18μF and a resistor of 188Ω according to the equations (5.3-5.4). The plots of the simulated turn-off behaviour have the same time scale for easy comparison except for the decoupling capacitor. It is of interest to see the oscillation of the decoupling capacitor and therefore another time scale is used.

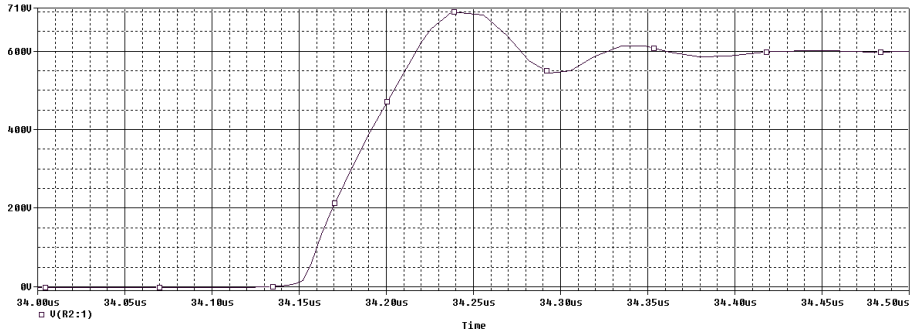

Figure 5.4: Simulation at turn-off without a snubber circuit.

In Figure 5.4 is a turn-off behaviour presented for a simulated circuit without a snubber circuit. The overshoot exceeds 700V which equals to 16.7% according to the DC bus level of 600V.

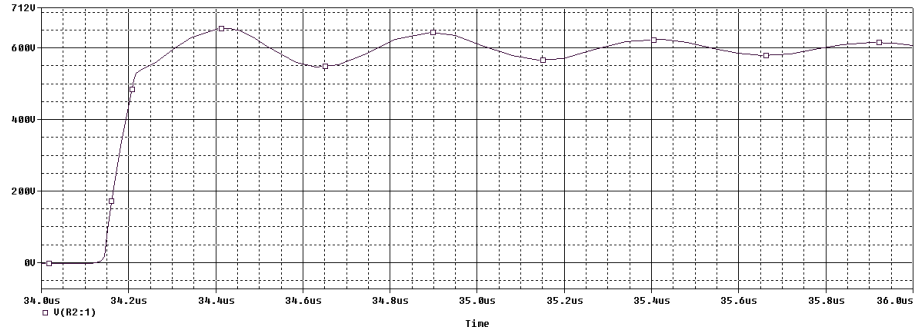

Figure 5.5: Simulation at turn-off with a decoupling capacitor.

In Figure 5.5 it can be seen that a decoupling capacitor has a favourable effect on the voltage overshoot but an oscillating behaviour is introduced. This in absence

of snubber resistor to damp the oscillations. Normally the system contains parasitic resistances that damp these oscillations but this can not be taken for granted. This is important to have in mind when introducing a snubber capacitor.

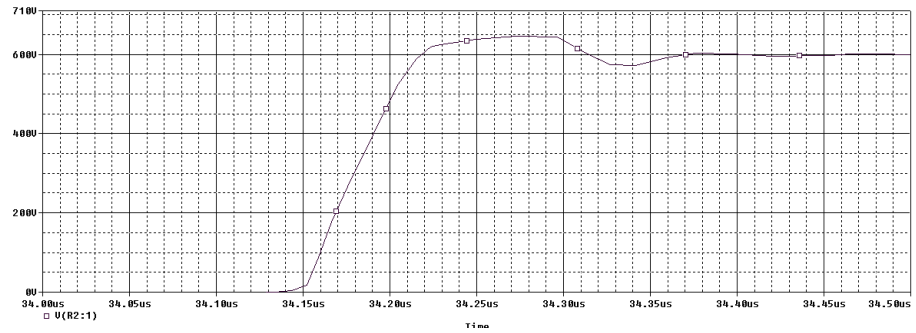

Figure 5.6: Simulation at turn-off with a discharged restricted decoupling capacitor.

When simulating the same circuit with a charged restricted decoupling capacitor connected the overshoot is damped to a level of 650V, which corresponds to 8.3%, see Figure 5.6. The oscillations are damped in a better way than for the decoupling capacitor because of the implemented resistor and diode.

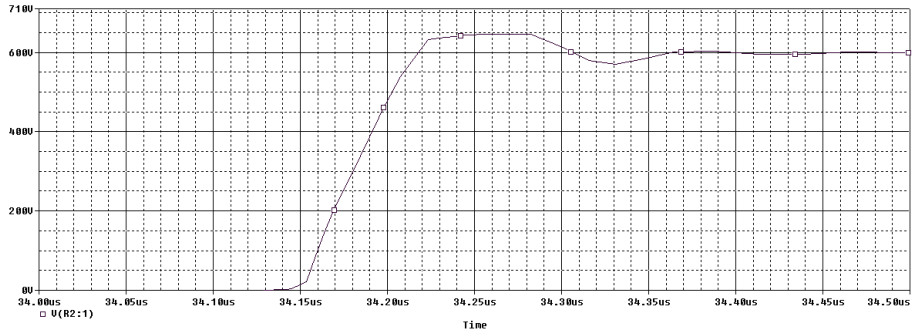

Figure 5.7: Simulation at turn-off with an RCD clamp snubber circuit.

In Figure 5.7 it can be see that the turn-off behaviour in the RCD clamp snubber circuit is similar to the charged restricted decoupling capacitor circuit.

The charge discharge RCD snubber circuit has the tendency to slow down the rise time of the voltage at turn-off, but have a smaller impact on the overshoot than the restricted decoupling capacitor circuit, see Figure 5.8. As described by equation (5.6) the power loss in the snubber components is a major disadvantage for the charge discharge RCD snubber. It can be easily seen in the simulation of the power loss in the snubber resistor during the switching progress in Figure 5.9.

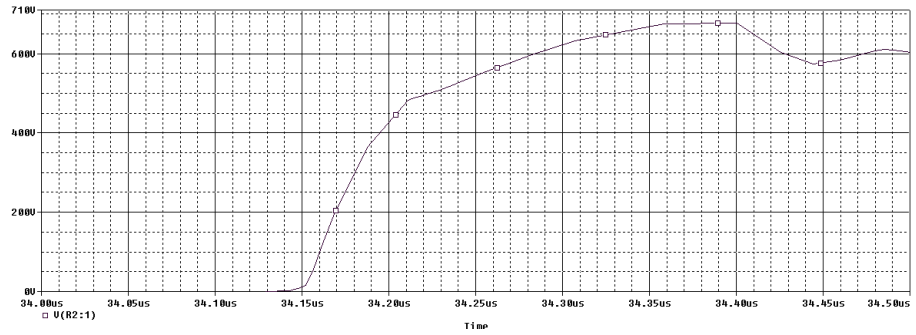

Figure 5.8: Simulation at turn-off with a charge discharge RCD snubber circuit.

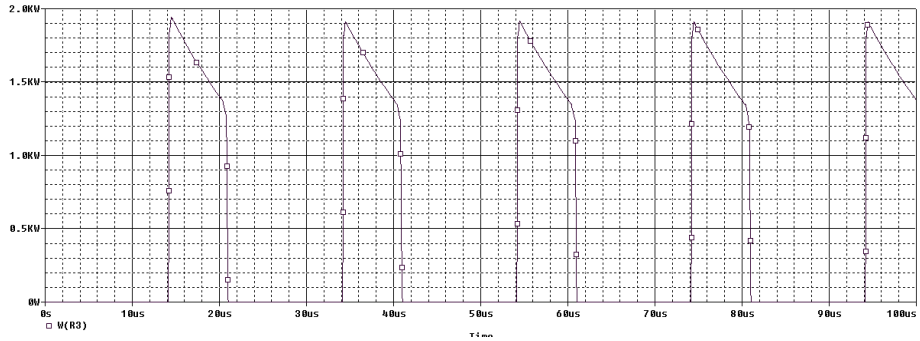

Figure 5.9: Power loss for a resistor in a charge discharge RCD snubber circuit.

The power losses in a snubber resistor for both the RCD clamp circuit and the restricted decoupling capacitor are shown in the Figures 5.10-5.11. The plots shows that the components for the latter snubber circuits are affected of a much lower stress than the ones for the charge discharge RCD snubber circuit.

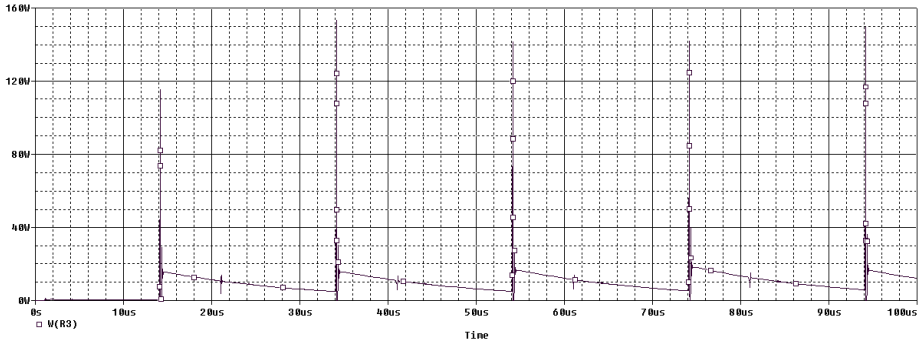

Figure 5.10: Power loss for a resistor in a restricted decoupling capacitor circuit.

In the simulations it can be seen that an accurate model of the IGBT together with good estimation of the stray inductance are enough to perform simulations of the switching behaviour of an inverter. When adding additional attributes to the simulations there is a major risk of simulation problems such as the problem

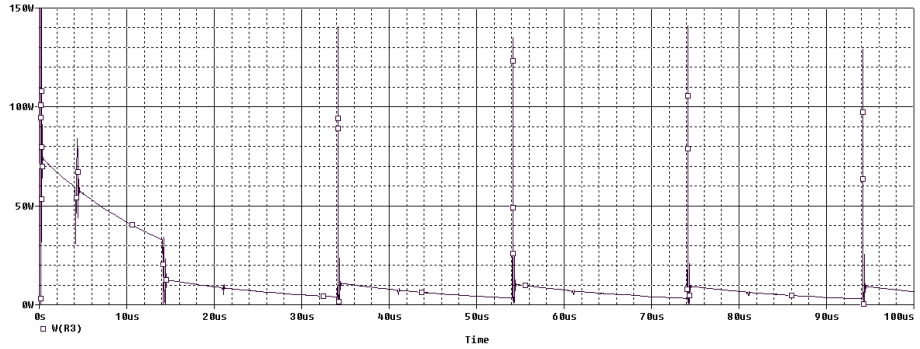

Figure 5.11: Power loss for a resistor in an RCD clamp snubber circuit.

described with overflow in complex models. The suggestion is for this reason to keep simulation models as simple as possible. The switching behaviour in addition to snubber circuit evaluations are the two essential parts where the largest benefits of simulations are made. The importance of minimizing the stray inductance can easily be realized when comparing the results in Figure 5.2 and Figure 5.4.

5.4 Simulation of switching losses

Snubber circuits could be a solution to the problem with high switching losses. When a snubber is implemented intention is to reduce overshoot and oscillations. When the overshoot is reduced, it is possible to use a smaller gate resistance to fasten up the switching behaviour. It is important to note that the delay of some of the simulation results in Figure 5.12-5.14 is due to Pspice and is not of interest.

To show how the different snubber solutions affect the switching losses an acceptable level of the overshoot was set to 5% i.e 30V. In Figure 5.12 a simulated turn-off can be seen. All simulation results are from the high side IGBT.

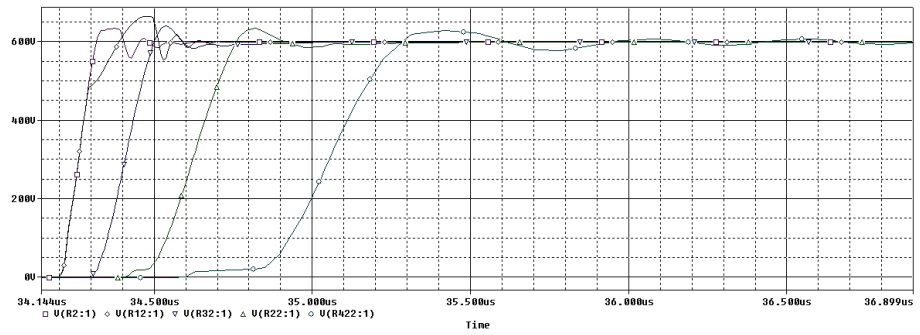

Figure 5.12: Turn-off behaviour with different setups.

In Figure 5.12 the simulation results of the different setups can be seen, from

left to right: RCD clamp snubber circuit, charge discharge snubber circuit, discharged restricted decoupling capacitor, without snubber and with a decoupling capacitor. In the Figure 5.12 it can be seen that the solution with a decoupling capacitor makes the rise time slower in relation to the other solutions. The reason for this is that a proper function requires stray resistances in the circuit to be able to consume the energy stored in the snubber capacitor. These are not implemented in the simulation model. The results for the setup with a decoupling capacitor is for this reason not of interest in the following simulations.

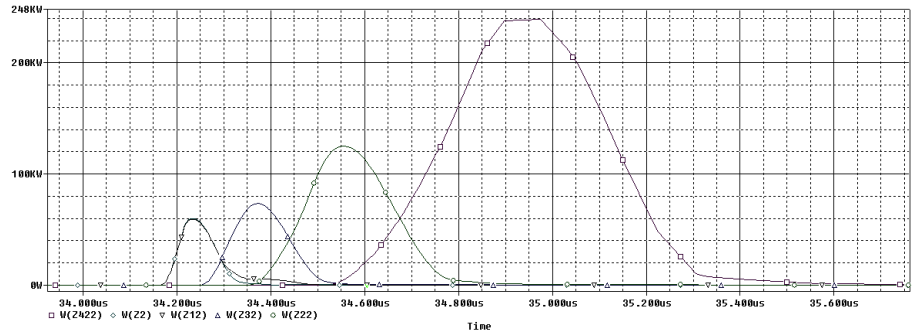

Figure 5.13: Switching losses at turn-off.

In Figure 5.13 and 5.14 the switching losses are shown. The most clear improvement can be seen at turn-off, see Figure 5.13. A comparison between the losses in the different solution can be seen in table 5.1.

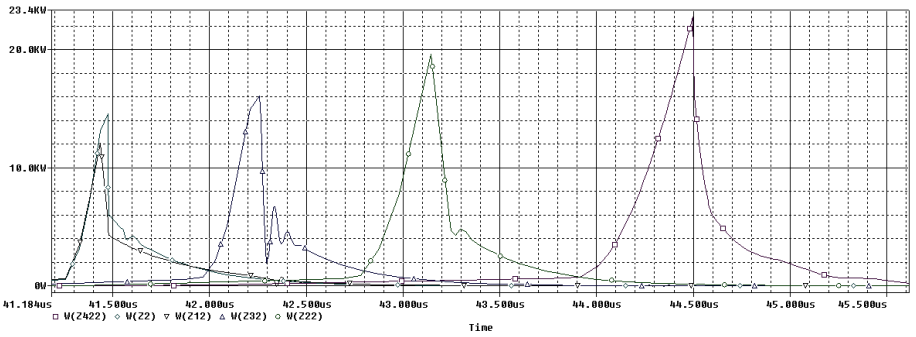

Figure 5.14: Switching losses at turn-on.

Table 5.1: Energy losses in an IGBT

Setup	Turn-off loss (mWs)	Turn-on loss (mWs)	Total loss (mWs)
Without snubber	26.0	5.5	31.5
Decoupling capacitor	97.5	7.1	104.6
Discharged restricted decoupling cap.	9.3	4.6	13.9
Charge Discharge RCD snubber	6.0	3.3	9.3
RCD clamp snubber	5.3	3.8	9.1

The simulation results show that relatively large loss benefits can be made by using a snubber circuit to speed up the switching behaviour, see table 5.1. It is important to note that the simulation results are strongly dependent on the estimations of parasitic inductance and resistance.

Chapter 6

Test results

This chapter will describe and show measurements done at turn-on and turn-off. Construction of two different types of snubber circuits are done. The measurements are done on one transistor on a phase of the IGBT module. The switching behaviour is measured in the same way both with and without snubber circuits. The outcome of the switch behaviour with and without snubber circuits will be compared and analyzed in the latter part of the chapter.

6.1 Switch behaviour

The switching behaviour is depending on the gate resistance. In Figure 6.1 the behaviour can be seen for three different gate resistances (0Ω, 15Ω and 40Ω). The important parameters to consider are the rise time, voltage overshoot and oscillations. As seen in the figure a low gate resistance gives a short rise time but increases the oscillations and the voltage overshoot, while a higher resistance increases the rise time but damps the oscillations and voltage overshoot. It is desirable to have as fast rise time as possible but the allowable voltage overshoot level is in many cases the decisive part. A large voltage overshoot can in worst case damage the inverter and short circuit it. Oscillations are caused by stray inductance in the inverter and it is desirable to keep them as low as possible.

As for the rise time, a higher value of the gate resistance will slow down the process and give a longer fall time. The negative voltage dip in Figure 6.2 is independent of the gate resistance and a consequence of reverse recovery current from the switching diode.

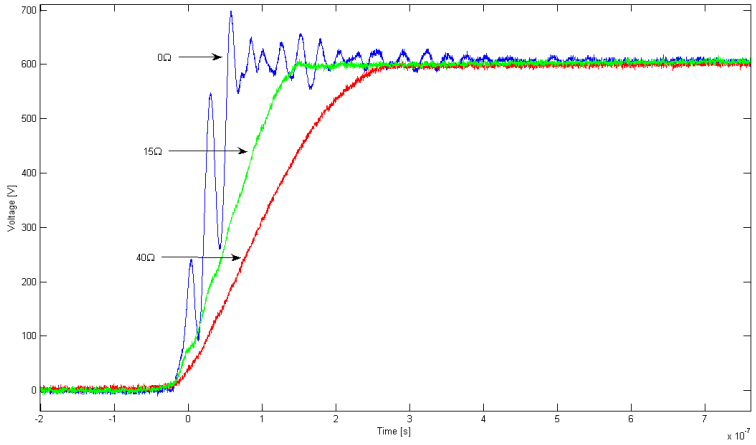

Figure 6.1: Different rise times depending on the value of the gate resistance.

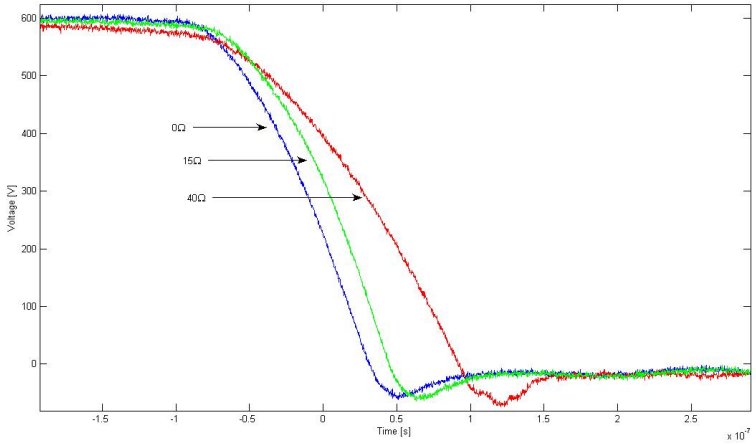

Figure 6.2: Different fall times depending on the value of the gate resistance.

6.2 Snubber measurements

For evaluation of snubber circuits, two different types were chosen, the discharged restricted decoupling capacitor and the RCD clamp snubber circuit. The charge discharge RCD snubber circuit was not chosen because it would need unrealistic large passive components due to high power requirements, this according to equation (5.6). The passive snubber components in a charge discharge snubber circuit are exposed for the entire DC bus voltage and for this reason it is not realistic to use this type of snubber in this kind of high voltage application.

The results of the equations (5.3-5.5) give a hint of in what range the value of the components should be selected [12]. Four different setups of the values were chosen to evaluate the effects of the snubber circuit. In the table 6.1 are the chosen values presented.

Table 6.1: Values of the components to four different snubber circuits.

Capacitance (μF)	Resistance (Ω)	Power requirements (W)
0.01	3300	3
0.1	330	10
0.2	150	30
0.3	100	30

Snubber capacitors for direct connection to the IGBT module are available, but the snubber solutions requested in table 6.1 were hard to find. Instead of snubber modules each component was ordered separately to get the desired values. Each snubber circuit was mounted and soldered on a printed circuit board and connected to the inverter by wires. A perfect result according to reducing the stray inductance in the snubber circuit is at this moment not of great importance and therefore the snubber circuit is not mounted directly on the IGBT module. The restricted decoupling capacitor was mounted on the DC bus outside the inverter box. The RCD clamp snubber circuit that has three connections was also connected to the phase of interest. The behaviour was measured on one output phase and the negative input potential. In section 2.4 the circuit diagrams of the two snubber circuits are available and photos of them can be seen in Figure 6.3 and 6.4.

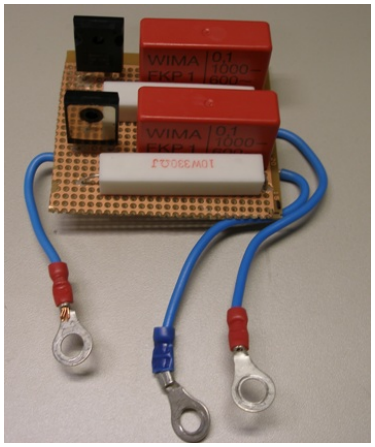

Figure 6.3: A photo of an RCD clamp snubber.

To investigate the divergence between the RCD clamp snubber and discharge restricted decoupling capacitor measurements at turn-off, with a gate resistance of 0Ω, was made. The value of the snubber capacitance for the both snubber circuits is in this setup 0.1μF.

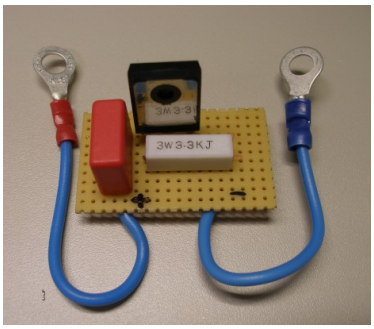

Figure 6.4: A photo of a discharged restricted decoupling capacitor snubber.

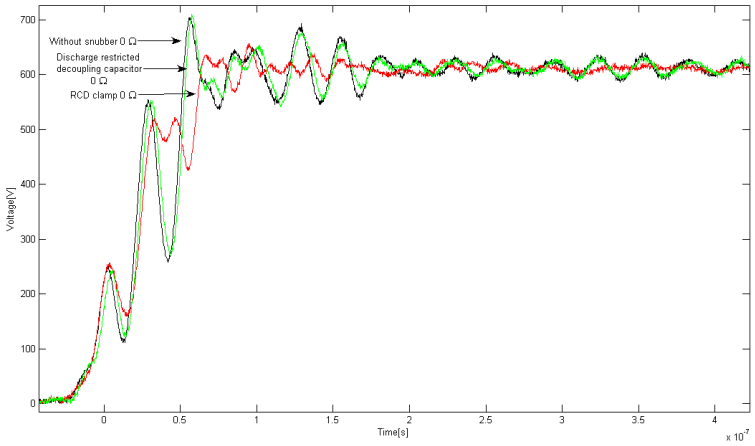

Figure 6.5: Turn-off behaviour with a value of 0Ω on the gate resistance for an RCD clamp snubber, a discharge restricted decoupling capacitor and without a snubber circuit.

As seen in Figure 6.5 does the RCD clamp snubber damp the overshoots. The discharge restricted decoupling capacitor does not reduce the overshoot and behaves in the same manner as the one without a snubber circuit. After more measurements the conclusion could be drawn that the discharge restricted decoupling capacitor does not improve the switching behaviour and is therefore not of interest further on, this in contrary to the simulation in chapter 5.

There are several ways to evaluate the functions and the usefulness of snubber circuits. In Figure 6.6 the RCD clamp snubber is evaluated in consideration of the dimensioning of capacitance and resistance. Here, it was desirable to get similar behaviour at turn-off. A reference signal that was considered as an acceptable level was set, this without a snubber circuit. To be able to achieve similar switching behaviour the gate resistance was adjusted when the RCD clamp snubber circuit was connected. The gate resistance of the reference signal (without a snubber circuit) became 12Ω. The RCD clamp snubber circuit consisting of the lowest value of the capacitance, 0.01μF, did not affect the curve

i.e. the same value of 12Ω had to be used. When the snubber capacitance was increased a lower gate resistance was required. For 0.1μF a value of 7Ω was required to get similar switching behaviour. At higher values of the capacitance the value of the gate resistance stagnated around 5Ω and the difference between 0.2μF and 0.3μF was almost not notable. Due to the calculated value of 0.18μF, see equation (5.3), the experimental measurements are well in accordance to the theory.

The conclusion of the measurement is that an RCD clamp snubber circuit with a capacitor of 0.2μF and a resistance of 150Ω is the best solution to reduce the gate resistance from 12Ω down to 5Ω.

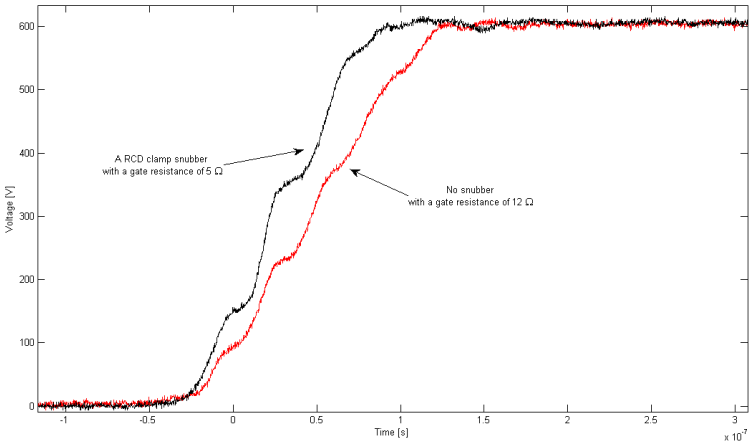

Figure 6.6: Different rise times depending on different values of the gate resistance.

As said before an RCD clamp snubber is to prefer to be able to reduce the value of the gate resistance. The reason of reducing the value of the gate resistance is to get a faster rise time and in that way reduce the switching losses. In Figure 6.6 is the difference between an RCD clamp snubber circuit with 5Ω gate resistance compared with one without a snubber circuit with 12Ω resistance. The result is a faster rise time of 40ns.

6.3 Current measurements

The output signal cables of the current transducer are located close to the phases, that generate high currents. These produce strong electromagnetic fields resulting in noise on the voltage measurement signal, due to inductive disturbances, see section 2.6. The output signal from the current transducers is a voltage in the region of a few volts. The maximum current of 50A corresponds to 4V on the output signal, see appendix A. In Figure 6.7 the current measurement is shown in the original design.

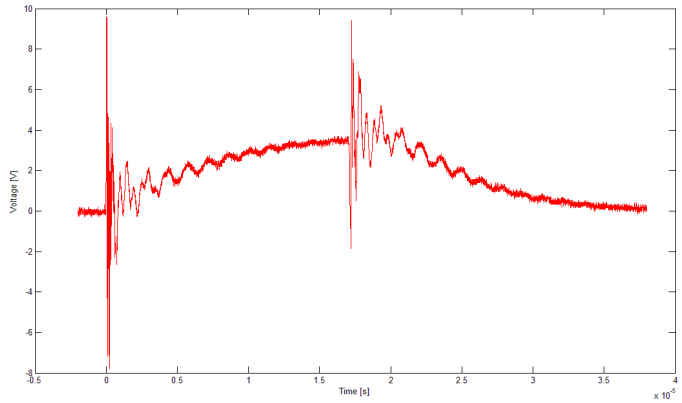

Figure 6.7: Disturbance on the signal from a current transducer.

In the original design the current transducers were supplied by the same voltage supply as in the rest of the system, see Figure 6.8. The voltage supply could be a possible source that affects the measurement. The suggestion is to have a separate supplies for the current transducers to avoid the disturbance and hopefully get a better result.

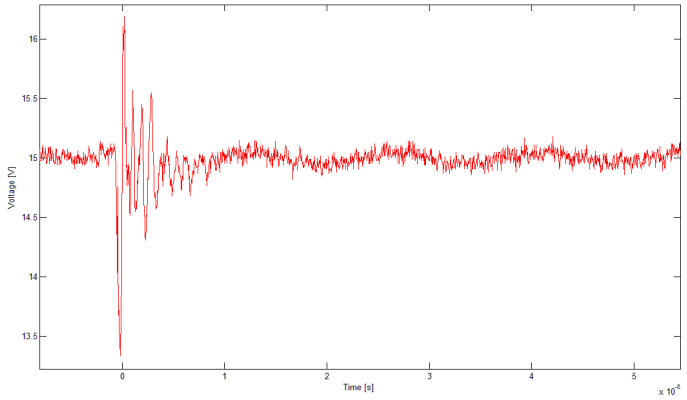

Figure 6.8: Disturbance on the 15V voltage supply.

One of the current transducers was connected to another voltage supply to minimize the disturbance. The measurement signal was also twisted and shielded. The result of this can be seen in Figure 6.9 and can be compared with the old one in Figure 6.7. The time scales have not the same proportions but the y-axis have the same values and is the one of interest. The measurement signal has improved a lot but is still not good enough because of its high transients that corresponds to tens of amperes.

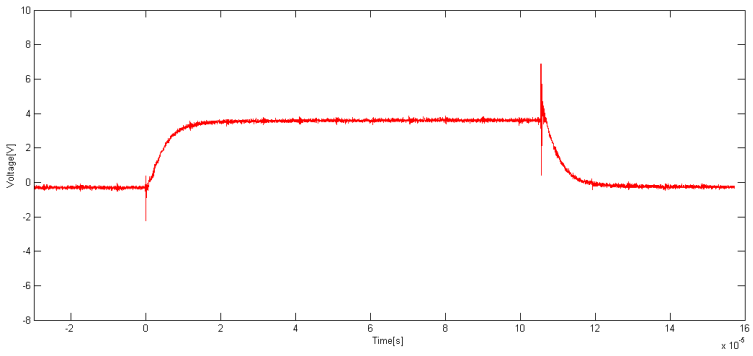

Figure 6.9: Current measurement after modifications.

One suggestion of a source of measurement error could be the long cables used in the prototype of the inverter box. The result could be that the transducer are not able to provide enough current on the output signal when a fast change in current the on phases occurs.

It is important to obtain a good signal in consideration of fault detection and the control of the current. It is unacceptable with too large disturbances on the output signal because the current has to be controlled in an electrical machine.

Chapter 7

Improvements of the construction and future work

In this chapter a discussion about what to think of during the construction and commissioning processes will be done. Some ideas of improvement of the prototype as well as suggestions for further testing will also be presented.

7.1 Improvements

There is in the existing prototype of the inverter a major problem to measure the current. The current transducers are very sensitive when it comes to disturbances on the voltage supply. Due to fast voltage and current derivatives from the switching, disturbances are induced in the 15V system. The signal from the current transducer can be seen in Figure 6.7 and the voltage supply is seen in Figure 6.8.

To be able to use the current transducers for measuring the current the system has to be rebuilt. The transducers need a separate voltage supply. The cables can be shortened and twisted. One further suggestion is to shield the cables from the electromagnetic field of the current conductors with a metal plate. It can also be worth testing if it is better to replace the existing transducers with ones with current output, that not are affected of the electromagnetic field, see section 2.6.

For further use of the prototype of the inverter the cables for connection to the control circuit card have to be replaced with another solution than ribbon cables. The ribbon cables caused extensive problems during the commissioning and the evaluation process. This because those are located on the control circuit card and the ribbon cables have to be removed every time the control circuit

card or the driver circuit card has to be removed for adjustments, see Figure 7.1 and Figure 3.5.

Figure 7.1: A typical cable breakdown

7.2 Future work

An important characteristic of an inverter is the EMC/EMI aspect. It is important to have control of how the fast switching affects the rest of the electric system in the vehicle, such as a 24V DC system. How much of the high frequency content, distributed by the inverter, passes through the 700V system to a 24V DC/DC converter? Is it possible to improve the situation with snubber circuits or is an EMI filter a possible solution to get satisfying characteristics of the system?

It is not only the EMI disturbance to other systems to take care of when designing an inverter. The components inside the inverter box has to be able to work in a closed environment without radiating to much and not to disturb the other components. It is important to consider this when selecting components and when making the packing layout. The radiation from the inverter box into the surroundings is another subject to consider, especially for a military vehicle were invisibility is of major importance.

The packaging layout in consideration to the temperature aspect is also an important factor. There is a trade off between the size and the temperature. A more compact design contributes to a rise in the temperature inside the inverter box. Further calculations and investigations have to be done to assure that the power losses together with cooling and packaging layout will fulfil the determined requirements with respect to temperature.

In a high voltage DC systems all parts, such as generators and inverters, normally contains DC capacitors. It could be a good idea to evaluate if it is possible to take advantage of the capacitors in the system not to over-dimension the amount of capacitors in each part of the system.

In thought of the physical size of the DC capacitors there may be an idea to split the capacitor bank in to many small units for a more compact design. Is it

possible to combine different types of capacitors to benefit the best qualities from each type? Could the advantages of metalized polypropylene capacitors, that has the advantages of high frequency characteristics and high current immunity, be combined with electrolytic capacitors that has high permittivity? [6]

Advancements are made in consideration of silicon structures for semiconductors. A relatively new material for IGBT modules called silicon carbide has lately been frequently discussed in articles about power electronics. The advantage of this material is a higher durability of temperature. Could this material be of interest when designing military products?

Chapter 8

Conclusions

The most important experience from the commissioning and evaluation process is that everything that has to be done in the laboratory is time demanding. Problems that at first sight do not seem to be hard to solve easily require many hours of fault detection. A small error as a too loose tightened clamping sleeve resulted in some extra days of fault detection and correction. A conclusion that can be made is: if you want to have a report written fast, keep away from the laboratory!

It is of great importance to test each component alone to assure correct function before connecting the components together. It is also important not to take for granted that all outputs on for example the driver circuit card are working correctly when only one is tested and evaluated. One small error can contribute to hazardous situation in case of a short circuit of the DC bus. The DC bus capacitors hold enough charge to blow up the metal case of the inverter. When modifications are made an evaluation of the system at low voltage has to be done on routine to assure proper function before charging the capacitors with a high DC voltage.

Simulations are useful when it comes to studying switching behaviour but keep the simulation model as simple as possible. Do not trust the simulation results blindly. A simulation tool like Pspice requires a good understanding of the system before it becomes useful.

From the simulations and measurements it is clearly shown that the RCD clamp snubber circuit have a favourable affect on transients and oscillations and also the possibility to reduce the power loss in the IGBT module. The charge restricted decoupling capacitor showed just as good result as the RCD clamp circuit in the simulations but worse results from measurements. No clear reason for this difference has been found. The most common snubber solution, a decoupling capacitor gives the same overshoot protection as the more complex solutions. The disadvantage with this solution is that it has the tendency to cause an oscillating behaviour when the oscillation energy is not consumed. Depending on the inverter design, different snubber solutions have a different impact on the switching behaviour. It has to be decided from case to case which

snubber solution that suits best for the purpose. But also if it is worth to sacrifice the extra space that the snubber components require to obtain the desired characteristics of the inverter.

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http://wwwd.national.com/national/PowerMB.nsf/(approved-attachments)/1879A8397C3BEB10882571FF0071A5DD/$File/AN-1095.pdf [2007-02-04]

Appendix A

Links to data sheets

IGBT Module - Mitsubishi CM50TL-24NF

http://www.mitsubishichips.com/Global/content/product/power/powermod/igbtmod/nf/cm50tl-24nf_e.pdf [070201]

Opto coupler - Agilent HCPL-4503

http://www.ortodoxism.ro/datasheets/hp/HCPL-0530.pdf [070201]

Driver circuit - International Rectifier IR2213

http://www.irf.com/product-info/datasheets/data/ir2213.pdf [070201]

AVR processor - Atmel ATmega8

http://www.atmel.com/dyn/resources/prod_documents/doc2486.pdf [070201]

Current transducer - LEM HAL 50S

http://www.lem.com/docs/products/hal_e.pdf [070201]

Appendix B

Pspice simulation

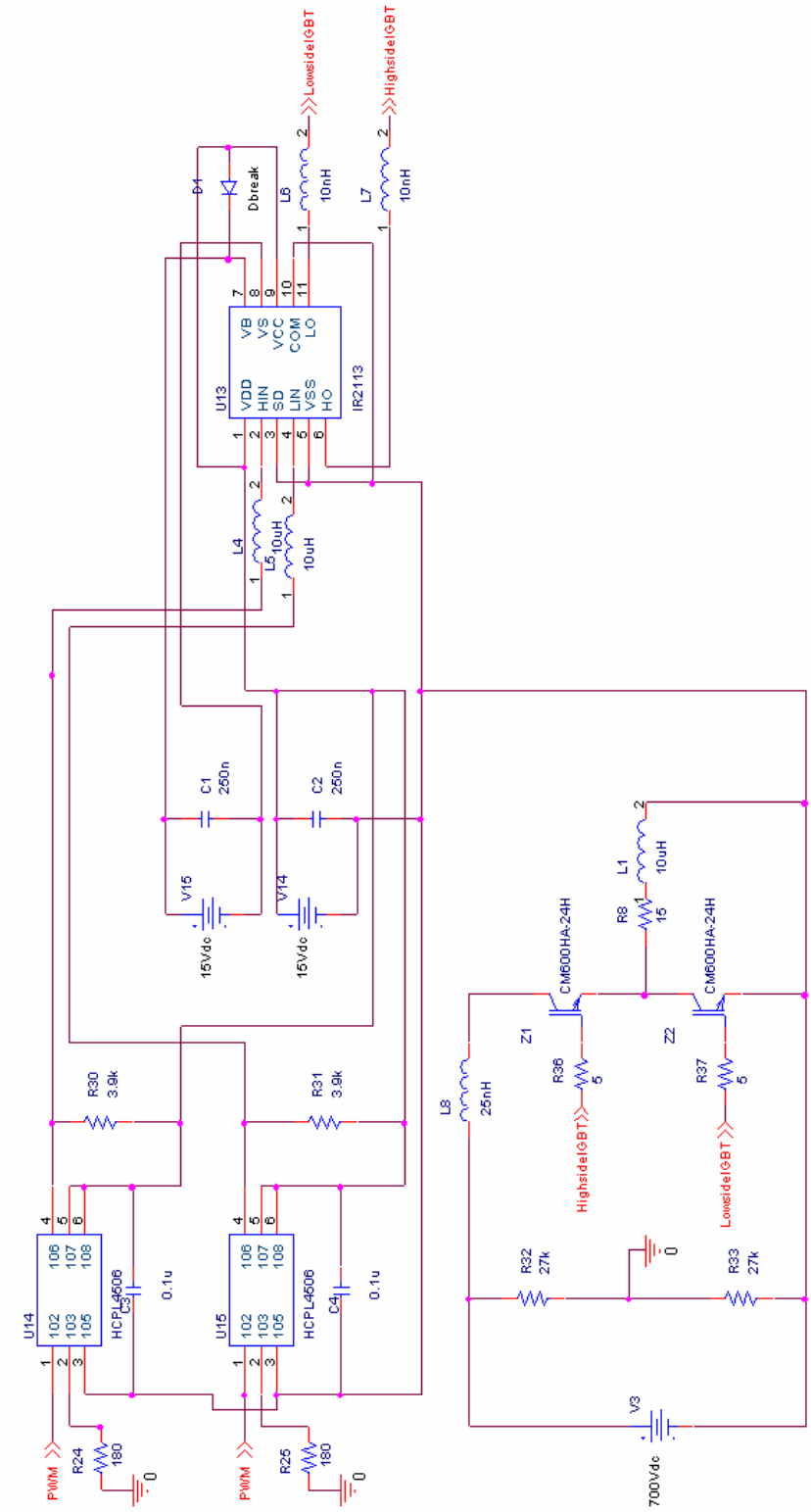

Figure B.1: A schematic layout of the Pspice simulation.

Appendix C

Circuit diagram of the driver circuit card

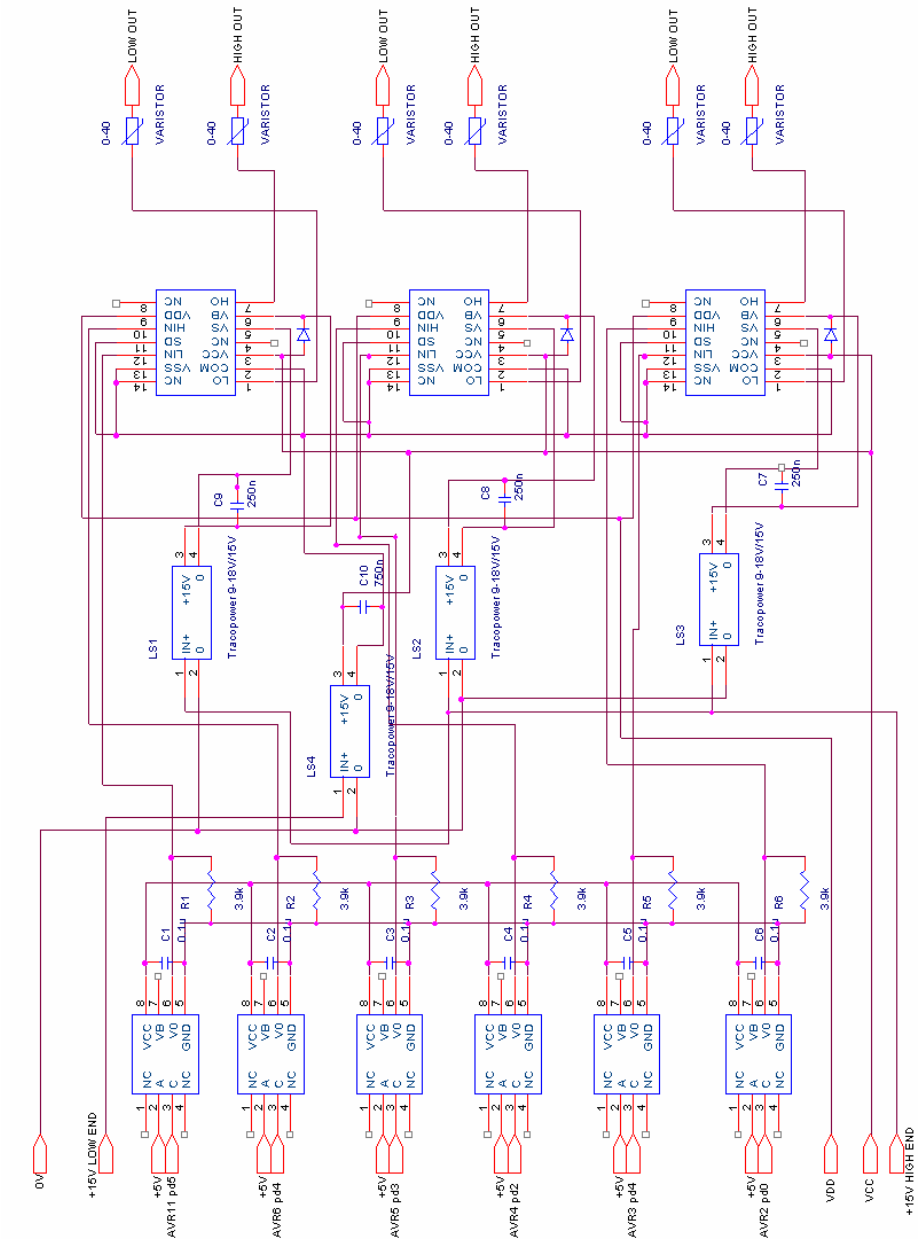

Figure C.1: Circuit diagram of the driver circuit card.

Appendix D

Circuit diagram of the voltage supply to the driver circuit card

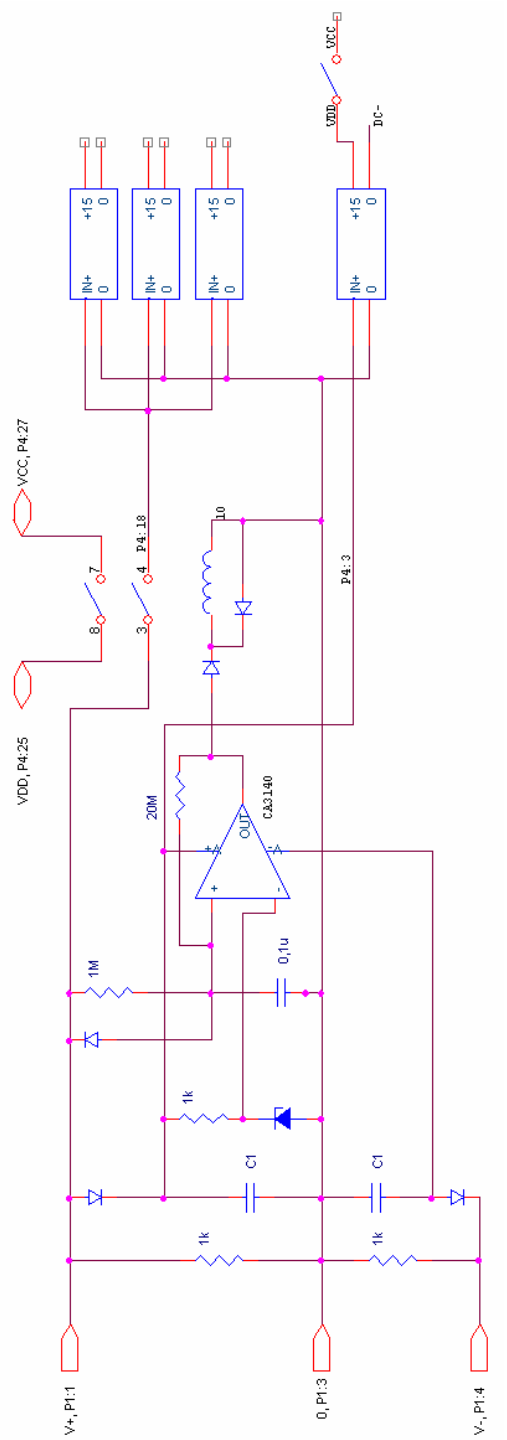

Figure D.1: Circuit diagram of the voltage supply to the driver circuit card.

Appendix E

Assembler code

```
;include files
.include "m8def.inc"
.def ud16ln=r2 ; tempreg for -Ud/16
.def ud16hn=r3 ; tempreg for -Ud/16
.def turns=r4
.def tbg1=r5 ; tempreg for background
.def tbg2=r6 ; tempreg for background
.def ud16l=r7 ; tempreg for Ud/16
.def ud16h=r8 ; tempreg for Ud/16
.def udcml=r9
.def udcmh=r10
.def pcvl=r11 ;AD control voltage
.def pcvh=r12 ;AD control voltage
.def temp1=r13 ; tempreg for main
.def temp2=r14 ; tempreg for main
.def temp=r16 ; temp register
.def tbg3=r17 ;
.def pstat=r18 ; bit status register
.def udl=r19
.def udh=r20
.def udpl=r21
.def udph=r22
.def udnl=r23
.def udnh=r24
.def tioff=r25 ;register used only in igbtoff
;*********************************************************************

.org $0000
rjmp init     ;reset handle
.org $003
rjmp igbtoff  ;jump igbtoff at timer2 output compare match
;.org $005
;rjmp main     ;jump main at timer1 input capture use for top detection
```

```
;.org $006
;rjmp ubout     ;jump ubout at timer1 compare A match
;.org $007
;rjmp ustopout  ;jump ustopout at timer1 compare B match
;.org $008
;rjmp startdelay ;jump to startdelay at timer1 overflow
.org $009
rjmp main     ;jump to main at timer0 overflow

;***********************************************************************

init:
cli     ;clear globally interupt
ldi temp,high(RAMEND)
out SPH,temp ; set stack pointer to top of RAM
ldi temp,low(RAMEND)
out SPL,temp ;
;init of port C pc0=AD input for ud+
;                pc1=AD input for ud-
;                pc2=AD input for capacitor midpoint
;  pc3=AD input from control panel
;
; DDRC=00000000
clr turns
clr pstat
ldi temp,0
out DDRC,temp
;init of AD
clr temp ; ADMUX=00000000
out ADMUX,temp ;init mux to ch. 0 with right-adjusted result,voltref=AREF
ldi temp,128
out ACSR,temp ;init analog comp switched off
ldi temp,$d7
out ADCSRA,temp ;init ad single mode with prescale 128 on clock

;init gate signals  (port D)
; phase1h = bit5
; phase1l = bit4
; phase2h = bit3
; phase2l = bit2
; phase3h = bit1
; phase3l = bit0
ldi temp,$ff
out DDRD,temp ;init port D as output
ldi temp,0
out portd,temp ;init gate signals to zero

;init of port B (pb6-7=crystal connection)
;
ldi temp,0
```

```
out DDRB,temp
;init of main routine execution number counter
mov turns,temp

; init of counter 0,2
ldi temp,4
out TCCR0,temp ; prescaler 256 for counter 0
ldi temp,5
out TCCR2,temp ; prescaler 128 for counter 2
ldi temp,1
out timsk,temp ; enable timer 0 overflow interupt
ldi temp,8
out ocr2,temp ; 64 microsecond long pulse

ldi r27,$02
ldi r28,$03  ;r27,r28 holds $340 = block level supply voltage

sei   ; enable interupt globally

;*****************************************************************
;************************start background************************

background:
;*************************************************************************************
;starting and reading of AD
sbic adcsra,6 ;check if ad ready
rjmp background
;*********************UD+ read*****************
ldi tbg3,0
out admux,tbg3 ;ad channel 0 select
ldi tbg3,$d7 ;11010111
out adcsra,tbg3 ;start new conversion
waitad0:
sbic adcsra,6 ;check if ad ready
rjmp waitad0
ldi tbg3,3
in udpl,ADCL ;
in udph,ADCH
and udph,tbg3 ;10 bit AD
;*********************UD- read*****************
ldi tbg3,1
out admux,tbg3 ;ad channel 1 select
ldi tbg3,$d7 ;11010111
out adcsra,tbg3 ;start new conversion
waitad1:
sbic adcsra,6 ;check if ad ready
rjmp waitad1
ldi tbg3,3
in udnl,ADCL ;
in udnh,ADCH
```

```
and udnh,tbg3 ;10 bit AD
;***********Capacitor mid-voltage read**********
ldi tbg3,2
out admux,tbg3 ;ad channel 2 select
ldi tbg3,$d7 ;11010111
out adcsra,tbg3 ;start new conversion
waitad2:
sbic adcsra,6 ;check if ad ready
rjmp waitad2
ldi tbg3,3
in udcml,ADCL ;
in udcmh,ADCH
and udcmh,tbg3 ;10 bit AD
;***********Panel control-voltage read**********
ldi tbg3,3
out admux,tbg3 ;ad channel 3 select
ldi tbg3,$d7 ;11010111
out adcsra,tbg3 ;start new conversion
waitad3:
in tbg1,adcsra ;check if ad ready
sbrc tbg1,6
rjmp waitad3
ldi tbg3,3
in pcvl,ADCL ;
in pcvh,ADCH
and pcvh,tbg3 ;10 bit AD

;*********** +15-voltage read for supervision**********
ldi tbg3,4
out admux,tbg3 ;ad channel 4 select
ldi tbg3,$d7 ;11010111
out adcsra,tbg3 ;start new conversion
waitad4:
in tbg1,adcsra ;check if ad ready
sbrc tbg1,6
rjmp waitad4
ldi tbg3,3
in tbg1,ADCL ;
in tbg2,ADCH
and tbg2,tbg3 ;10 bit AD
; tbg1,tbg2 holds +VCC with scale 776/13V
;block level is ~13V <-> 770 =$302
cp tbg1,r27
cpc tbg2,r28
brlo blockset
sbr pstat,4 ;set bit 2 of pstat
rjmp udcalc
blockset:
cbr pstat,4 ;clear bit 2 of pstat
```

```
;*************** Calculate ud **********
udcalc:
mov udl,udpl
mov udh,udph
add udl,udnl
adc udh,udnh

;******* evaluate earthfault*********************
mov ud16l,udl
mov ud16h,udh
lsr ud16h
ror ud16l
lsr ud16h
ror ud16l
lsr ud16h
ror ud16l
lsr ud16h
ror ud16l ;ud16l=Ud/16
clr ud16h
ldi tbg3,20
cp tbg3,ud16l
brlt nolimit
mov ud16l,tbg3
nolimit:
mov tbg1,udpl
mov tbg2,udph  ; tbg1,2 holds UDC+
sub tbg1,udnl
sbc tbg2,udnh ; tbg1,2 holds |UDC+|-|UDC-|
asr tbg2
ror tbg1 ;tbg1,2 holds udm=(|UDC+|-|UDC-|)/2
cp tbg1,ud16l
cpc tbg2,ud16h ; |UDC+|-|UDC-|-ud/16?
brlt testlow1 ;if    " <0 go to testlow
sbi portd,7 ;port d bit 7 set at earthfault
rjmp endearth
testlow1:
ldi tbg3,0
mov ud16ln,ud16l
neg ud16ln
sbc tbg3,ud16h
mov ud16hn,tbg3 ;ud16l(h)n holds -ud/16
cp tbg1,ud16ln
cpc tbg2,ud16hn
brge noearthfault ; UDC+|-|UDC-|+ud/16?
sbi portd,7 ;port d bit 7 set at earthfault
rjmp endearth
noearthfault:
cbi portd,7 ;port d bit 7 cleared at no earthfault
endearth:
```

```
;*************** evaluate capacitor fault**********

ldi tbg3,2 ;sub 2.5 V offset
sub udcmh,tbg3 ;udcm holds -udcm
add udcml,tbg1 ;tbg1,2 holds udm=(|UDC+|-|UDC-|)/2
adc udcmh,tbg2  ;udcm holds udm-udcm
cp udcml,ud16l
cpc udcmh,ud16h ; udm-udcm-ud/16?
brlt testlow ;if    " <0 go to testlow
sbi portd,6 ;port d bit 6 set at capacitorfault
rjmp endcap
testlow:
cp udcml,ud16ln
cpc udcmh,ud16hn ; udm-udcm+ud/16?
brge nocapfault ;if    " >0 no capfault
sbi portd,6 ;port d bit 6 set at capacitorfault
rjmp endcap

nocapfault:
cbi portd,6 ;port d bit 6 cleared at no capacitorfault
endcap:


rjmp background

;*********************end background*******************************


;******************start main interupt*****************************

;4096 us interupt (16 MHz/256 input, cont0 is counting 256, input capture irq)
main:
inc turns   ;increment program turn counter
ldi temp,$ff
cp turns,temp
brne cont1
sbr pstat,1 ;set bit 0 of pstat if 256 turns occured since cleared
cont1:
sbrs pstat,0  ;skip push detect if bit 0 of pstat cleared
rjmp cont2
sbrc pstat,2  ;block if bit 2 of pstat cleared
rjmp pushdet
in temp,portd
andi temp,$c0 ;clear all bits except pd6,pd7
out portd,temp ;block all igbts
rjmp cont2
;*****************detection of push button**************
pushdet:
```

```
sbis pinb,3 ; skip push detect if bit 3 of port b cleared
rjmp cont2
in temp,pinb; read position to be pulsed (pb0 - pb2, 0-5)
andi temp,7;
ldi r26,0
mov temp1,r26
ldi r26,1
loop1:
inc temp1  ;first value = 1
cp temp,temp1 ;if pinb=0
brlo setpos ;go to setpos directly (tbg3=00000001)
lsl r26
rjmp loop1
setpos:
in temp,portd
andi temp,$c0 ;clear all bits except pd6,pd7
or temp,r26
out portd,temp; set read position high (pos 0-5)
mov temp,pcvl
mov temp1,pcvh ; temp= panel pot voltage 0-1023
lsr temp1
ror temp
lsr temp1
ror temp   ;temp= panel pot voltage 0-255
cpi temp,1
brge pulselength
ldi temp,1
pulselength:
out ocr2,temp ; pulselength = temp*8 micros
in temp,sfior
ori temp,2
out sfior,temp ;clear counter 2 prescaler
ldi temp,0
out tcnt2,temp ;clear counter 2
in temp,tifr
ori temp,$80
out tifr,temp ;clear ocf2 flag by writing 1 to TIFR bit 7
ldi temp,$81
out timsk,temp ;enable counter 2 output compare interupt
cont2:
reti
igbtoff:
in tioff,portd
andi tioff,$c0 ;clear all bits except pd6,pd7
out portd,tioff ;shut off all igbt
cbr pstat,1 ;clear bit 0 of pstat
ldi tioff,1
out timsk,tioff ;disable counter 2 output compare interupt
reti
```