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Industrial Electrical Engineering and Automation

Auxiliary Module for Unbalanced Three Phase Loads with a Neutral Connection

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Abstract

The company *Land Systems Hägglunds AB* is a leading manufacturer of combat vehicles and all terrain vehicles. One of Land systems Hägglunds projects for the future is the multi purpose combat vehicle, SEP, using a hybrid diesel-electrical drive train. Because of the diesel-electrical drive train, all the mechanical power produced by the diesel engines is transformed into electricity. The electrical system of the vehicle is by that dimensioned for high electrical power. This power could be used, besides for traction of the vehicle, for numerous purposes. For example external electrical tools, motors, PC:s, radios, radar equipment etc.

To make the electrical power useful for an arbitrary load, it needs to be transformed into a four wire three-phase 230/400V 50Hz AC system, using the dc-link voltage of the SEP as raw material. Ideally, the three phase system should act similar to an ordinary connection to the main electric grid. The purpose of the thesis is to examine the possibility to achieve this by using a 50 kVA DC/AC power electronic converter with four half bridges, providing three phase terminals and one neutral terminal. The converter is called *ACM (Auxiliary Converter Module)*

The thesis deals in a structured way with the problems and issues concerning design of the converter and especially its control. Effects of unbalanced three phase loads, voltages and currents, in a four wire system, are highlighted. It covers theory of three-phase systems and their representation in phasors, sequences and vectors. The vectors are presented in stationary (α - β -γ) and rotating (d-q-0) coordinate systems. It also covers the theory of pulse-width modulation as well as circuit models and design methods for vector control in rotating d-q-0-coordinates. Dimensioning aspects of main physical components and loss calculations of the semiconductors are covered but not highlighted. Finally some issues concerning the implementation of a digital control are dealt with.

A model of the designed converter, including control systems, is built in Matlab/Simulink. The model contains the important aspects of a physical converter. Specified load scenarios are simulated and the results are presented.

Acknowledgements

First we would like to thank our supervisor Per Karlsson for his advice, expertise and support. We also want to thank our examiner Mats Alaküla for, during the years, strongly contributing to our interests in power electronics. Anders Robertsson (department of Automatic Control, LTH) has also been very helpful to us in our work. The people we were connected with at Land Systems Hägglunds deserve a special appreciation for providing a nice and friendly working environment. Especially Örjan Sjöström, Urban Lundgren, Svante Bylund and Lars-Gunnar Larsson. Finally we want to thank our families for their support during our years of studies at Lund Institute of Technology, LTH.

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Contents

1. Introduction

1.1 Background

The company *Land Systems Hägglunds AB* is a leading manufacturer of combat vehicles and all terrain vehicles. Hägglunds has delivered military vehicles to more than 40 countries worldwide. The company is situated in Örnsköldsvik, a town 550 km north of Stockholm. Land Systems Hägglunds employs around 1100 personnel and had in 2004 a turnover of 3 billion Swedish kronor.

One of Land systems Hägglunds projects for the future is the multi purpose combat vehicle SEP (Swedish abbreviation for "*Splitterskyddad Enhets Plattform*", Modular Armoured Tactical System). The interesting part of SEP from this thesis point of view, is the fact that SEP utilizes a hybrid diesel-electrical drive train (see fig. 1.1-1). From a vehicle point of view this gives advantages like: volume efficiency, fuel efficiency, reduced life cycle costs, reduced environmental impact and increased stealth characteristics. Since the diesel engines are decoupled from the final drives, an increased flexibility in placing of the systems in the vehicle is achieved, as well as an easily installation of two smaller diesel engines instead of one larger. With batteries integrated into the electric drive system, the vehicle is also allowed to be driven silently, with the diesel engines shut down.

There is however a further advantage with the hybrid diesel-electrical drive train. All the mechanical power produced by the diesel engines is transformed into electrical power by generators and rectified before it is transformed back to mechanical power by electrical machines. The central part of this electric transmission is the dc-link and it is here the basic possibility for the purpose of this thesis is provided. Since the generators and the dc-link are dimensioned for the full traction power of the vehicle, they create a possibility of supplying external loads with high power, to the cost of less traction power, at for example stand still of the vehicle. The structure of the drive train of the SEP may be simplified as a diesel-electric UPS (Uninterruptible Power Supply) that feeds the electrical traction motors. If only the first parts of the drive train are considered, the SEP is an UPS.

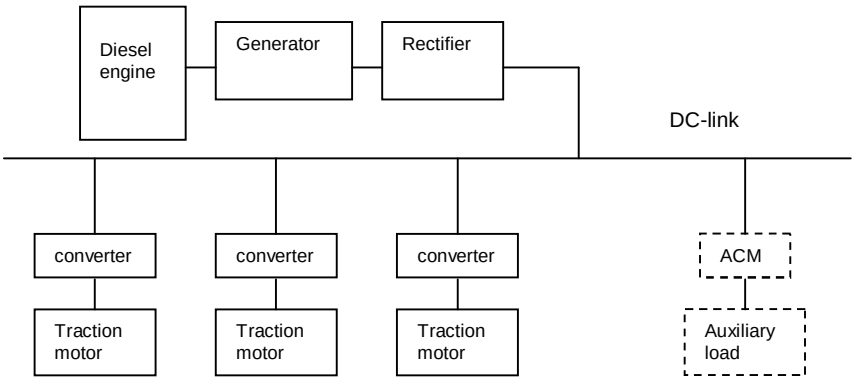


Figure 1.1-1. Principle diagram of the drive train of SEP.

1.2 Problem

Since the possibility of using the vehicle as an UPS is given, the extension of the usefulness of the SEP it would provide is an advantage that not should be foreseen. Possible loads for the SEP, partly working as an UPS, could be different kinds of internal or external electrical systems and machines, for example electrical tools, motors, PC:s, radios, radar equipment etc.

To make the electrical power useful for an arbitrary load, it needs to be transformed from DC level of the vehicle to a three-phase four-wire 230/400V 50 Hz AC system. To get the most out of the three phase system it should be flexible and stable enough to regulate the output voltage correctly during any load (single-phase load, two-phase load, three-phase load or combinations) less than, or equal to nominal load. The ideal case would be if the three-phase connection could be seen as an ordinary connection to the main grid. This forms the need of three line output terminals and one neutral output terminal, as well as a tight control system for the equipment performing the transformation.

1.3 Purpose

The purpose of this thesis is to examine the possibilities of transforming the dc-link voltage in the vehicle to a four-wire three-phase 230/400V 50 Hz AC system by utilization of a power electronic converter. The converter is from now on referred to as the *ACM (Auxiliary Converter Module).* This is done by studying existing theory, examine different alternative solutions, building a model, performing

simulations on the model and examine the results. The dimensioning process of the main physical components of the converter is also explained.

For this purpose, one need to investigate the effects of unbalanced three phase loads, how the unbalance affects the voltage regulation, and what countermeasures may be used to reduce their impacts. Understanding of the design process of power electronic converters and their control methods, as well as the behavior and representations of unbalanced three phase systems, are therefore needed.

The main objective of the thesis is to provide this understanding.

1.4 Delimitation

Due to the always present lack of time and resources, one has to put limitations to the scope of a work. The theory needed for the understanding of the effects, design, model building etc., mentioned in the section above, is covered. Some limiting simplifications are however made in the model and the simulations:

In the model of the converter the dc link voltage is assumed to be ideal. The voltage is not affected by the load connected to the converter or other loads or sources connected to the dc link. Probably there will be a need for some kind of step-up converter with voltage regulation between the dc link of the vehicle and the dc-link used by the converter described in this thesis.

There are only simulations performed with balanced and unbalanced, resistive and inductive loads connected to the converter.

The control systems of the converter are simulated in Matlab and Simulink. Little is covered about the implementation of the control system in software for a real converter (for example C-code for a DSP).

The project is purely theoretical. The construction of a physical converter is not the target of the project. The most obvious limitation is the lack of a prototype of a physical converter for practical tests and verifications of the results obtained from simulations.

1.5 Outline

The ambition of the thesis is to treat, in a structured way, the problems and issues concerning the design of a power electronic converter, working as a provider of a three phase voltage source. The structured outline involves passing through some theory in the first sections of the thesis that the later sections are depending on. The aim is to present the contents of the thesis in a pedagogical and logical order. The content is now presented in short:

Chapter 1 is the introduction.

Chapter 2 handles the theory and is the major part of the thesis. Section 2.1 concerns the basic theory of three-phase systems, unbalanced voltages and currents, and how to represent them. In section 2.2 different load scenarios and their impacts on the converter are presented. Section 2.3 deals with the basic theory of ordinary three phase converters with three half-bridges and their limitations. Section 2.4 expands the three half-bridge converter with a fourth half-bridge to achieve a four legged converter with a neutral connection. In section 2.5 circuit models of the whole converter, including filters and loads, are presented. Section 2.6 deals with dimensioning issues, for example dc-link voltage, switches, switching frequencies and filters. Section 2.7 finally presents a structured method for the design of the control systems for the converter.

Chapter 3 presents a simulation model of the converter. In section 3.1 the construction of the model, built in Matlab and Simulink is thoroughly explained. In section 3.2 the simulation scenarios, based on the load scenarios from section 2.2, are presented.

Chapter 4 gives a presentation of the results from the simulations in chapter 3.

Chapter 5 concerns implementation of a physical converter. Section 5.1 covers some issues concerning a digital control. Section 5.2 gives a suggestion of what hardware to use.

Chapter 6 is an evaluation of the project, as well as a discussion for the future.

2. Theory

2.1 Three-phase systems

The project concerns the transformation of the available DC-link voltage to a three-phase 400V AC voltage, including a neutral connection. Commonly used subjects in the thesis are for example: phase representation, sequence representation, vector representation, definition of power, Y- and Δ-connections and unbalanced voltages and currents. To clarify the methods and concepts, the thesis is opened with a section providing the theory of the above mentioned subjects in short.

2.1.1 Three-phase systems in phasor representation

In a three phase system, the three phases are denoted a, b, and c. The frequency *f* is the same in all three phases. During ideal conditions, the phase components are distributed by 120° and their amplitudes are equal. If phase a is taken as reference, phase b lags 120° behind phase a. The phasors rotate counterclockwise.

In an ideal situation (like above), the three phase system has equal amplitudes in all three phases and exactly 120° phase distribution. The system is then called *symmetric* or *balanced*.

$$\begin{cases} v_a(t) = \hat{V}_a \cos(2pf \cdot t) \\ v_b(t) = \hat{V}_b \cos(2pf \cdot t - 2p/3) \\ v_c(t) = \hat{V}_c \cos(2pf \cdot t - 4p/3) \end{cases}$$ Equation 2.1.1

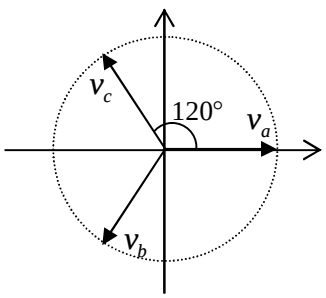


Figure 2.1-1. Phasor diagram of three-phase system.

2.1.2 Three-phase systems in sequense representation

When phase b lags 120° behind phase a, as in eq. 2.1.1, the system is said to have a *positive sequence*. If the rule of ordering the phases in section 2.1.1 is not followed and phase b is taken as the phase lagging 240° behind phase a:

$$\begin{cases} v_a(t) = \hat{V}_a \cos(2pf \cdot t) \\ v_b(t) = \hat{V}_b \cos(2pf \cdot t - 4p/3) \\ v_c(t) = \hat{V}_c \cos(2pf \cdot t - 2p/3) \end{cases} \qquad \text{Equation 2.1.2}$$

the system is said to have a *negative sequence*. Positive and negative sequence can be visualized as rotating counterclockwise and clockwise, respectively.

An important property of a three phase system with *only* positive sequence, negative sequence, or a sum of both, is that the instantaneous sum of the phase components is zero.

$$v_a(t) + v_b(t) + v_c(t) = 0 \qquad \text{Equation 2.1.3}$$

If eq. 2.1.3 *not* holds, the mean value:

$$v_0 = \frac{v_a(t) + v_b(t) + v_c(t)}{3} \qquad \text{Equation 2.1.4}$$

is called the *zero sequence* component. The zero sequence component v_0 represents a un-symmetry component which is the same in all three phases.
As long as there is no neutral conductor in a three phase system (a three wire system), no zero sequence current is possible. However, in a four wire system the possibility of zero sequence currents exists.

Finally: An un-symmetric, or unbalanced, three phase system can be decomposed into a *positive sequence component*, a *negative sequence component* and a *zero sequence component*:

$$\begin{bmatrix} v_a(t) \\ v_b(t) \\ v_c(t) \end{bmatrix} = \begin{bmatrix} \hat{V}_a \cos(2pf \cdot t + r_a) \\ \hat{V}_b \cos(2pf \cdot t + r_b) \\ \hat{V}_c \cos(2pf \cdot t + r_c) \end{bmatrix} = \begin{bmatrix} \hat{V}_p \cos(2pf \cdot t) \\ \hat{V}_p \cos(2pf \cdot t - 2p/3) \\ \hat{V}_p \cos(2pf \cdot t - 4p/3) \end{bmatrix} + \begin{bmatrix} \hat{V}_n \cos(2pf \cdot t) \\ \hat{V}_n \cos(2pf \cdot t - 4p/3) \\ \hat{V}_n \cos(2pf \cdot t - 2p/3) \end{bmatrix} + \begin{bmatrix} v_0(t) \\ v_0(t) \\ v_0(t) \end{bmatrix}$$

Equation 2.1.5

Where:

$$v_0(t) = \hat{V}_0 \cos(2pf \cdot t + r_0) = \frac{v_a(t) + v_b(t) + v_c(t)}{3}$$ Equation 2.1.6

The decomposition in eq. 2.1.5 is visualized in fig. 2.1-2.

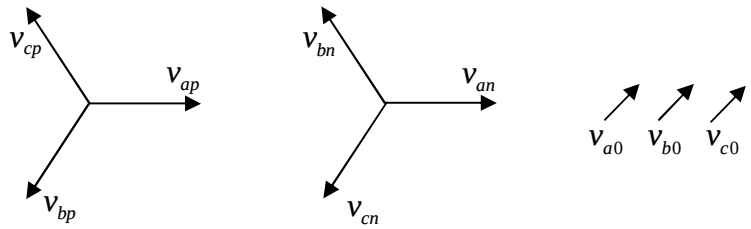


Figure 2.1-2. Visualization of decomposition in sequences. Positive sequence (left), negative sequence (center), zero sequence (right).

The transformation between a-b-c components and sequence components is expressed in eq. 2.1.7 and eq. 2.1.8. [2]

$$\begin{bmatrix} X_p \\ X_n \\ X_0 \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & a & a^2 \\ 1 & a^2 & a \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} X_a \\ X_b \\ X_c \end{bmatrix}$$ Equation 2.1.7

$$\begin{bmatrix} X_a \\ X_b \\ X_c \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ a^2 & a & 1 \\ a & a^2 & 1 \end{bmatrix} \begin{bmatrix} X_p \\ X_n \\ X_0 \end{bmatrix}$$ Equation 2.1.8

Where X may be voltages or currents and $a = e^{j2p/3}$ is a displacement with 120°.

2.1.3 Y- and Δ-connections

A tree phase load consisting of three impedances (Z_1, Z_2, Z_3) can be connected in a Y or in a Δ, as shown in fig. 2.1-3. Assuming balanced load ($Z_1=Z_2=Z_3$), the voltages can be illustrated as the phasor diagram in fig. 2.1-3 (right).

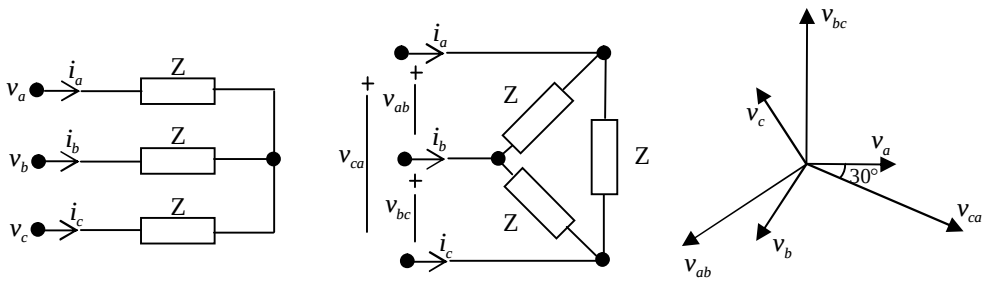


Figure 2.1-3. Three phase loads. Y connection (left), Δ connection, (center), Phasor diagram Y and Δ (right).

From the geometry of fig. 2.1-3 (right) it is seen that, compared with the line to neutral voltages (or currents), the line to line voltages (or currents) have their peak values a factor $\sqrt{3}$ higher and their arguments displaced by 30°. Because of this the total power developed in a three phase load is decreased by a factor 3 when changing the connection from Δ to Y. In the following equations U_{load} is the voltage over *one* of the impedances Z.

Conclusions Y-connection

$$U_{load} = U_{line-neutral} = U_{line-line} \cdot 1/\sqrt{3}$$

$$I_{load} = I_{line}$$ Equation 2.1.9

$$P_Y = 3 \cdot U_{load} \cdot I_{load} \cdot \cos r = \frac{(U_{line-line})^2}{|Z|} \cdot \cos r$$

Conclusions Δ-connection

$$U_{load} = U_{line-line}$$

$$I_{load} = I_{line} \cdot 1/\sqrt{3}$$ Equation 2.1.10

$$P_\Delta = 3 \cdot U_{load} \cdot I_{load} \cdot \cos r = 3 \cdot \frac{(U_{line-line})^2}{|Z|} \cdot \cos r$$

Equivalent Y

During balanced loads, it is of no concern, from the standpoints of dynamics and control, if the load is connected in Y or Δ. A Δ connected load can be treated as if it were connected in a Y, but with all the impedances reduced to1/3 of the actual values. This is called an *equivalent Y.* [1]

2.1.4 Three-phase systems in vector representation in fixed coordinates

The system expressed as a vector in two dimensions

Assuming a balanced three phase three-wire system, following equation holds [2]:

$$X_a(t) + X_b(t) + X_c(t) = 0. \qquad \text{Equation 2.1.11}$$

Where X may be voltages or currents.

This means that the system is over-determined and that one of the components always can be expressed in the other two. Therefore it's possible to describe the system as equivalent two phase system, with two perpendicular axes, denoted as a and b . These axes are considered to be the real and imaginary axes in a complex plane. The two components, a and b forms a vector $\overline{X}_{ab}(t)$. The three phase/two phase transformation is given by eq. 2.1.12:

$$\overline{X}_{ab}(t) = X_a(t) + jX_b(t) = \frac{2}{3}\left[X_a(t) + e^{j2p/3}X_b(t) + e^{j4p/3}X_c(t)\right]$$

Equation 2.1.12

Fig. 2.1-4 shows the construction of the vector in a - b -coordinates graphically.

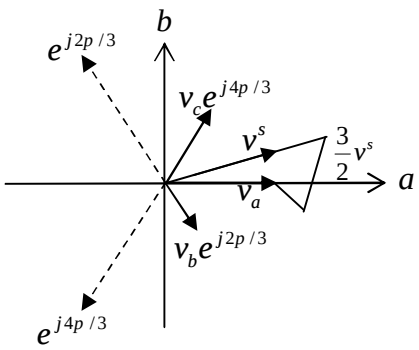


Figure 2.1-4. Construction of the vector in alpha-beta-coordinates.

The transformation between a-b-c coordinates and a - b coordinates is expressed in eq. 2.1.13 and 2.1.14.

$$\begin{bmatrix} X_a(t) \\ X_b(t) \end{bmatrix} = \underbrace{\begin{bmatrix} 2/3 & -1/3 & -1/3 \\ 0 & 1/\sqrt{3} & -1/\sqrt{3} \end{bmatrix}}_{T_1} \begin{bmatrix} X_a(t) \\ X_b(t) \\ X_c(t) \end{bmatrix} \qquad \text{Equation 2.1.13}$$

$$\begin{bmatrix} X_a(t) \\ X_b(t) \\ X_c(t) \end{bmatrix} = \underbrace{\begin{bmatrix} 1 & 0 \\ -1/2 & \sqrt{3}/2 \\ -1/2 & -\sqrt{3}/2 \end{bmatrix}}_{T_1^{-1}} \begin{bmatrix} X_a(t) \\ X_b(t) \end{bmatrix} \qquad \text{Equation 2.1.14}$$

The system expressed as a vector in three dimensions.

When the three wire system above is extended with a forth neutral wire, the possibility of a zero sequence load current is given. Because of this eq. 1.1.11 does *not* necessarily hold [2].

$$X_a(t) + X_b(t) + X_c(t) \neq 0 \qquad \text{Equation 2.1.15}$$

This means that the systems components are truly independent variables and could not be mapped into a two dimensional vector. Instead a *three dimensional* vector, in a three dimensional space with the orthogonal a - b - g -coordinates is used.

$$\overline{X}_{abg}(t) = X_a(t) + jX_b(t) + kX_g(t) \qquad \text{Equation 2.1.16}$$

Fig. 2.1-5 demonstrates how the three phasors in a-b-c may relate to the a - b - g - coordinate system.

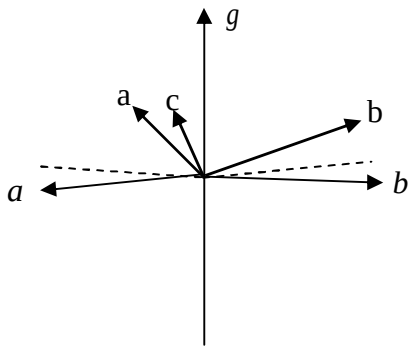


Figure 2.1-5. Relationship between the phasors in a-b-c and the alpha- beta-gamma-coordinate system.

The transformations between a-b-c coordinates and a - b -g -coordinates are expressed in eq. 2.1.17 and 2.1.18.

$$\begin{bmatrix} X_a(t) \\ X_b(t) \\ X_g(t) \end{bmatrix} = \underbrace{\frac{2}{3}\begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \\ 1/2 & 1/2 & 1/2 \end{bmatrix}}_{T_2} \begin{bmatrix} X_a(t) \\ X_b(t) \\ X_c(t) \end{bmatrix} \qquad \text{Equation 2.1.17}$$

$$\begin{bmatrix} X_a(t) \\ X_b(t) \\ X_c(t) \end{bmatrix} = \underbrace{\begin{bmatrix} 1 & 0 & 1 \\ -1/2 & \sqrt{3}/2 & 1 \\ -1/2 & -\sqrt{3}/2 & 1 \end{bmatrix}}_{T_2^{-1}} \begin{bmatrix} X_a(t) \\ X_b(t) \\ X_g(t) \end{bmatrix} \qquad \text{Equation 2.1.18}$$

2.1.5 Vector representation in synchronous coordinates

In a system, during steady state, the vector representations above would both be rotating in their a - b or a - b -g -coordinate systems. The controllers for such a system would have constantly oscillating reference signals even at steady state, which would lead to stationary errors in the output signals [2].

To avoid this problem and achieve a stationary DC operating point at steady state (at least in a balanced system, which will be discussed later), the system is transformed into the rotating d-q- or d-q-0-coordinate system. The d-q- or d-q-0-transformation can be regarded as an observation of the rotating vector from a coordinates system that rotates with the same frequency as the fundamental frequency of the vector in the a - b -plane. Since the a - b to d-q transformation

just is a simplification of the a -b -g to d-q-o transformation, only the latter will be dealt with here.

Fig. 2.1-6 demonstrates how the fixed coordinate system in a -b -g relates to the rotating coordinate system in d-q-0. As can be seen, the d and q axes rotate on the a -b plane, while the o axis essentially is the preserved g axis.

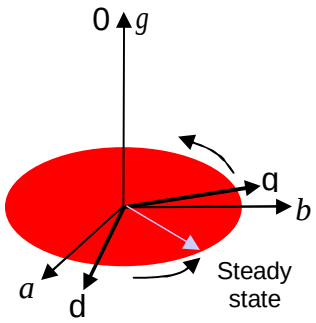


Figure 2.1-6. Relationship between the alpha-beta-gamma- and d-q-o-coordinates.

The transformation from a -b -g -coordinates to d-q-0-coordinates is expressed in eq. 2.1.19.

$$\begin{bmatrix} X_d(t) \\ X_q(t) \\ X_0(t) \end{bmatrix} = \underbrace{\begin{bmatrix} \cos(wt) & \sin(wt) & 0 \\ -\sin(wt) & \cos(wt) & 0 \\ 0 & 0 & 1 \end{bmatrix}}_{T_3} \begin{bmatrix} X_a(t) \\ X_b(t) \\ X_g(t) \end{bmatrix} \qquad \text{Equation 2.1.19}$$

Physically, for a vector in the d-q-0-coordinates, the d-component is the reactive component and the q-component is the active component (voltage or current).

Direct transformation a-b-c to d-q-o

Later, in models and simulations, transformations will be made directly from phasor representation in a-b-c to vector representation in d-q-0. This is done by combining T_2 and T_3 , expressed in eq. 2.1.20 and eq. 2.1.21.

$$\begin{bmatrix} X_d(t) \\ X_q(t) \\ X_0(t) \end{bmatrix} = \underbrace{\frac{2}{3}\begin{bmatrix} \cos(wt) & \cos(wt-\frac{2p}{3}) & \cos(wt+\frac{2p}{3}) \\ -\sin(wt) & -\sin(wt-\frac{2p}{3}) & -\sin(wt+\frac{2p}{3}) \\ 1/2 & 1/2 & 1/2 \end{bmatrix}}_{T_4} \begin{bmatrix} X_a(t) \\ X_b(t) \\ X_c(t) \end{bmatrix}$$

Equation 2.1.20

$$\begin{bmatrix} X_a(t) \\ X_b(t) \\ X_c(t) \end{bmatrix} = \underbrace{\begin{bmatrix} \cos(wt) & -\sin(wt) & 1 \\ \cos(wt-\frac{2p}{3}) & -\sin(wt-\frac{2p}{3}) & 1 \\ \cos(wt+\frac{2p}{3}) & -\sin(wt+\frac{2p}{3}) & 1 \end{bmatrix}}_{T_4^{-1}} \begin{bmatrix} X_d(t) \\ X_q(t) \\ X_0(t) \end{bmatrix}$$

Equation 2.1.21

2.1.6 Unbalanced system

In most cases a converter is designed under the assumption that the load is balanced and an unbalanced load is treated as an abnormal condition. However, in the real world, as well as in the proposed use for the converter in this project, unbalanced loads are expected. Unbalanced loads will result in unbalanced load currents, which in turn, with insufficient control, may cause unbalanced output voltages [2].

Since the load conditions have impacts on the performance and design of the converter, it will now be shown how unbalance appears and behave in different representations, as well as how unbalance can be defined.

Unbalance in a-b-c phase representation

Compared to what was said in section 2.1.1, unbalance or asymmetry in phase representation is characterized by phasors with different peak values and/or phase distributions different from 120°. An example of unbalanced phase voltages and phasors is shown in fig. 2.1-7. Compare with fig 2.1-1.

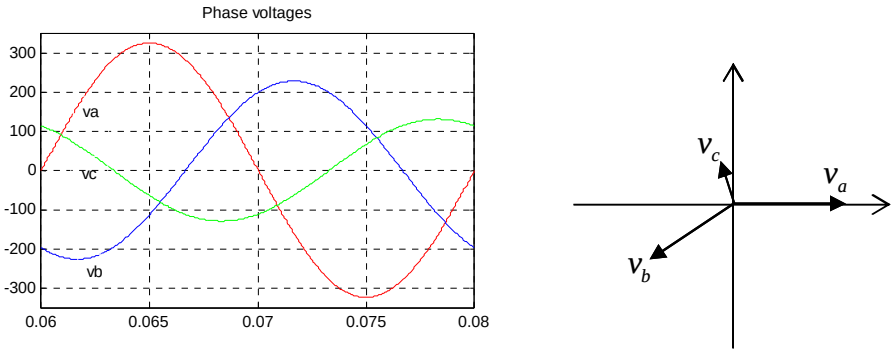


Figure 2.1-7. Phase voltages (left) and phasor diagram (right) of a three-phase unsymmetrical system.

Unbalance in sequence representation

According to section 2.1.2, unbalance or asymmetry will in sequence representation lead to the appearance of negative and/or zero sequences. As an example the phase voltages in fig. 2.1-7 can be split up in a positive, a negative and a zero sequence according to fig. 2.1-8.

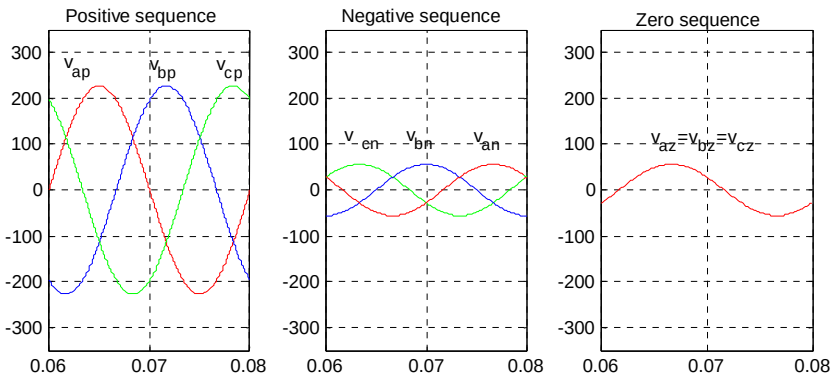


Figure 2.1-8. Visualization of decomposition in sequences.

Unbalance in α - β - γ -coordinate vector representation

During balanced conditions, the vector described in section 2.1.4, will rotate circularly on the α - β plane. No movement will appear in the γ -direction. Fig. 2.1-9a shows the vector trajectory during balanced conditions. Compare it with the sequence representation, where only the positive sequence exists.

During unbalanced conditions however, if there is a negative sequence, the backwards rotating negative sequence component will be added to the vector as well. The vector will then consist of two components: One part rotating with the fundamental frequency in the positive direction and one superimposed part rotating

with the fundamental frequency in the negative direction. This will result in an ellipsoidal vector trajectory on the a - b plane. If there is a zero sequence component, this will appear as a movement with the fundamental frequency in the g -direction. Fig 2.1-9b shows the vector trajectory during unbalanced conditions, assuming that positive, negative, and zero sequences exist. Compare it with the sequence representation during unbalance.

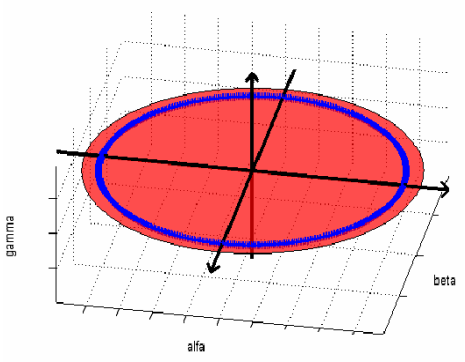


Figure 2.1-9a. Vector trajectory in the stationary coordinate system during balanced conditions.

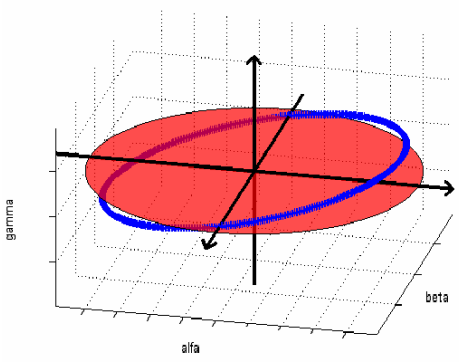


Figure 2.1-9b. Vector trajectory in the stationary coordinate system during unbalanced condition

Unbalance in d-q-o-coordinate vector representation

As mentioned in section 2.1.5, the d-q-0-transformation can be regarded as an observation of the rotating vector from a coordinate system that rotates with the same frequency as the fundamental frequency of the vector in the a - b plane. The d and q axis rotate on the a - b plane, while the o axis essentially is the preserved g axis. Thus, unbalance leads to the following behavior of the d-,q- and 0-components of a vector in the d-q-0-coordinate system (see fig 2.1-10b).

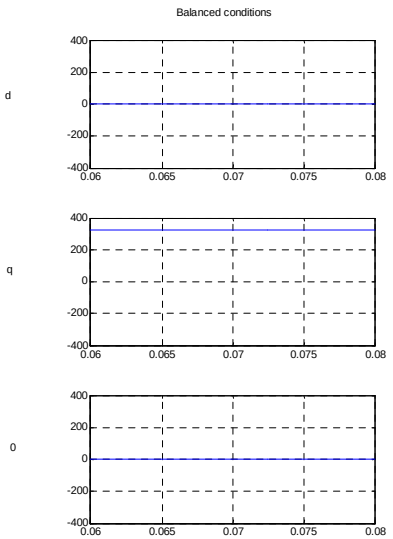


Figure 2.1-10a. Behavior of the d- q- and 0-components of a vector in the d-q-0-coordinate system during balanced conditions.

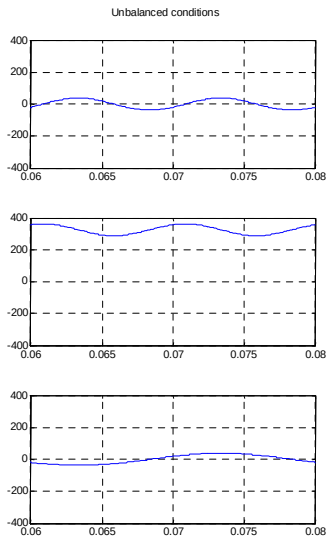


Figure 2.1-10b. Behavior of the d- q- and 0-components of a vector in the d-q-0-coordinate system during unbalanced conditions.

Since the added negative sequence causes an ellipsoidal vector trajectory on the a - b plane, both d and q will have a sinusoidal component, at twice the fundamental frequency, added to their stationary DC components.

The zero sequence component will in the 0-direction, as in the g -direction, appear as a sinusoidal component at the fundamental frequency.

Definition of unbalance

There are different ways to define unbalanced loads. One way is based on the differences between the maximum per phase load and the minimum per phase load [9]:

$$\%UnBal = \frac{Max(per\_phase\_load) - Min(per\_phase\_load)}{Total\_three\_phase\_load} \cdot 100$$

Equation 2.1.22

The drawback of this definition is that no concern is taken of the load power factors. If different phases are connected to loads with different power factors, conditions that very well may have impacts of the converters performance, will not be distinguished [2].

Another way is to base the definition on the sequence representation. According to [2], IEC gives the definition of unbalance in a three phase system as the ratio between the rms values of the negative sequence, or the zero sequence, and the positive sequence.

$$\%UnBal\_N = \frac{negative\_sequence\_component}{positive\_sequence\_component} \cdot 100 \quad \text{Equation 2.1.23}$$

and

$$\%UnBal\_0 = \frac{zero\_sequence\_component}{positive\_sequence\_component} \cdot 100 \quad \text{Equation 2.1.24}$$

In the next chapter, where different load conditions are discussed, both definitions will be used.

2.2 Loads to evaluate

The ultimate goal is to create a balanced three-phase voltage source that, independent of the load condition, always provides the correct voltage. Now, this is more of a target to take aim at, than an in practice achievable goal. The presented simulations of the converter will be limited by a number of different load conditions. To put a limit to the number of experiments, five different load scenarios considered to be reasonable are chosen.

Only resistive and inductive loads, with power factor between 0.2 and 1, are evaluated. Capacitive loads, that are assumed to be rarer, are put on hold for the time being.

Unbalanced loads are assumed to be a common load for the converter and will therefore be carefully examined. The unbalance may be caused by unevenly distributed single-phase loads, or by a combination of single-phase loads and three-phase loads.

The converters possibility to regulate voltage during transients is of interest. This will be simulated by sudden steps in the load.

The following scenarios of load conditions will be examined and simulated:

Scenario 1

Balanced load with power factor 1 and a step in the load. Starting at low power (approximately no load) and by a step, reach nominal power (50 kVA).

The scenario simulates that the converter starts with no load connected and then is subject to a purely resistive load, corresponding to rated power of the converter.

	I_a (current / powerfactor)	I_b (current / powerfactor)	I_c (current / powerfactor)	%unbalance	%neg.seq. unbalance	%zero.seq. unbalance	I_n (current)
Before step:	0 A/ 1	0 A/ 1	0 A/ 1	0 %	0 %	0 %	0 A
After step:	72.2 A/ 1	72.2 A/ 1	72.2 A/ 1	0 %	0 %	0 %	0 A

Table 2.2-1. Load scenario 1.

Scenario 2

Balanced load with power factor 0.2 and a step in the load. Starting at low power (approximately no load) and by a step, reach nominal power (50kVA).

The scenario simulates that the converter starts with no load connected and then is subject to a heavily inductive load, corresponding to rated power of the converter. The interesting part here is to see how well the inverter copes under inductive load conditions.

	I_a (current / powerfactor)	I_b (current / powerfactor)	I_c (current / powerfactor)	%unbalance	%neg.seq. unbalance	%zero.seq. unbalance	I_n (current)
Before step:	0 A/ 0.2	0 A/ 0.2	0 A/ 0.2	0 %	0 %	0 %	0 A
After step:	72.2 A/ 0.2	72.2 A/ 0.2	72.2 A/ 0.2	0 %	0 %	0 %	0 A

Table 2.2-2. Load scenario 2.

Scenario 3

Unbalanced load with power factor 0.8. The phase currents I_b and I_c are set equal to 0. The phase current I_a is set equal to nominal current I_n.

The scenario simulates that a partly inductive single-phase load is connected to phase a. Phase b and c are not connected. The interesting part here is to see how well the converter copes under unbalanced load conditions.

	I_a (current (A)/ powerfactor)	I_b (current (A)/ powerfactor)	I_c (current (A)/ powerfactor)	% unbalance	% neg.seq. unbalance	% zero.seq. unbalance	I_n (current (A))
No step	72.2 A/ 0.8	0 A	0 A	100 %	100 %	100 %	72.2 A

Table 2.2-3. Load scenario 3.

Scenario 4

A combination of one balanced three-phase load and one single-phase load with a step in the three-phase load. Both loads have a power factor of 0.8. Initially the phase currents I_b and I_c are set to $0.5 \cdot I_{nominal}$ and the phase current I_a is set to $I_{nominal}$. Then, there is a sudden change in the load so that I_b and I_c are set to 0 and I_a is set to $0.5 \cdot I_{nominal}$.

The scenario simulates that one partly inductive three-phase load as well as one partly inductive single-phase load at phase a are connected to the converter. Then the three-phase load is disconnected. The interesting part here is to see how the removal of a quite heavy three-phase load affects the voltage over a simultaneously connected single-phase load.

	I_a (current (A)/ powerfactor)	I_b (current (A)/ powerfactor)	I_c (current (A)/ powerfactor)	% unbalance	% neg.seq. unbalance	% zero.seq. unbalance	I_n (current (A))
Before step:	72.2 A/ 0.8	36.1 A/ 0.8	36.1 A/ 0.8	25 %	25 %	25 %	36.1 A
After step:	36.1 A/ 0.8	0 A	0 A	100 %	100 %	100 %	36.1 A

Table 2.2-4. Load scenario 4.

Scenario 5

A combination of one heavily inductive single-phase load and one resistive single-phase load. The inductive phase c has a power factor of 0.2. I_a and I_c are both set equal to nominal current $I_{nominal}$.

The scenario simulates that one heavily inductive single-phase load, as well as one purely resistive single-phase load are connected to the converter. The interesting

part here is to see how the converter behaves under this heavily unbalanced load where the neutral current exceeds the line currents.

	I_a (current (A)/ powerfactor)	I_b (current (A)/ powerfactor)	I_c (current (A)/ powerfactor)	% unbalance	% neg.seq. unbalance	% zero.seq. unbalance	I_n (current (A))
No step:	72.2 A/ 1	0 A	72.2 A/ 0.2	50 %	20 %	120 %	134 A

Table 2.2-5. Load scenario 5.

2.3 Three leg converters

This section deals with the basic theory of three leg power electronic converters. For this project, as will be shown later, the choice has fallen on the use of a four leg converter. Though, for a start, the three leg converter is examined to demonstrate theory, function and properties of three phase converters.

2.3.1 The three leg bridge

The principles for the physical layout of three phase converters, also known as voltage-source converters (VSC:s) are shown in fig. 2.3-1. The bridge is connected to the DC-link, whose voltage is raw material in the creation of the three-phase output voltage. The link voltage is from now on called *dc-link*. The mid potential of the dc-link is defined as neutral.

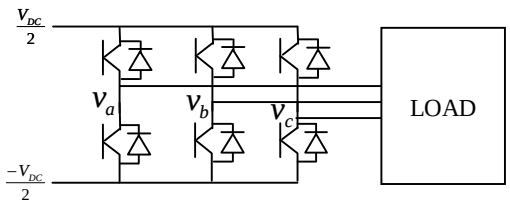


Figure 2.3-1.Three-phase converter network.

Between the two poles of the dc link, the three half-bridges are connected. Each half-bridge has two power electronic switches. By switching them, between fully conducting and fully blocking, the potentials of each half-bridge (v_a, v_b, v_c), with respect to the mid potential of the dc link, can attain $\pm V_{DC}/2$.

The switch states are denoted (a, b, c). With, for example the state (a, b, c) = (+,-,-) (like in fig. 2.3-2 a) $v_a = V_{DC}/2$ and $v_b = v_c = -V_{DC}/2$.

If the potentials (v_a, v_b, v_c) =($V_{DC}/2$, $-V_{DC}/2$, $-V_{DC}/2$), like in the example above, are transformed to a vector in a - b -coordinates (according to eq. 2.1.13), it will attain the value: $v_a = \frac{2 \cdot V_{DC}}{3}$, $v_b = 0$ (as in fig. 2.3-2 b)

The switch state (a, b, c) can attain the states (+,-,-), (+,+,-), (-,+,-), (-,+,+), (-,-,+) and (+,-,+), who are creating the six possible active values of the voltage vector, and (+,+,+) and (-,-,-), who are creating the zero-vectors, in the a - b -coordinates according to fig. 2.3-2b.

According to eq. 2.1.13, the output voltage vector **v** in the a - b -plane can therefore only attain the following values:

$$v_a = \left\{0, \pm\frac{V_{DC}}{3}, \pm\frac{2 \cdot V_{DC}}{3}\right\}$$
$$v_b = \left\{0, \pm\frac{V_{DC}}{\sqrt{3}}\right\} \qquad \text{Equation 2.3.1}$$

The maximum modulus of the voltage vector is:

$$|v| = \frac{2 \cdot V_{DC}}{3} \qquad \text{Equation 2.3.2}$$

The resulting vector diagram is shown in fig. 2.3-2b.

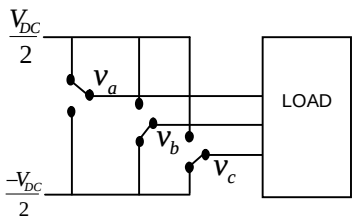


Figure 2.3-2a. The three phase converter switching network.

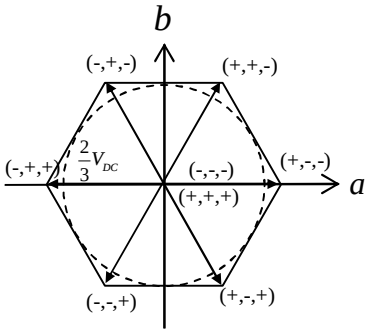


Figure 2.3-2b. The attainable voltage vectors.

By combining the eight possible switching states, including the zero vectors, using *pulse width modulation* (described below), any voltage vector within the hexagon in fig. 2.3-2b can be generated in average. However, there is an even tighter limitation for the voltage vector to achieve a *linear* modulation, namely the circle that touches the inner sides of the hexagon. The circle has a radius of $\sqrt{3}/2$ times the maximum modulus of the voltage vector.

Circle radius = $V_{base} = |v|_{max} \cdot \sqrt{3}/2 = V_{DC}/\sqrt{3}$ Equation 2.3.3

The radius of the circle is denoted V_{base} which is further referred to in the section below. $\mathbf{v}_{ref}$ is the desired value of the mean voltage vector.

2.3.2 Pulse-width modulation

Pulse-width modulation is a way of choosing the sequence of the switch-states above so that the *mean value* $\boldsymbol{v}_{mean}$, becomes the desired $\boldsymbol{v}_{ref}$. Referring to fig. 2.3-3 the average value can be expressed as:

$$v_{mean} = \frac{1}{T}\left[t_+ \cdot V_{base} + t_- \cdot \left(-V_{base}\right)\right] \qquad \text{Equation 2.3.4}$$

Where T is the switch-period and t_+ and t_- are the periods when the switches, in the current half bridge, are connecting the phase to V_{base} or $-V_{base}$ respectively. For example: If $t_+ = T$, then $\boldsymbol{v}_{mean} = V_{base}$; if $t_+ = t_- = T/2$, then $\boldsymbol{v}_{mean} = 0$ and if $t_+ = 0$, $\boldsymbol{v}_{mean} = -V_{base}$. The resulting voltage waveform is pulse-width modulated and this operation of the inverter is called *pulse-width modulation* (PWM). See fig. 2.3-3.

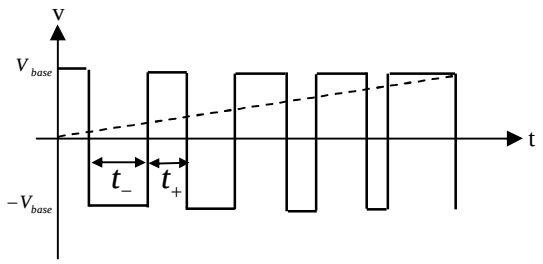


Figure 2.3-3. Pulse-width modulated waveform and mean value.

The classical method to generate appropriate switching signals from the reference signal $\boldsymbol{v}_{ref}$, is the triangle wave comparison method. The idea is to compare $\boldsymbol{v}_{ref}$ to a

triangular carrier signal of amplitude V_{base}. When v_{ref} is larger than the carrier, the potential of the current half-bridge is set to V_{base}, and otherwise to $-V_{base}$. This is illustrated in fig. 2.3-4. The only difference compared to fig. 2.3-3 is that the switchings are made within the period $0 < t < T$ and not at the beginning and end of the period.

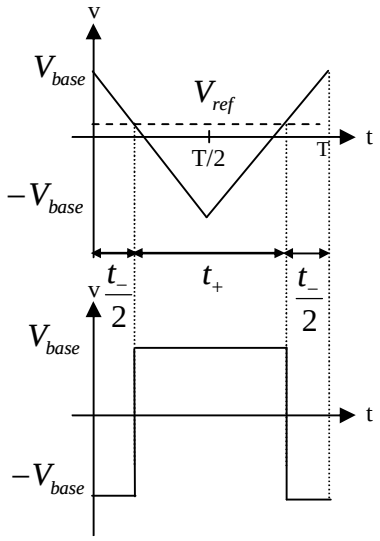


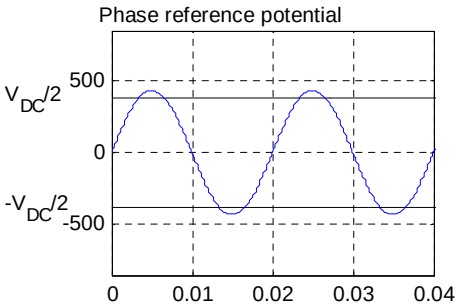
Figure 2.3-4.Triangle comparison method.

As mentioned above, V_{base} was originally set to $V_{base} = V_{DC}/\sqrt{3}$ to achieve a linear modulation. It is proven to be an unreachable voltage with a sinusoidal reference voltage, since only the potentials $\pm V_{DC}/2$ are available for the potentials delivered from each half-bridge, with respect to the dc-link defined neutral. But, if V_{base} instead is selected to $V_{DC}/2$, it is not possible to utilize all of the available dc link voltage, as shown below.

Since the *line to line* voltage is equal to the line to neutral voltage times $\sqrt{3}$, ($U_{ab} = U_{an} \cdot \sqrt{3}$), the maximum line to line voltage from the converter will be (see fig. 6a, b, c):

$$U_{\max\_\ phase-phase} = \frac{V_{DC}}{2} \cdot \sqrt{3} = V_{DC} \cdot \sqrt{3}/2 \approx 0.87 \cdot V_{DC} \qquad \text{Equation 2.3.5}$$

Since the converter, as later will be seen, will need to deliver as much voltage as possible, this is a drawback.



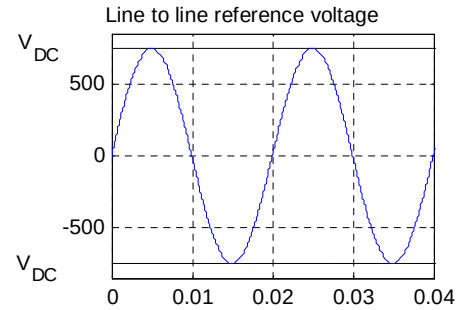
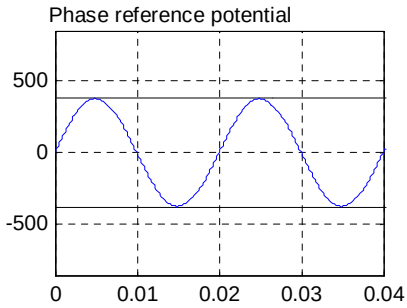


Figure 2.3-5a. Phase reference potential and line to line reference voltage, compared to available dc link voltage when $V_{base}=V_{DC\,sq.}$*/sq.root(3)*



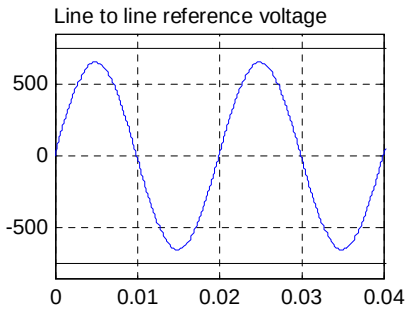


Figure 2.3-5b. Phase reference potential and line to line reference voltage, compared to available dc link voltage when $V_{base}=V_{DC}/2$.

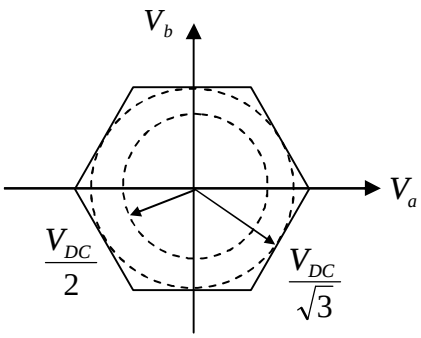


Figure 2.3-5c. $V_{base}=V_{DC}/2$ *and* $V_{base}=V_{DC}$ */ sq.root(3)*

A way to achieve full utilization of the dc link voltage, and still have a linear modulation, is to allow some movements of the neutral point. This method is called the *Symmetrized triangle wave comparison method.*

2.3.3 Symmetrized modulation

If the same deviation is added or subtracted from all reference signals (v_a, v_b, v_c), a zero-sequence Δ is added. The voltage vector **v** in the a - b -plane is by that not altered.

By studying the three sinusoidal phase potential waves as a group, one can see that they are moving in an "unsymmetrical way" compared to the center of the triangular wave. For example, when v_a reaches its maximum value, v_b and v_c are at half of their minimum values (See fig. 2.3-6a).

The key to extend the modulation range is to select Δ so that:

$$\max(v_a', v_b', v_c') = -\min(v_a', v_b', v_c'). \qquad \text{Equation 2.3.6}$$

This implies selecting:

$$\Delta = \frac{\max(v_a, v_b, v_c) + \min(v_a, v_b, v_c)}{2} \qquad \text{Equation 2.3.7}$$

and

$$(v_a', v_b', v_c') = (v_a, v_b, v_c) - \Delta \qquad \text{Equation 2.3.8}$$

where (v_a', v_b', v_c') are the *symmetrized* phase voltage references (see fig. 2.3-6b)

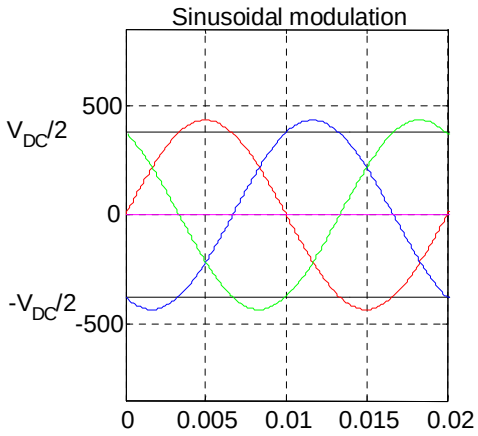


Figure 2.3-6a.Sinusoidal modulation. Phase and neutral reference potentials.

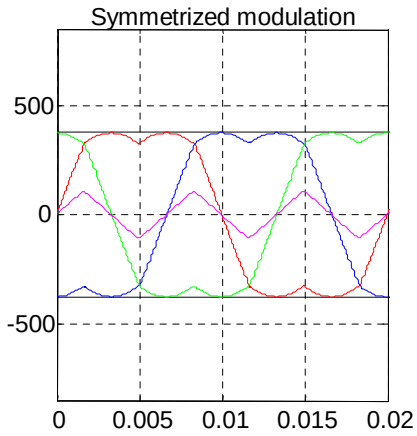


Figure 2.3-6b. Symmetrized modulation. Phase reference potentials and zero sequence deviation (delta).

By doing this, one can see that the amplitude of the symmetrized phase potential references (fig. 2.3-6b), *compared to the center of the triangular wave*, is less than in the sinusoidal case (2.3-6a). This makes it possible to increase the amplitude of the line to neutral reference voltage by a factor $2/\sqrt{3}$ and to select $V_{base} = V_{DC}/\sqrt{3}$, still using the maximum phase potentials $\pm V_{DC}/2$.

Since the line to line voltage is $U_{ab} = \sqrt{3} \cdot U_{an}$, the maximum line to line voltage will by this method reach $\sqrt{3} \cdot V_{DC}/\sqrt{3} = V_{DC}$, and all of the dc link voltage may be utilized:

$$U_{\max\_\, phase-phase} = V_{DC} \qquad \text{Equation 2.3.9}$$

The line to line voltages will not be affected by the movements in the neutral point. Only the phase potentials and the potential of the neutral, *with respect to the dc link defined neutral point*, is altered.

2.3.4 Overmodulation

Using the symmetrized modulation method it is possible, under linear modulation, to reach V_{DC} as the maximum line to line voltage amplitude and $V_{DC}/\sqrt{3}$ as the maximum line to neutral voltage amplitude. The limit for reachable output voltages

is thereby set by the dc link. If the reference voltage vector $\mathbf{v}_{ref}$ reaches outside the limit set by the circle radius $=V_{DC}/\sqrt{3}$ inside the hexagon in fig. 2.3-7a, the PWM goes into *overmodulation*. Then the output voltage vector will follow the reference vector when the reference vector is inside the hexagon and the hexagon when the reference vector is outside the hexagon (fig. 8b).

In the following simulations, this will be avoided by limiting the reference signal to the linear modulation area:

$$\left|v_{ref}\right| \le V_{base} = \frac{V_{DC}}{\sqrt{3}} \qquad \text{Equation 2.3.10}$$

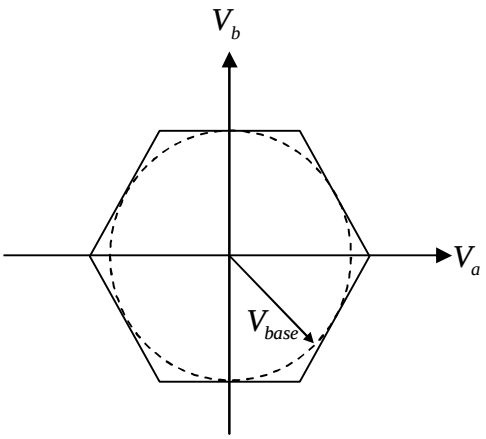


Figure 2.3-7a. Limit for overmodulation.

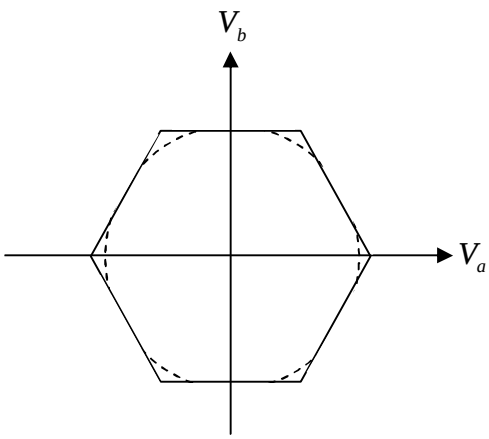


Figure 2.3-7b Output voltage during overmodulation.

2.3.5 Unbalanced conditions

According to the assumption that the load connected to the converter is balanced, the reference voltage vector will follow a circular trajectory in the a - b -plane. The definition in eq. 2.3.10 for the dc link voltage may then be sufficient for control (see fig. 2.3-8a).

During balanced load conditions, the reference voltage vector will only consist of the positive sequence component (mentioned earlier in section 2.1.6). During unbalanced load however, a negative sequence component will be added to the reference voltage vector as well. This combination of positive and negative sequence voltages will give the trajectory of the reference voltage vector the shape of an ellipse (see fig. 2.3-8b). To be able to control the negative sequence reference

voltage as well as the positive, the major radius of the ellipse must be confined within the inscribed circle of the hexagon, with the radius V_{base}.

$$\left|v_{ref\_pos.seq}\right| + \left|v_{ref\_neg.seq}\right| \le V_{base} = \frac{V_{DC}}{\sqrt{3}} \qquad \text{Equation 2.3.11}$$

The minimum dc link voltage in the unbalanced case depends on the degree of unbalance of the load. However, a higher dc link voltage will lead to a higher ability of the converter to control the output voltage. This may be even more important if the load is unbalanced.

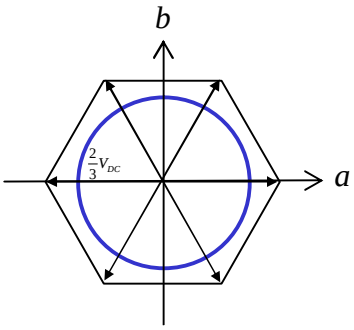


Figure 2.3-8a.Voltage reference vector trajectory under balanced conditions.

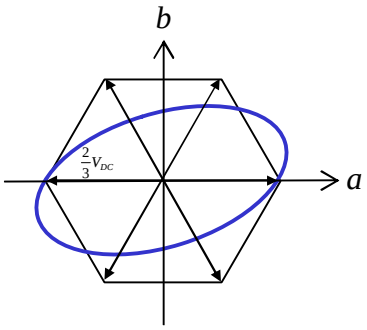


Figure 2.3-8b.Voltage reference vector trajectory under unbalanced conditions.

2.3.6 The creation of a neutral connection

For a three-phase three-wire system, due to the topology, the sum of the three phase currents are zero and the voltage in the neutral point is floating. During balanced load condition this is not a problem. Since the potential in the neutral point during balance always will be zero, the load voltages can be correctly controlled. During unbalanced load conditions however, the line to neutral output voltages will unavoidable become unbalanced as well since the voltage in the neutral point cannot be controlled separately. *The control target of balanced three-phase voltages contradicts with the fact that the zero-sequence current cannot exist* [2]. Only the positive and negative sequence current exists in the system.

In order to make the control target possible, a neutral conductor must be provided so that the zero sequence current can flow through. For a three-phase four-wire system there is a neutral connection that provides current to flow from the neutral point of the load. Here the sum of the three phase currents *and* the neutral current

are zero and the voltage in the neutral point may be defined. In this system both positive, negative *and zero* sequence exists.

Passive methods

There are passive methods to provide the neutral connection for unbalanced loads [2]:

Transformer

The Δ/Y transformer is a zero sequence trap. Connecting the Δ windings to the inverter and the Y windings to the load, the zero sequence current caused by the load is trapped into the Δ windings. Circulating within the transformer winding, it is prevented from traveling back to the inverter and the dc link. Another passive way to provide the neutral connection is to use a zig-zag transformer, which also balances the load to some extent. The zero sequence currents from each phase are shifted at different phase angles, and thus can be canceled with each other.

The problem with the approaches mentioned above, is that they add the transformer to the converter. Transformers for high power are very bulky components.

Split dc link capacitor

Another passive approach to provide a neutral connection is to use two capacitors to split the dc link and connect the neutral point to the mid-point of the two capacitors (see fig. 2.3-9).

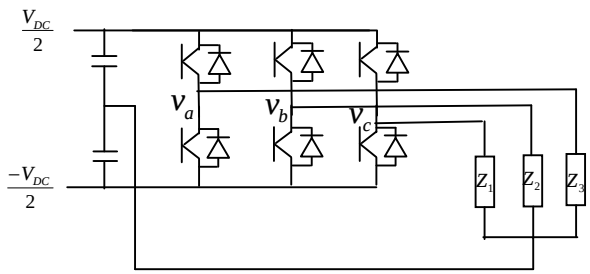


Figure 2.3-9. Split dc link capacitor to provide the neutral point.

There are two problems with this approach. Firstly, the neutral point will be fixed to the middle of the dc link, which will cause poor utilization of the dc link voltage. (The motivation for this is in section 2.3.2, eq. 2.3.5.) Secondly, a huge increase of the capacitance is needed to maintain the dc link voltage ripple at a reasonable level [2].

The ripple will consist of two frequencies, $2w$ and w. The $2w$ ripple is caused by the negative sequence load current and the w ripple is caused by the zero sequence load current. The ripple caused by the negative sequence current will occur under unbalanced conditions in any case. The ripple caused by the zero sequence current on the other hand, is directly caused by the connection of the neutral conductor to the split dc link capacitor. See Appendix A for calculations of capacitor size.

A fourth leg

By replacing the three leg switching network in fig. 2.3-1 with a four leg switching network, as shown in fig. X10, a four half-bridge power electronic converter is obtained. By tying the neutral connection of the load to the mid point of the fourth half-bridge, the four-legged PWM converter can handle the neutral current caused by an unbalanced load. A balanced output voltage can be achieved with a tightly regulated neutral point.

The method should, compared to the above mentioned approaches, have the advantages of:

1. Possibility for high utilization of the dc link voltage.
2. No bulky transformers / much smaller dc link capacitors.

Disadvantages are that one more switch pair and one more output filter inductor are added to the design.

This approach seems to be the most preferable and is the one chosen for the project. From now on, when a converter is mentioned, it refers to a four leg converter if nothing else is mentioned.

2.4 The four legged converter

The choice is made to use a converter with a fourth half-bridge to obtain the neutral connection. This converter has much in common with the regular three-phase converter. With the fourth half-bridge, the possibility to connect the neutral is achieved as well. By this a third degree of freedom is added. Instead of using the a - b coordinates, one have to add yet another dimension and work in the a - b - g -coordinate system.

2.4.1 The four leg bridge

The layout of a four legged three phase converter is shown in fig. 2.4-1.

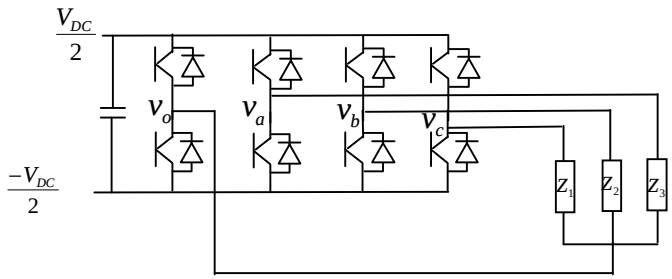


Figure 2.4-1. Four-legged converter network.

Each half-bridge has two power electronic switches. By switching them between fully conducting and fully blocking, the potentials of each half-bridge (v_a, v_b, v_c, v_n) can all attain $\pm V_{DC}/2$, with respect to the neutral point defined as the mid potential of the dc link. This means that the voltages (v_{an}, v_{bn}, v_{cn}), can attain $\pm V_{DC}$.

The switch states are now denoted (a, b, c, n), (see fig. 2.4-2). Compared to the 8 switch states in the three half-bridge case, the converter with four half-bridges can attain 16 switch states. Since a third degree of freedom is added with the neutral half-bridge and its possibility of a neutral current, the a-b-coordinate system needs an extension to the a-b-g-coordinate system.

If the output voltage components (v_{an}, v_{bn}, v_{cn}), according to the 16 possible switch states of (a, b, c, n), are transformed (using eq. 2.1.17) into a output voltage vector **v** in the a-b-g-coordinates, it can attain the following values:

$$v_a = \left\{0, \pm\frac{V_{DC}}{3}, \pm\frac{2\cdot V_{DC}}{3}\right\}$$
$$v_b = \left\{0, \pm\frac{V_{DC}}{\sqrt{3}}\right\} \qquad \text{Equation 2.4.1}$$
$$v_g = \left\{0, \pm\frac{V_{DC}}{3}, \pm\frac{2\cdot V_{DC}}{3}\right\}$$

The resulting vector diagram containing all attainable vectors is shown in fig. 2.4-3.

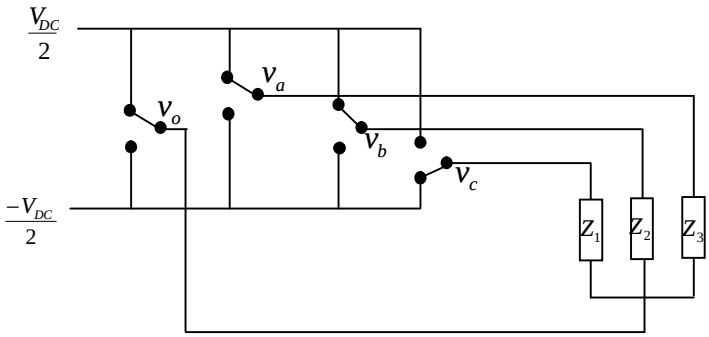


Figure 2.4-2.The four legged converter switching network.

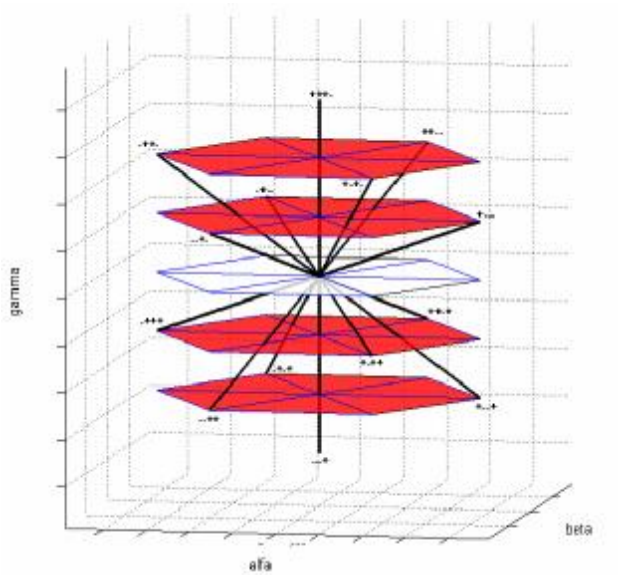


Figure 2.4-3. The output voltage vectors in alfa-beta-gamma coordinates.

By combining the 16 possible switching states, using *pulse width modulation*, any voltage vector within the *polygon* in fig. 2.4-4 can be generated in average. Compare this with the hexagon in the three half-bridge converter case.

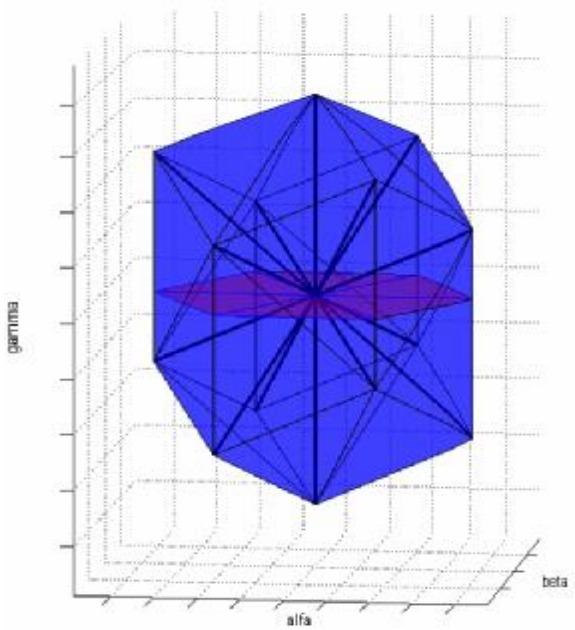


Figure 2.4-4. The polygon limiting the output voltage vector (reference voltage vector) in the four leg converter case.

2.4.2 Over modulation

The phenomenon is similar to the case with a three leg converter. If the reference voltage vector $\mathbf{v}_{ref}$ reaches outside the limit set by the polygon in fig. 2.4-4, the PWM goes into *overmodulation*. The output voltage vector will then follow the reference vector when the reference vector is inside the polygon and the surface of the polygon when the reference vector is outside the sphere.

2.4.3 Unbalanced conditions

During balanced load conditions, the reference voltage will only consist of the positive sequence component (mentioned earlier in 2.1.6). It will therefore follow a circular trajectory in the a - b -plane (see fig. 2.4-5a).

During unbalanced load however, the reference voltage will not only consist of the positive sequence component, but both negative and zero sequence components may be added as well. The combination of positive, negative and zero sequence voltages will give the trajectory of the reference voltage vector the shape of a skewed ellipse (see fig. 2.4-5b).

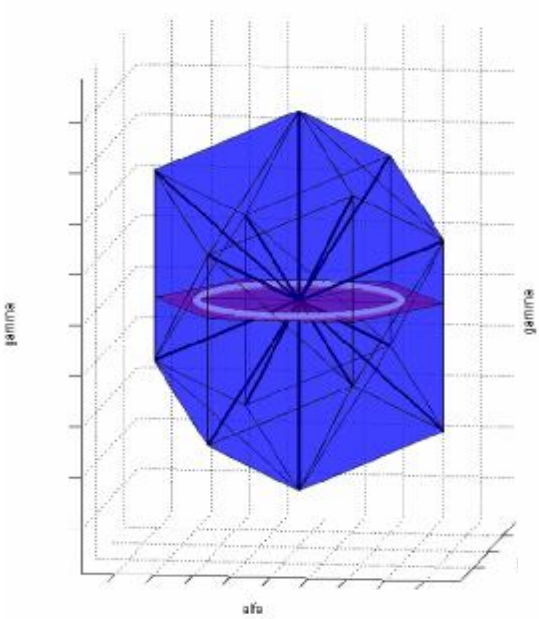


Figure 2.4-5a. The reference voltage vector trajectory during balance and the polygon limiting the reference voltage vector in the four leg converter case.

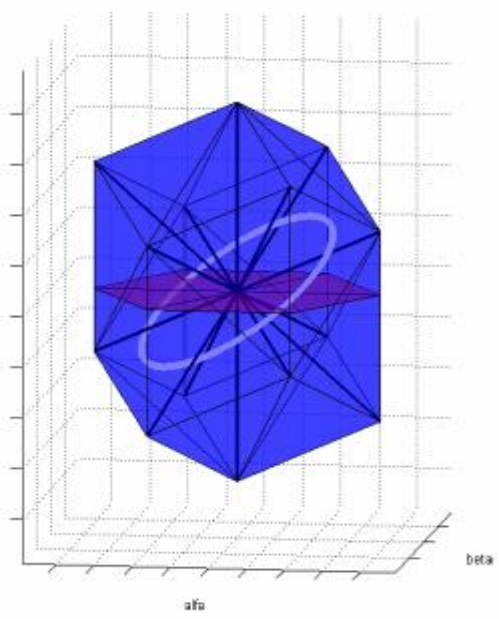


Figure 2.4-5b.The reference voltage vector trajectory during unbalance and the polygon limiting the reference voltage vector in the four leg converter case.

To be able to create both the positive, negative and zero sequences of the reference voltage vector, the major radius of the ellipse must be confined within the polygon, according to fig. 2.4-5b. Obvious, a higher dc link voltage will lead to a higher ability of the converter to control the output voltage. This may be especially important during unbalanced load conditions.

2.5 Circuit model of the system

The following section deals with the system in overall. The system consists of the filter inductors, the filter capacitors, the load, and the control voltage sources, which are the voltages from the converter. The model assumes that the switching frequency is very high compared to the fundamental frequency, so that voltage and current ripple are negligible. In this way the switching model can be approximated as an average circuit model. The system is first modeled as the “real” system in a-b-c–coordinates. Then the model is transformed, for control-purposes, to the corresponding system in d-q-0-coordinates.

2.5.1 The system in abc-coordinates

The average circuit model of the system is modeled according to fig. 2.5-1.

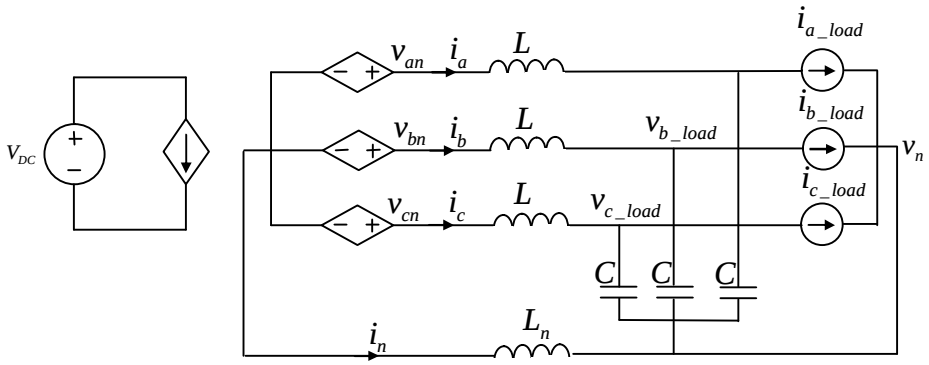


Figure 2.5-1. The average circuit model in a-b-c-coordinates.

Assuming the dc link voltage to be an ideal voltage source V_{DC}, the control voltage sources (v_{an}, v_{bn}, v_{cn}) can be expressed as:

$$\begin{bmatrix} v_{an} \\ v_{bn} \\ v_{cn} \end{bmatrix} = \begin{bmatrix} v_a - v_n \\ v_b - v_n \\ v_c - v_n \end{bmatrix} = V_{DC} \begin{bmatrix} d_{an} \\ d_{bn} \\ d_{cn} \end{bmatrix} \qquad \text{Equation 2.5.1}$$

(d_{an}, d_{bn}, d_{cn}) are the phase to neutral duty ratios of the converter.

The differential equations describing the system are expressed as:

$$\frac{d}{dt}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \frac{L_n}{L} \cdot \frac{d}{dt}\begin{bmatrix} i_n \\ i_n \\ i_n \end{bmatrix} + \frac{V_{DC}}{L} \cdot \begin{bmatrix} d_{an} \\ d_{bn} \\ d_{cn} \end{bmatrix} - \frac{1}{L}\begin{bmatrix} v_{a\_load} \\ v_{b\_load} \\ v_{c\_load} \end{bmatrix} \qquad \text{Equation 2.5.2}$$

$$i_a + i_b + i_c + i_n = 0 \qquad \text{Equation 2.5.3}$$

$$\frac{d}{dt}\begin{bmatrix} v_{a\_load} \\ v_{b\_load} \\ v_{c\_load} \end{bmatrix} = \frac{1}{C}\left(\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} - \begin{bmatrix} i_{a\_load} \\ i_{b\_load} \\ i_{c\_load} \end{bmatrix}\right) \qquad \text{Equation 2.5.4}$$

Where (i_a, i_b, i_c) are the inductor currents (the converter currents), $(v_{a\_load}, v_{b\_load}, v_{c\_load})$ are the output capacitor voltages (the load voltages) and $(i_{a\_load}, i_{b\_load}, i_{c\_load})$ are the load currents.

It can be seen that the system is a second order system with $V_{DC} \cdot (d_{an}, d_{bn}, d_{cn})^T$ as the input signals, the inductor currents (i_a, i_b, i_c) , as states and the capacitor voltages $(v_{a\_load}, v_{b\_load}, v_{c\_load})$ as states as well as output signals.

The phase load currents will in turn depend on the output capacitor voltages and the load impedances as:

$$\begin{bmatrix} i_{a\_load} \\ i_{b\_load} \\ i_{c\_load} \end{bmatrix} = \begin{bmatrix} v_{a\_load} \\ v_{b\_load} \\ v_{c\_load} \end{bmatrix} \cdot \begin{bmatrix} Z_a & Z_b & Z_c \end{bmatrix} \qquad \text{Equation 2.5.5}$$

There are problems controlling such a system. The steady state solutions for all the variables are sinusoidal. Due to the time varying nature of the model in a-b-c-coordinates, there is no DC operation point for the system. The controllers for a system like this would have sinusoidal reference signals even at steady state, which would lead to constantly stationary errors in the output signals. The control methods for a system like this would also suffer from poor performance due to conflicts among the three phase controllers [2].

To avoid the problems above and achieve a DC operating point at steady state, the system is transformed into the rotating d-q-0-coordinate system

2.5.2 The system in d-q-0-coordinates

In section 2.1.5 its shown how variables, represented in the a-b-c-coordinates, are transformed into representation in d-q-0-coordinates. This is what will be done next to the whole system described in section 2.5.1. [2]

The systems average circuit model in d-q-0-coordinates can be obtained by applying the coordinate transformation matrix T_4 (from section 2.1.5) to both sides of eq. 2.5.2 and eq. 2.5.4. To make the transformations easier, the following expressions may be used:

$$T_4 \begin{bmatrix} i_n \\ i_n \\ i_n \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ -3 \cdot i_o \end{bmatrix}$$

Equation 2.5.6

$$T_4 \frac{dX_{abc}}{dt} = T_4 \frac{dT_4^{-1}}{dt} X_{dq0} + \frac{dX_{dq0}}{dt}$$

Equation 2.5.7

and

$$T_4 \frac{dT_4^{-1}}{dt} = \begin{bmatrix} 0 & -w & 0 \\ w & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}$$

Equation 2.5.8

By using them on equation 2.5.2, and 2.5.4, the resulting circuit model in d-q-0-coordinates is expressed according to:

$$\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} = V_{DC}\begin{bmatrix} 1/L & 0 & 0 \\ 0 & 1/L & 0 \\ 0 & 0 & 1/(L+3\cdot L_n) \end{bmatrix}\begin{bmatrix} d_d \\ d_q \\ d_0 \end{bmatrix} - \begin{bmatrix} 1/L & 0 & 0 \\ 0 & 1/L & 0 \\ 0 & 0 & 1/(L+3\cdot L_n) \end{bmatrix}\begin{bmatrix} v_d \\ v_q \\ v_0 \end{bmatrix} + w\begin{bmatrix} i_q \\ -i_d \\ 0 \end{bmatrix}$$

Equation 2.5.9

and

$$\frac{d}{dt}\begin{bmatrix} v_d \\ v_q \\ v_0 \end{bmatrix} = \frac{1}{C}\left(\begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} - \begin{bmatrix} i_{d\_load} \\ i_{q\_load} \\ i_{0\_load} \end{bmatrix}\right) + w\begin{bmatrix} v_q \\ -v_d \\ 0 \end{bmatrix}$$

Equation 2.5.10

Where (i_d, i_q, i_0) is the inductor current (the converter current), (d_d, d_q, d_0) is the duty ratios of the converter, (v_d, v_q, v_0) is the output capacitor voltage

(the load voltage) and $(i_{d\_load}, i_{q\_load}, i_{0\_load})$ is the load current, now expressed as vectors in the d-q-0-coordinates.

In d-q-0-coordinates, the second order system has $V_{DC} \cdot (d_d, d_q, d_0)^T$ as the input signals, the inductor currents (d_d, d_q, d_0) , as states and the capacitor voltages (v_d, v_q, v_0) as states as well as output signals.

The equivalent circuit model, expressed by eq. 2.5.9 and eq. 2.5.10 is shown in fig. 2.5-2. Note the cross coupling terms between d and q caused by the last terms in eq. 2.5.9 and eq. 2.5.10.

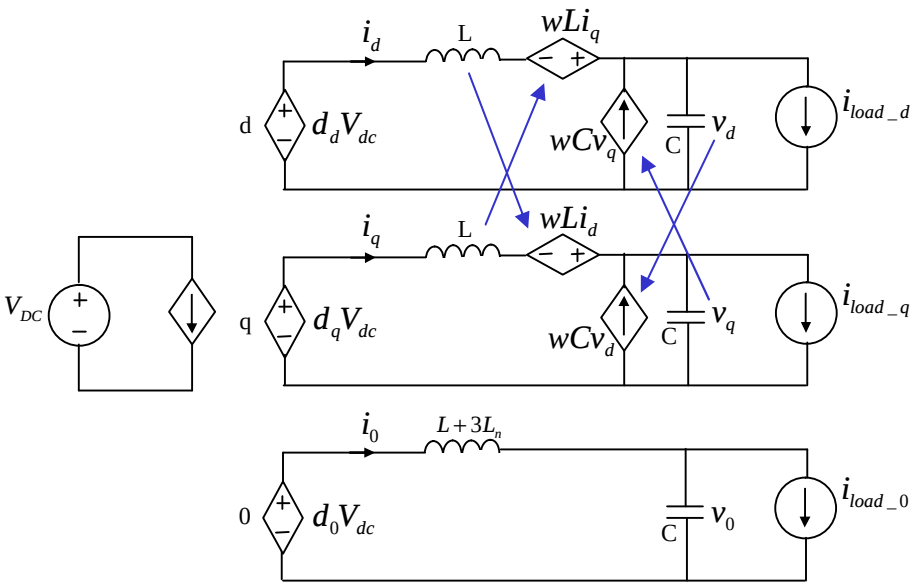


Figure 2.5-2.The average circuit model in d-q-0-coordinates.

If concern is taken to the equivalent series resistances (ESR:s) in the inductors and capacitors, they should be modeled like in fig. 2.5-3 [7].

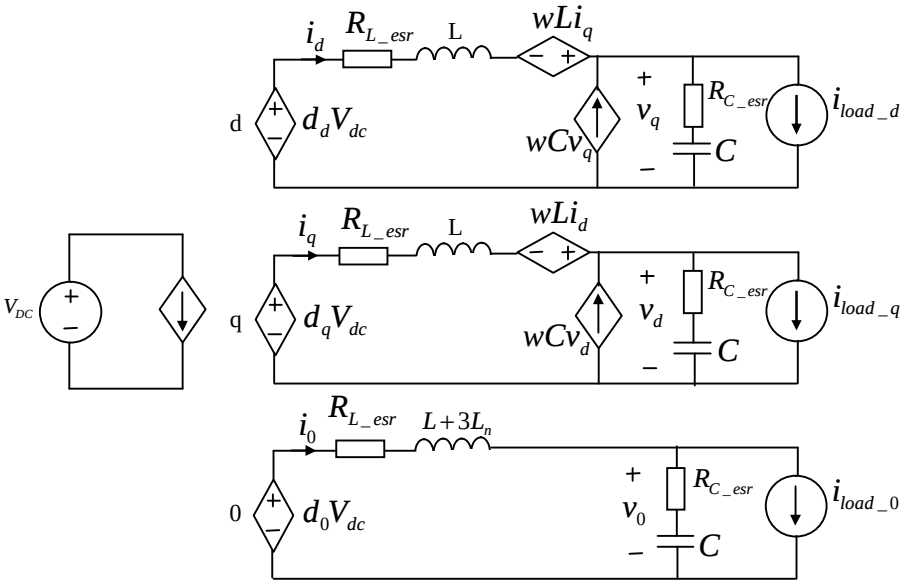


Figure 2.5-3.The average circuit model in d-q-0-coordinates, with ESR:s.

This is the model later used in the control of the converter.

2.6 Dimensioning

This section deals with the choices concerning: Dc link voltage, switching frequencies and parameters of the components in the system. For example how different choices of components affect the properties of the converter, what trade offs have to be made between different characteristics, and some definite specifications and limitations.

2.6.1 Dc-link voltage

The selection of dc link voltage is a trade-off between power switch voltage stress and control margin for transients and unbalanced load conditions. It is of course also limited, unless the use of some step-up converter, by the available dc voltage.

Assuming balanced load conditions and that the wanted line to neutral output voltage is 230VAC, the voltage reference vector is needed to be at least $230 \cdot \sqrt{2} \approx 325V$. The dc link voltage would then, according to eq. 2.3.10, need to be at least $230 \cdot \sqrt{2} \cdot \sqrt{3} \approx 564V$. There will however be voltage drops during heavy load in the ESR:s (parasitic resistances) in the

output filters. There is also a need for some control margin. A reasonable dc link voltage would therefore be something like 700-750 V.

Under unbalanced conditions however, according to eq. 2.3.11 and fig. 2.6-1, the demand on the dc link voltage is higher than in the balanced case. If the voltage reference vector reference extends outside the circle with V_{base} as radius, the converter has no possibility to correct all of the control error.

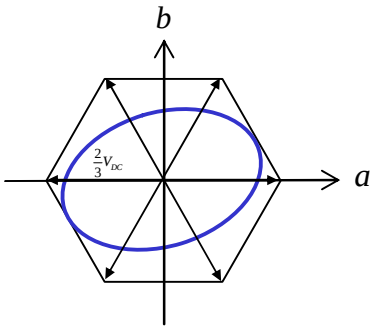


Figure 2.6-1.Example of voltage reference vector trajectory under unbalanced conditions.

2.6.2 Power electronic switches

The power electronic switches of the converter need to, under a specified maximum operating temperature, withstand the voltages and current applied to them. They must also, for control issues, be able to switch at a certain rate at reasonable losses. The choice has fallen on using IGBT:s (Isolated Gate Bipolar Transistors). The IGBT:s compromises the abilities of withstanding high voltage and high current density, with the possibility of short switch intervals and low on-state voltage drop [5].

The voltage the IGBT:s needs to withstand is the maximal dc link voltage. For commercial IGBT:s there are different standardized voltage levels. In this case the voltage levels 600V, 1200V and 1700V may be of interest.

On the phase half bridges, the current the IGBT:s has to withstand is the maximal line current during full load. Assuming a nominal 3-phase load for the converter of S_n, the nominal line current I_{line} will be:

$$I_{line} = \frac{S_n}{3 \cdot U_{line-neutral}} = \frac{S_n}{\sqrt{3} \cdot U_{line-line}} \qquad \text{Equation 2.6.1}$$

On the neutral half bridge, the current the IGBT has to withstand depends on both the maximal load *and* the assumed worst case of unbalanced load. Assuming balanced condition, no current passes trough the neutral half bridge. Assuming 33% zero sequence unbalance (see section 2.1.6), the current trough the neutral half bridge will be equal to the rated per phase current.

2.6.3 Switching frequency and converter losses

The switching frequency is a trade-off between thermal losses and control bandwidth.

From a control point of view, the switching frequency should be selected as high as possible. The higher the frequency is, the more often the control signals can be updated. The switching frequency thereby has a direct connection to the possible control bandwidth of the converter.

The temperature normally sets the limitation for the switching frequency when the heat, caused by the losses, no longer can be sufficiently removed by cooling devises. Another limitation may be when the efficiency of the converter is assumed to be too low. In converters for high power, like in this case, most probably cooling issues will be the limiting factor for the switching frequency.

Loss calculations

The calculations of the losses are made for one half bridge of the converter (see fig. 2.6-2)

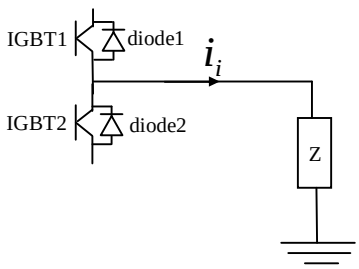


Figure 2.6-2 One half bridge of the converter.

Fig. 2.6-3 shows the fundamental components of the output voltage and output current for the half bridge.

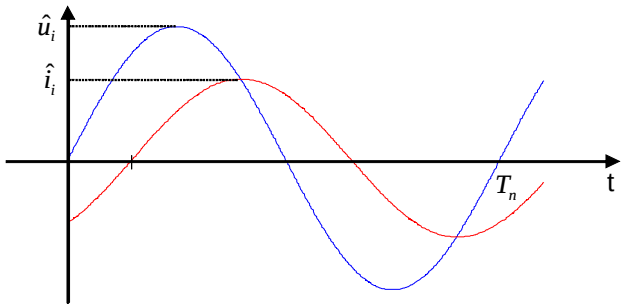


Figure 2.6-3. Converter output voltage (blue) and current (red). The current is displaced by an angle phi, relative the voltage.

The losses are of two types: First, the losses during the turn-on and turn-off states of the semiconductors, when there for a short moment both is a high voltage across the semiconductor and a high current through it. And second, the losses during the conducting state of the semiconductors, due to the current going through it and the forward voltage drop of the semiconductor.

Turn-on, turn-off losses

A method presented in [10] may be used to calculate the turn-on and turn-off losses. For the IGBT:s of one half-bridge, i.e. one leg of the converter, the turn-on and turn-off losses are estimated as:

$$\overline{P}_{sw,IGBT} = \frac{1}{T_n}\int_{T_n}(P_{on}+P_{off})dt = \frac{f_{sw}}{T_n}\int_{T_n}(E_{on}+E_{off})dt =$$

$$= \frac{(E_{on,n}+E_{off,n})}{V_{dc,n}I_n}\cdot\frac{V_{dc}f_{sw}}{T_n}\cdot\int_{T_n}\left|\hat{i}_i\sin(wt-j)\right|dt = \qquad \text{Equation 2.6.2}$$

$$= \frac{2\sqrt{2}}{p}\cdot\frac{(E_{on,n}+E_{off,n})}{V_{dc,n}I_n}\cdot V_{dc}I_i f_{sw}$$

Where T_n is the period time of the fundamental frequency, P_{on} and P_{off} are turn-on and turn-off power, E_{on} and E_{off} turn-on and turn-off energy, $E_{on,n}$ and $E_{off,n}$ turn-on and turn-off energy at $V_{dc,n}$ and I_n, given by the data sheet for the IGBT. f_{sw} is the switching frequency, V_{dc} the dc link voltage, and I_i the current through the IGBT.

In data sheets, E_{on} and E_{off} are given at specific values ($V_{dc,n}$ and I_n). The term $\frac{V_{dc} I_i}{V_{dc,n} I_n}$ compensates for that so the losses are given at V_{dc} and I_i.

The turn-on and turn-off losses for the freewheeling diodes of one half bridge, are calculated in a similar way. However, the losses for the freewheeling diodes may be approximated as the turn-off losses only. The turn-on losses for the diodes are small compared to the turn-off losses caused by the reverse recovery current during turn off.

$$\overline{P}_{sw,diode} = \frac{1}{T_n}\int_{T_n}(P_{on} + P_{off})dt = \frac{f_{sw}}{T_n}\int_{T_n}(E_{on} + E_{off})dt =$$
$$\approx \frac{E_{off,n}}{V_{dc,n} I_n} \cdot \frac{V_{dc} f_{sw}}{T_n} \cdot \int_{T_n} \left|\hat{i}_i \sin(wt - j)\right| dt = \qquad \text{Equation 2.6.3}$$
$$= \frac{2\sqrt{2}}{p} \cdot \frac{E_{off,n}}{V_{dc,n} I_n} \cdot V_{dc} I_i f_{sw} = \frac{2\sqrt{2}}{p} \cdot \frac{E_{Drr,n}}{V_{dc,n} I_n} \cdot V_{dc} I_i f_{sw}$$

Where $E_{Drr,n}$ is the reverse recovery energy at $V_{dc,n}$ and I_n, given by the data sheet for the diode.

Conduction losses

A method presented in [10] and [11] may be used to calculate the conduction losses for the half bridge. The calculations are made for one IGBT and one freewheeling diode. To get the losses for the whole half bridge, the result is multiplied by two.

First the conduction losses of the IGBT are calculated. To do that the forward voltage drop, $V_{IGBT(on)}$, of the IGBT is needed.

$$V_{IGBT(on)} = V_{IGBT,0} + R_{IGBT(on)} i_i \qquad \text{Equation 2.6.4}$$

Where $V_{IGBT,0}$ is the threshold voltage and $R_{IGBT(on)}$ is the on-state resistance. The duty cycle for $IGBT1$ is given by:

$$d_{IGBT1} = \frac{1}{2} + \frac{\hat{u}\sin(wt + j)}{V_{dc}}$$ Equation 2.6.5

The conduction loss for IGBT1 becomes:

$$P_{cond,IGBT1} = V_{IGBT(on)} \cdot i_i \cdot d_{IGBT1}$$ Equation 2.6.6

To calculate the average losses $\overline{P}_{cond,IGBT}$, $P_{cond,IGBT}$ in eq. 2.6.6 is integrated over a half period and divided by the whole period time. This is because IGBT1 is only conducting half of the period, i.e when the current is positive.

$$\overline{P}_{cond,IGBT} = \frac{1}{T_n}\int_0^{\frac{T_n}{2}} V_{IGBT(on)} \cdot i_i \cdot d_{IGBT1} dt$$ Equation 2.6.7

Using eq. 2.6.4 and eq. 2.6.5 results in:

$$\overline{P}_{cond,IGBT} = \frac{1}{T_n}\int_0^{\frac{T_n}{2}} \left(V_{IGBT,0} + R_{IGBT(on)} \cdot \hat{i}_i \cdot \sin(wt)\right)\left(\hat{i}_i \sin(wt)\right)\left(\frac{1}{2} + \frac{\hat{u}\sin(wt + j)}{V_{dc}}\right) dt$$
Equation 2.6.8

By solving eq. 2.6.8 , the result is:

$$\overline{P}_{cond,IGBT1} = \frac{\hat{i}_i V_{IGBT,0}}{2p} + \frac{\hat{i}_i^2 \cdot R_{IGBT(on)}}{8} + \frac{\hat{u}}{V_{dc}}\cos(j)\left(\frac{\hat{i}_i V_{IGBT,0}}{4} + \frac{2\hat{i}_i^2 R_{IGBT(on)}}{3p}\right)$$
Equation 2.6.9

The conduction losses for the freewheeling diode are calculated in a similar way:

The forward voltage for the diode is given by:

$$V_{diode(on)} = V_{diode,0} + R_{diode(on)} \cdot i_i$$

The duty cycle for diode2 differs from IGBT1 and is given by:

$$d_{diode2} = 1 - d_{IGBT1} = \left(\frac{1}{2} - \frac{\hat{u}\sin(wt + j)}{V_{dc}} \right)$$ Equation 2.6.10

The conduction loss for diode2 becomes:

$$P_{cond,diode2} = V_{diode(on)} \cdot i_i \cdot d_{diode2}$$ Equation 2.6.11

and the average losses:

$$\overline{P}_{cond,diode2} = \frac{1}{T_n} \int_0^{\frac{T_n}{2}} V_{diode(on)} \cdot i_i \cdot d_{diode2} dt$$ Equation 2.6.12

With the same calculations as for the IGBT this results in:

$$\overline{P}_{cond,diode2} = \frac{\hat{i}_i V_{diode,0}}{2p} + \frac{\hat{i}_i^2 \cdot R_{diode(on)}}{8} - \frac{\hat{u}}{V_{dc}} \cos(j) \left(\frac{\hat{i}_i V_{diode,0}}{4} + \frac{2\hat{i}_i^2 R_{diode(on)}}{3p} \right)$$

Equation 2.6.13

As mentioned before, the calculations of the conduction losses above only concerns *one* of the IGBTs and *one* of the diodes in the half bridge. To get the total conduction losses for the half bridge, the results must be multiplied by two.

Simulated continues converter losses

The methods described above for calculations of the losses are only usable during steady state and with sinusoidal output voltages and currents. Therefore, another method is used in the simulations of the converter. The methods above were however used to verify the results from the method below.

The losses are calculated in "real time" from voltages and currents achieved in the simulations. To clarify the calculations in eq. 2.5.14 - 2.6.25, fig. 2.6-4 shows a short sequence of the output voltage and the currents in IGBT1 and diode2 during operation.

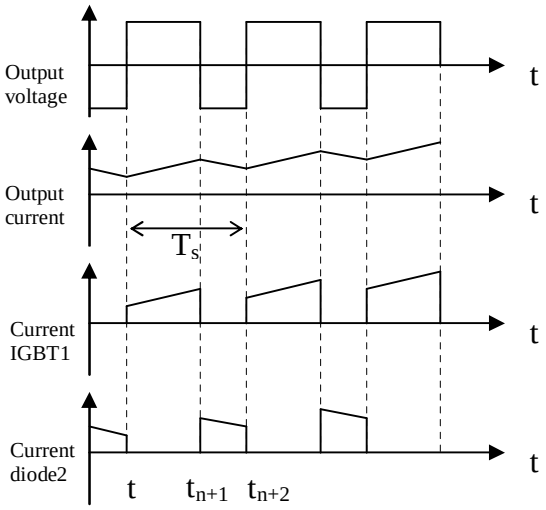


Figure 2.6-4. Output voltage and currents in IGBT1 and diode2 during operation.

During a switching interval T_{sw}, following calculations are made:

At t_n, turn-on loss energy of IGBT1 and turn-off loss energy of diode2:

$$E_{on\_IGBT1} = E_{on,n\_IGBT1} \cdot \frac{V_{dc} i_i}{V_{dc,n} I_n}$$ Equation 2.6.14

$$E_{off\_diode2} = E_{off,n\_diode2} \cdot \frac{V_{dc} i_i}{V_{dc,n} I_n}$$ Equation 2.6.15

At t_{n+1}, turn-off loss energy of IGBT1 and turn-on loss energy of diode2:

$$E_{off\_IGBT1} = E_{off,n\_IGBT1} \cdot \frac{V_{dc} i_i}{V_{dc,n} I_n}$$ Equation 2.6.16

$$E_{on\_diode2} = E_{on,n\_diode2} \cdot \frac{V_{dc} i_i}{V_{dc,n} I_n}$$ Equation 2.6.17

At t_{n+1}, conduction loss energy of IGBT1:

$$\overline{V}_{IGBT(on)} = V_{IGBT,0} + R_{IGBT(on)}\overline{i}_i$$ Equation 2.6.18

$$\overline{i}_i = \frac{i_i(t_n) + i_i(t_{n+1})}{2}$$ Equation 2.6.19

$$E_{cond,IGBT1} = \overline{i}_i \cdot \overline{V}_{IGBT(on)} \cdot (t_{n+1} - t_n)$$ Equation 2.6.20

At t_{n+2}, conduction loss energy of diode2:

$$\overline{V}_{diode(on)} = V_{diode,0} + R_{diode(on)}\overline{i}_i$$ Equation 2.6.21

$$\overline{i}_i = \frac{i_i(t_{n+1}) + i_i(t_{n+2})}{2}$$ Equation 2.6.22

$$E_{cond,diode2} = \overline{i}_i \cdot \overline{V}_{diode(on)} \cdot (t_{n+2} - t_{n+1})$$ Equation 2.6.23

At t_{n+2}, total loss during switching period:

The continuous power loss.

$$P_{loss} = \frac{E_{on,IGBT1} + E_{on,diode2} + E_{off,IGBT1} + E_{off,diode2} + E_{cond,IGBT1} + E_{cond,diode2}}{T_{sw}}$$

Equation 2.6.24

And the average power loss, during a specified time period T.

$$\overline{P}_{loss} = \frac{1}{T}\int^{T} P_{loss}(t)dt$$ Equation 2.6.25

Appendix D contains the m-file performing the loss calculations for the simulated converter.

2.6.4 Filter components

The switching causes harmonics. The harmonic content in the inductor currents and the output voltages are of two types: *Differential mode (DM) harmonics*, in (i_a, i_b, i_c) and (u_{ab}, u_{bc}, u_{ca}), and *common mode harmonics (CM)*, in u_n, (i_a, i_b, i_c) and i_n.

The DM harmonics in the line inductor currents (i_a, i_b, i_c) are attenuated by *L*. The CM harmonics in the line- and neutral inductor currents (i_a, i_b, i_c) and i_n are attenuated by $L + 3L_n$.

L and *C* forms a 2nd order low pass filter that attenuates the DM harmonics in the output voltages (u_{ab}, u_{bc}, u_{ca}). $L + 3L_n$ and *C* forms a 2nd order low pass filter that attenuates the CM harmonics in u_n.

The total harmonic contents in the inductor currents (i_a, i_b, i_c) and i_n, and the line to neutral output voltages (u_{an}, u_{bn}, u_{cn}) are calculated by adding the DM and CM harmonic spectra. This is not trivial and for the following simulated model of the converter the filter components are dimensioned based of results achieved in simulations.

2.6.5 Dc link capacitor

The design method is treated in Appendix A. The negative sequence load current is the limiting design constraint of the dc link capacitor. Eq. A.5 in Appendix A may thereby be used in dimensioning the dc link capacitor.

2.6.6 Dimensioning main components of the converter in the project

Specifications

- Output voltage: 3*230/400V
- Output frequency: 50Hz
- Nominal power: 50kVA

- Output maximum per phase power: $50/3\,\mathrm{kVA}$
- Load power factor: 0.2 - 1
- Max temperature cooling water (IGBT-modules): 70°C
- Switching frequency: 5kHz
- Max dc-link voltage: 750V.

Power electronic switches, phase half bridges

The switch modules needs to withstand the voltages and currents applied to them. With water cooling of the modules and a maximal water temperature of 70°C, the junction temperature of the modules is assumed to always be below 100°C. Since the DC-link voltage is 750V, 1200V IGBT-modules are needed.

The maximal line current is given by eq. 2.6.1 (Or the load scenarios in section 2.2). With $S_n = 50kVA$ and $U_{line-neutral} = 230V$, the maximal current is 72.2A (102A peak value).

IGBT-module, *Semikron SKM 200GB123D*, fulfills the requirements and is proposed for the project.

Power electronic switches, neutral half bridge

Except from the current level, the conditions for the switches of the neutral half bridge are the same as for the switches of the phase half bridges.

The maximal current however, is different. Load scenario 5, in section 2.2, covers the "worst" scenario for the neutral half bridge (within the specification above). The current through the neutral is then 134A (190A peak value).

IGBT-module, *Semikron SKM 300GB124D*, fulfills the requirements and is proposed for the project.

LC-filter components

The dimensioning of the filter components are based on results achieved in simulations. Following filter components provided a line-to-neutral load voltage ripple of 0.6%, a line-inductor current ripple of 6 A_{p-p} (3% at nominal power), and a neutral-inductor current ripple of 9 A_{p-p}.

C=33.8μF
L=3mH
Ln=1.5mH

The capacitors needs to withstand the voltage applied to them. In this case, 230V at 50 Hz. According to Hägglunds, long life time is important. Polypropylene film type capacitors are therefore to prefer before electrolytic capacitors.

Capacitor, *Epcos B323-C1356 35mF*, fulfills the requirements and is proposed for the project.

The inductors need to withstand the current through them. The maximal current through the line inductors, *L*, are 72.2A at 50Hz. The maximal current through the neutral inductor, *Ln*, is 134A at 50Hz.

Inductors, custom made by *Tramo ETV AB*, are proposed for the project.

DC-link capacitor

When designing the DC-link capacitor, concern has to be taken to the global demands of the dc-link voltage of the vehicle as well as the dc-link capacitance in the whole system. Hägglunds do not see this area as within the scope of this thesis. However, the method described in Appendix A may be used for the design.

The capacitor needs to withstand the applied voltage, in this case 750V DC. According to Hägglunds, long life time is important. The life time is largely depending of the currents (fundamental and harmonics) that will flow through the capacitor bank. This aspect is however not evaluated.

2.7 Control of the system

This section deals with issues concerning the control of the converter. The ultimate goal is to achieve a stable, balanced three-phase voltage, independent of the load conditions specified in section 2.2. Brought up subjects are for

example: PI-controllers, delays, feedback control in cascade, decoupling and feed-forward control.

2.7.1 Model of the system to control

The system which is the target of the control, is the one described in section 2.5.2 and fig. 2.5-3. The system is represented in the rotating d-q-0-coordinate system. From section 2.6, the values of the components are known as well.

Fig. 2.7-1 shows the system, now represented as a block schematic and expressed in Laplace.

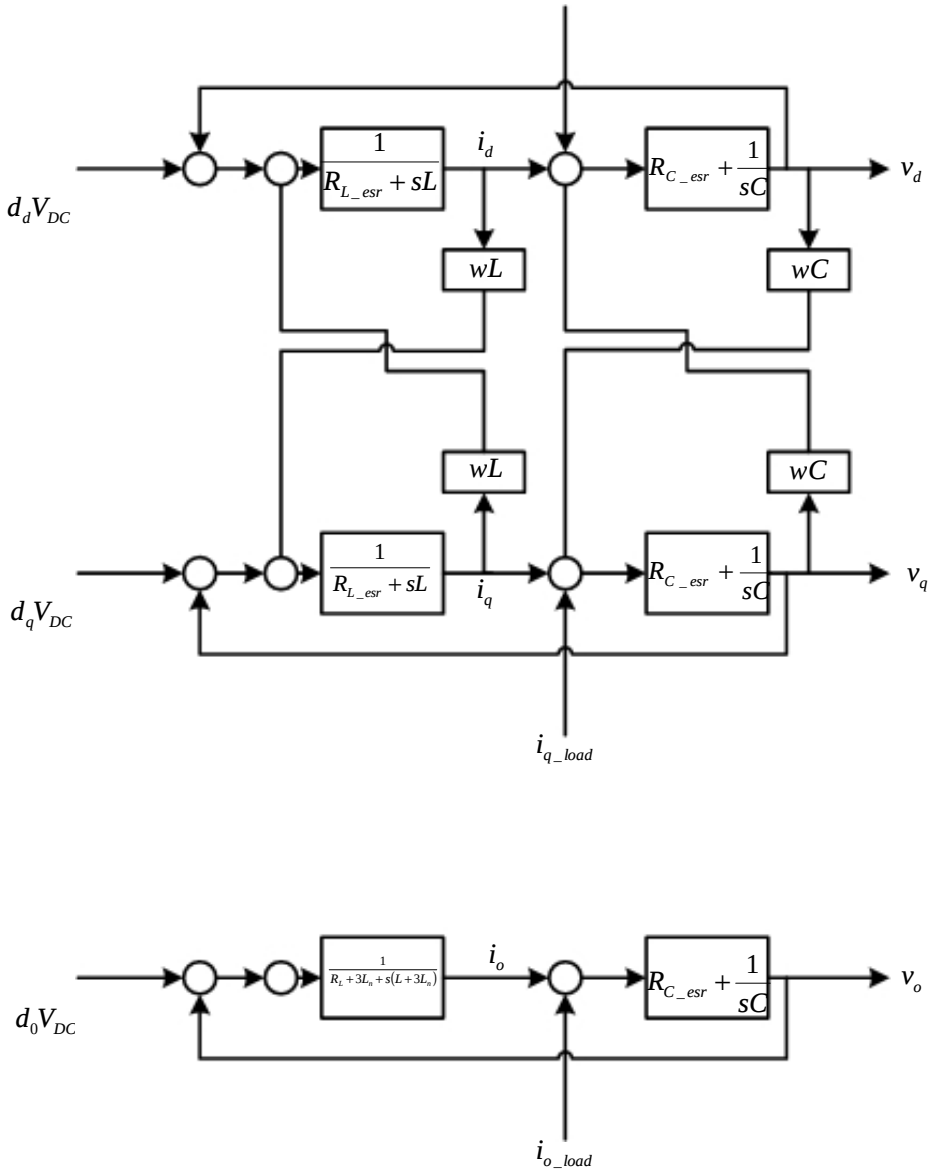


Figure 2.7-1.The system to control represented as a block schematic.

2.7.2 Delays

The control of the system will in a real converter be made digital. Due to the digital implementation there will be delays introduced in the control-loops. The transducer signals are low pass filtered and sampled and the digital signal processor will need time to calculate the new control signals.

According to section 5.2, the filtering, sampling, and calculation time will lead to a delay in the control signals of 1,4 sample periods. The delay is modeled as a dead time in the block schematic of the circuit model in fig. 2.7-2.

2.7.3 Voltage control

As mentioned before, the ultimate goal is to achieve a stable, balanced three-phase *load voltage*, independent of the load condition. The load current *will* however affect the system, as can be seen in fig. 105, and is considered as a disturbance in the control constraints.

The goal is to achieve the voltage in each channel (d, q and 0) to follows its respectively reference value, where d represents the reactive component, q represents the active component and 0 represents the zero component of the total voltage vector.

Considering the behavior of the control voltage vector during unbalance (described in section 2.1.6), different properties considering control bandwidth are preferred in the different channels. During balanced conditions only positive sequence exists. In d-q-0-coordinates a positive sequence will appear as a pure DC component in the d-, q- and 0-channels. During unbalance however, negative- and zero sequence exist as well. See section 2.1.5 and 2.1.6.

The *zero sequence* causes, in the d-q-0-system, an addition of a sinusoidal component, with the fundamental frequency, to the 0-channel.
The *negative sequence* causes, in the d-q-0-system, an addition of a sinusoidal component, with *twice* the fundamental frequency, to the d- and q-channels.

Since these sinusoidal components are caused by errors, who the control voltage vector is supposed to suppress, the controllers must be able to respond

to them. Because of this, it is appreciated to have a control bandwidth way above 50 Hz in the o-channel and 100 Hz in the d- and q-channels.

2.7.4 Control methods

To simplify the explanations of the control methods, first only one of the channels (channel d), is examined. With the cross coupling terms and load disturbances foreseen at the moment (dotted lines), fig. 2.7-2 shows how a single loop voltage control could be implemented in the system.

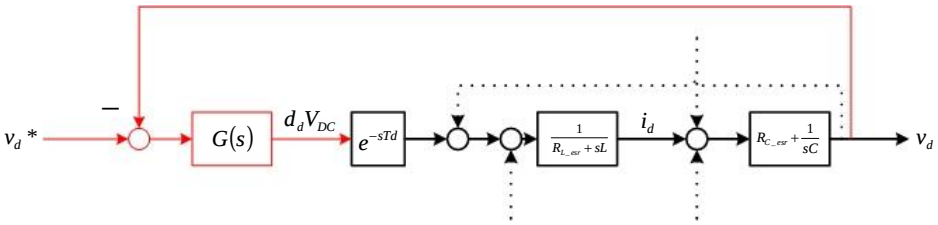


Figure 2.7-2.Channel d of the system (black), including the controller (red).

Single loop control

[4],[6] The system is, as described in section 2.5, a second order system, with the inductor current and the capacitor voltage as states. The converter output voltage, $(d_d \cdot V_{DC})$ which is the control signal for the total channel d system, affects the inductor current (i_d), which in turn affects the capacitor voltage (v_d), which is the output signal.

If, as in fig. 2.7-2, only the capacitor voltage state is measured and used for control, the closed loop transfer function for the system (with the delay block foreseen and the controller G(s) as a proportional controller with gain K) will be:

$$H_{CL}(s) = \frac{v_d(s)}{v_d^*(s)} = \frac{K(1+s\cdot C\cdot R_{C\_esr})}{s\cdot C(R_{L\_esr}+s\cdot L)+K(1+s\cdot C\cdot R_{C\_esr})}$$

Equation 2.7.1

Since R_{C_esr} and R_{L_esr} are small, the poles of this system are both close to the imaginary axis and by that the system is close to unstable. If R_{C_esr} and R_{L_esr} approaches zero, $H_{CL}(s)$ approaches:

$$H_{CL}(s) = \frac{v_d(s)}{v_d^*(s)} = \frac{K}{s^2 \cdot C \cdot L + K} \qquad \text{Equation 2.7.2}$$

Where the poles of the system both are *on* the imaginary axis.

With a purely proportional (P) or a proportional and integral controller (PI) this system is hard to stabilize (the bandwidth will be low). To achieve stability, the controller needs a derivative part (D). A derivative controller however, is sensitive to disturbances and noise. Since the capacitor voltage most certainly contains noise and ripple, the derivation of this is tricky.

There is a way around this problem. To derivate the capacitor voltage is actually the same thing as measuring the current through the capacitor. If the load current, which is seen as a disturbance and is dealt with by *feed forward control* (explained below) is foreseen, the current trough the capacitor is the same as the current trough the inductor. Therefore, as an alternative to the derivative controller, the inductor current, which is the other state in the system, may be measured and controlled as well as the capacitor voltage above. *By that a state feedback control from the two states inductor current and capacitor voltage is achieved,* and P or PI controllers will be adequate [4].

Cascade control

[6] A generalization of the method mentioned above, often used when there are different timescales in a system, is the cascade control. Cascade control means that two control loops, with different bandwidth, are used to control the system. The inner loop needs to be much faster than the slower outer loop. The inner loop should, from an outer loop point of view, react instantly (See fig. 2.7-3).

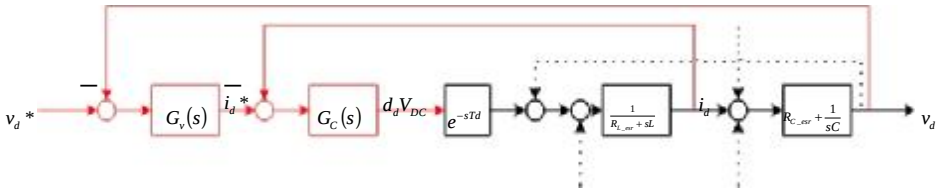


Figure 2.7-3. Channel d of the system (black), including the feedback controllers (red) connected in cascade.

The inductor current controller, which provides the converter voltage reference $d_d \cdot V_{DC}$ directly as control signal, can react quickly. Because of this, the inductor current control loop should be the inner loop. The capacitor voltage control, which uses the inductor current as control signal (and by that only indirectly is controlled by $d_d \cdot V_{DC}$), should be the outer loop and must, compared to the current loop, react slower.

In this way, when the outer voltage control loop senses an error in the output voltage, the voltage loop changes the reference value for the inner current loop, which with $d_d \cdot V_{DC}$ quickly sets the inductor current to a value that corrects the output voltage.

By using different bandwidth in the two control loops, they can be treated as two independent loops during design and by that simplify the control design significantly. Ideally, the current loop sees the voltage loop as stationary (very slow reaction) and the voltage loop sees the current loop as perfect current source (very fast reaction). The difference in bandwidth between the loops should preferably be at least one decade.

Current loop

When designing the inductor current controller, following simplification of the system, seen by the controller, can be made (See fig. 2.7-4).

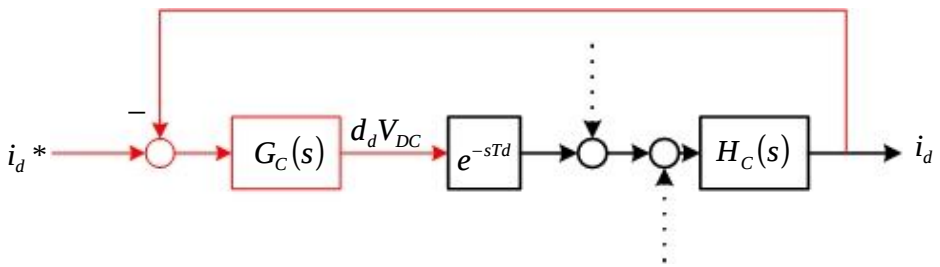


Figure 2.7-4.Simplified current loop of channel d. The system as the current controller sees it (black) and the controller (red).

The system may then be described as [6]:

$$H_{c\_tot}(s) = e^{-s \cdot T_d} \cdot H_c(s) = e^{-s \cdot T_d} \cdot \frac{1}{R_{L\_esr} + s \cdot L} = e^{-s \cdot T_d} \cdot \frac{1/R_{L\_esr}}{1 + s\frac{L}{R_{L\_esr}}}$$

Equation 2.7.3

Where the delay T_d is caused by the lowpass filter, the digital control and the PWM.

By using a PI controller:

$$G_c(s) = Kc_P \cdot \frac{1 + s \cdot Tc_i}{s \cdot Tc_i} \qquad \text{Equation 2.7.4}$$

Where Kc_P is the proportional part and Tc_i is the integral time of the PI controller, the open loop transfer function of the system including controller, will be:

$$G_c(s) \cdot H_{c\_tot}(s) = Kc_P \cdot \frac{1 + s \cdot Tc_i}{s \cdot Tc_i} \cdot e^{-s \cdot T_d} \cdot \frac{1/R_{L\_esr}}{1 + s\frac{L}{R_{L\_esr}}} \qquad \text{Equation 2.7.5}$$

And the closed loop transfer function for the system will be:

$$H_{C\_CL}(s) = \frac{G_C(s) \cdot H_{C\_tot}(s)}{1 + G_C(s) \cdot H_{C\_tot}(s)} \qquad \text{Equation 2.7.6}$$

By tuning the values of Kc_P and Tc_i until the phase margin for the open loop transfer function is about 50 degrees and the step response for the closed loop transfer function looks nice, the current controller can be considered tuned.

This is preferably done by simulating the system above with *Matlab Control Toolbox*, until the result is satisfying.

Voltage loop

When designing the capacitor voltage controller, the following simplification of the system, seen by the controller, is made (See fig. 2.7-5). The current loop is here modeled as the dynamic of the closed loop transfer function of the current loop above.

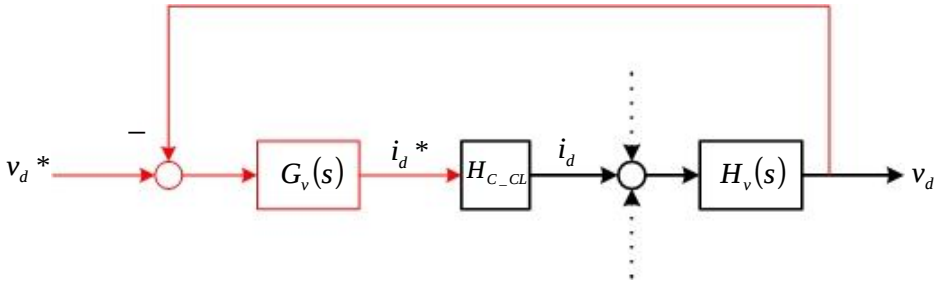


Figure 2.7-5 Simplified voltage loop of channel d. The system as the voltage controller sees it (black) and the controller (red).

The system may then be described as:

$$H_{v\_tot}(s) = H_{C\_CL}(s) \cdot H_v(s) = H_{C\_CL}(s) \cdot (R_{C\_esr} + \frac{1}{s \cdot C}) = H_{C\_CL}(s) \cdot \frac{1 + s \cdot R_{C\_esr} \cdot C}{s \cdot C}$$

Equation 2.7.7

By using a PI controller:

$$G_v(s) = Kv_P \cdot \frac{1 + s \cdot Tv_i}{s \cdot Tv_i}$$ Equation 2.7.8

Where Kv_P is the proportional part and Tv_i is the integral time of the PI controller, the open loop transfer function of the system including controller, will be:

$$G_v(s) \cdot H_{v\_tot}(s) = Kv_P \cdot \frac{1 + s \cdot Tv_i}{s \cdot Tv_i} \cdot H_{C\_CL}(s) \cdot \frac{1 + s \cdot R_{C\_esr} \cdot C}{s \cdot C}$$

Equation 2.7.9

And the closed loop transfer function for the system will be:

$$H_{v\_CL}(s) = \frac{G_v(s) \cdot H_{v\_tot}(s)}{1 + G_v(s) \cdot H_{v\_tot}(s)} \qquad \text{Equation 2.7.10}$$

By tuning the values of Kv_P and Tv_i until the phase margin for the open loop transfer function is about 50 degrees and the step response for the closed loop transfer function looks nice, the voltage controller can be considered tuned.

As with the current controller, this is preferably done by simulating the system above with *Matlab Control Toolbox,* until the result is satisfying.

Compensation of the disturbance signals.

Until now, no concern has been taken to the disturbance signals in the model caused by the capacitor voltages (load voltages), the load currents and the cross coupling terms (see fig. 2.7-6). During the design of the feedback controllers, the disturbance signals were assumed to be neutralized by other methods. These methods are now dealt with.

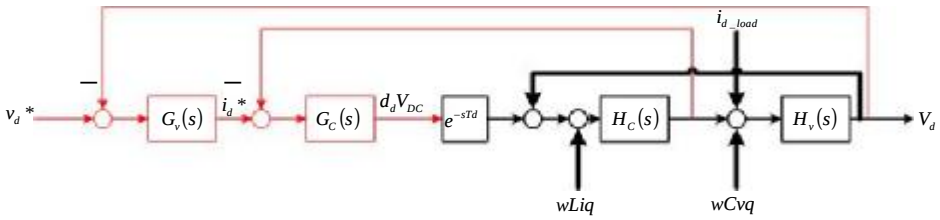


Figure 2.7-6 .Channel d of the system (black), including the disturbance signals (highlighted) and the feedback controllers connected in cascade (red).

Decoupling

The method of reducing the interconnection between the channels d and q is called *decoupling*. For simplicity, still only channel d is studied. The control system in fig. 2.7-6, is in fig. 2.7-7 extended with the decoupling control signal paths.

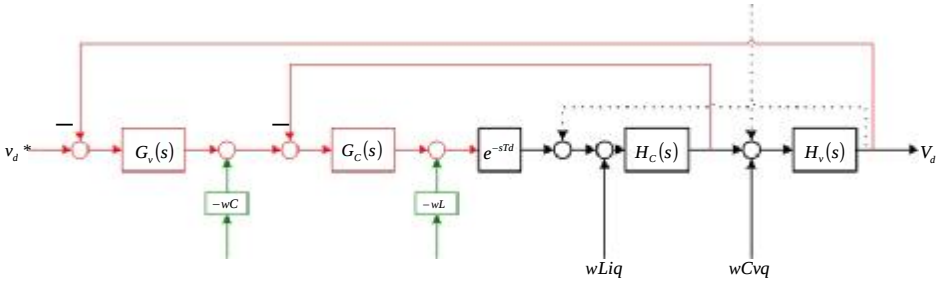


Figure 2.7-7.Channel d of the system (black), including the feedback controllers connected in cascade (red) and the decoupling control signal paths (green).

Referring to fig. 2.7-7, the influence of the cross coupling signals $w \cdot C \cdot v_{q\_load}$ and $w \cdot L \cdot i_q$, may be reduced by measuring and use the capacitor voltage v_q and the inductor current i_q from channel q. By multiply them with the known $w \cdot C$ and $w \cdot L$ and add the product (with opposite sign compared to the cross coupling terms) to the control signals from the voltage controller and the current controller respectively, the decoupling signals reduce the cross coupling terms.

Feed forward control

The method of reducing the impacts from the load currents and the load voltages (capacitor voltages) is called *feed forward control*. For simplicity, still only channel d is studied. The control system in fig. 2.7-7, is in fig. 2.7-8 extended with the feed forward control signal paths.

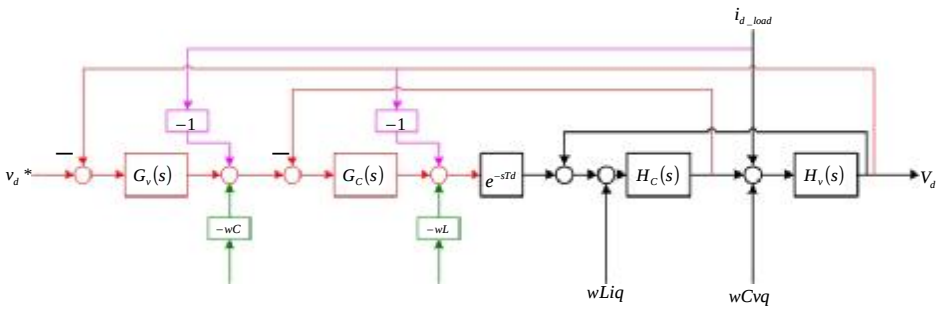


Figure 2.7-8.Channel d of the system (black), including the feedback controllers connected in cascade (red), the decoupling control signal paths (green) and the feed forward control signal paths (purple).

Referring to fig. 2.7-8, the influence of the load disturbances in v_q and i_{q_load} may be reduced by measuring and adding them (with opposite sign compared to the load disturbance signals) to the control signals from the voltage

controller and the current controller respectively. The feed forward signals will then reduce the influence from the load disturbances.

Sensors

To be able to use the control methods mentioned above, some measurements of voltages and currents in the converter are needed. How many sensors to use is a trade-off between control possibilities and costs. The methods used above will require following signals to be measured:

The current control loops: The inductor currents
The voltage control loops: The capacitor voltages
The decouplings: The inductor currents and the capacitor voltages.
The feed forward controls: The capacitor voltages and the load currents.

For calculations of the duty-cycles, the dc-link voltage must be measured as well.

Since the system is a four wire system, the measurements needs to be done on all three phases. So, to be able to use all methods mentioned above, three inductor currents, three capacitor voltages, three load currents and the dc link voltage need to be measured. In total ten sensors.

2.7.5 Model of the system, including controllers and delays

Now, when more is known of the total system, including all control methods and delays, the earlier schematic of the system in fig. 2.7-1 can be extended to the schematic in fig. 2.7-9.

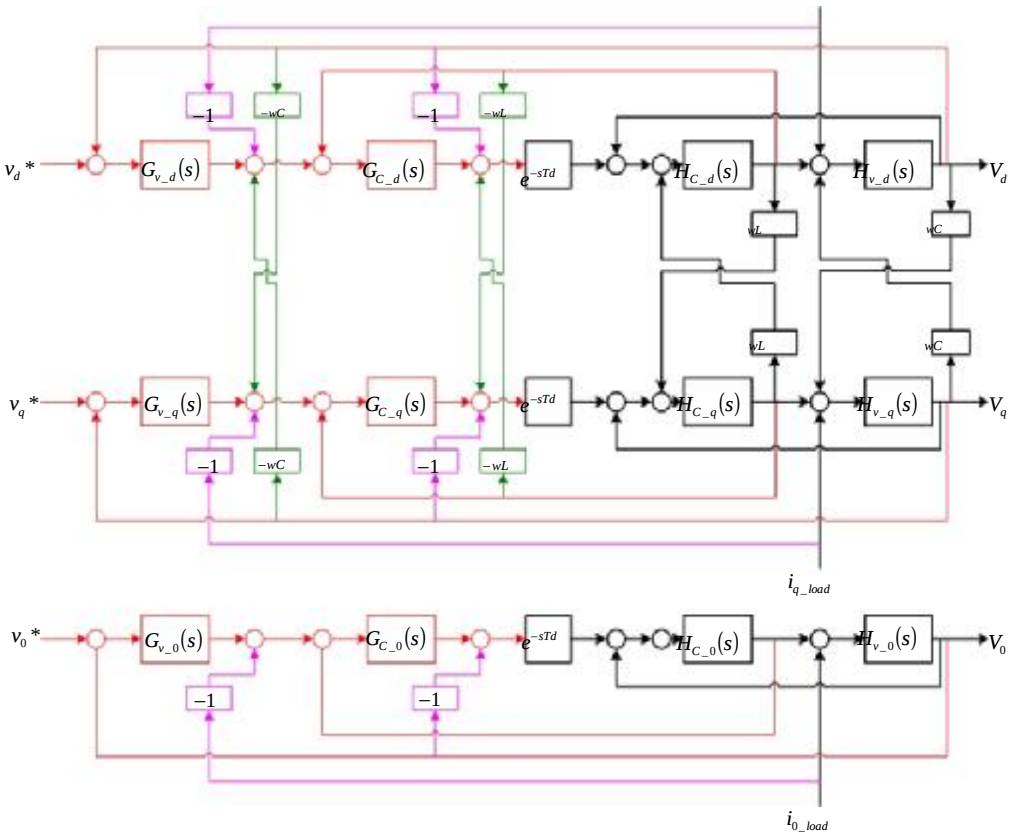


Figure 2.7-9.The total system to be controlled (black), including the feedback controllers connected in cascade (red), the decoupling control signal paths (green) and the feed forward control signal paths (purple).

2.7.6 Parameters of the controllers

By using the methods described above and simulating the control loops one by one, following suitable parameters for the PI-controllers are obtained:

	Channel d	Channel q	Channel 0
Kc_P	12	12	40
Tc_i	0.022	0.022	0.089
Kv_P	0.075	0.075	0.11
Tv_i	0.00047	0.00047	0.00047

Table 2.7-1. Parameters PI_controllers.

From simulations, the best results (in response and stability) are achieved with following feed forward- and decoupling terms:

- A factor 1 of the load voltages (in d, q and 0) for the feed forward control.

- A factor 1 of the converter currents (in d and q) for the calculations of the decoupling terms.
- A factor 0.8 of the load currents (in d, q and 0) for the feed forward control.
- A factor 0.8 of the load voltages (in d and q) for the calculations of the decoupling terms.

3. Method

The main object for the project is of cause to find out how the converter might be expected to work. Until now, only basic theoretical issues have been dealt with.

Section 2.1 covered the basics for three phase systems and different ways to represent them. Section 2.2 covered expected load scenarios. Section 2.3 and 2.4 covered the principals for three and four legged converters. Section 2.5 described the three-phase circuit model of the converter, including filter and load, as well as the transformation of the whole system from a-b-c- to d-q-0-coordinates for control issues. Section 2.6 dealt with the dimensioning of dc-link voltage, switches, switching frequencies and filters. Section 2.7 covered the theory of suitable control methods for the converter.

Finally, it is time to see what this theory might be used for in a simulation model of the converter. This chapter deals with the structure of the model, what the different blocks does and the theory that has been used building them.

3.1 The simulink model of the converter

The model of the system (see fig 3.1-1) is built in Matlab and Simulink. These tools are user friendly, give a nice graphical presentation of calculations and signal routings and are very useful for the purpose.

This section only covers the basic function of each block and the signals entering and leaving the block. There are also references to where in the thesis the theory of the block is covered. The blue colored blocks are simulating software implementations, while the orange colored blocks are simulating physical hardware implementations. Detailed layouts of the model are presented in appendix B.

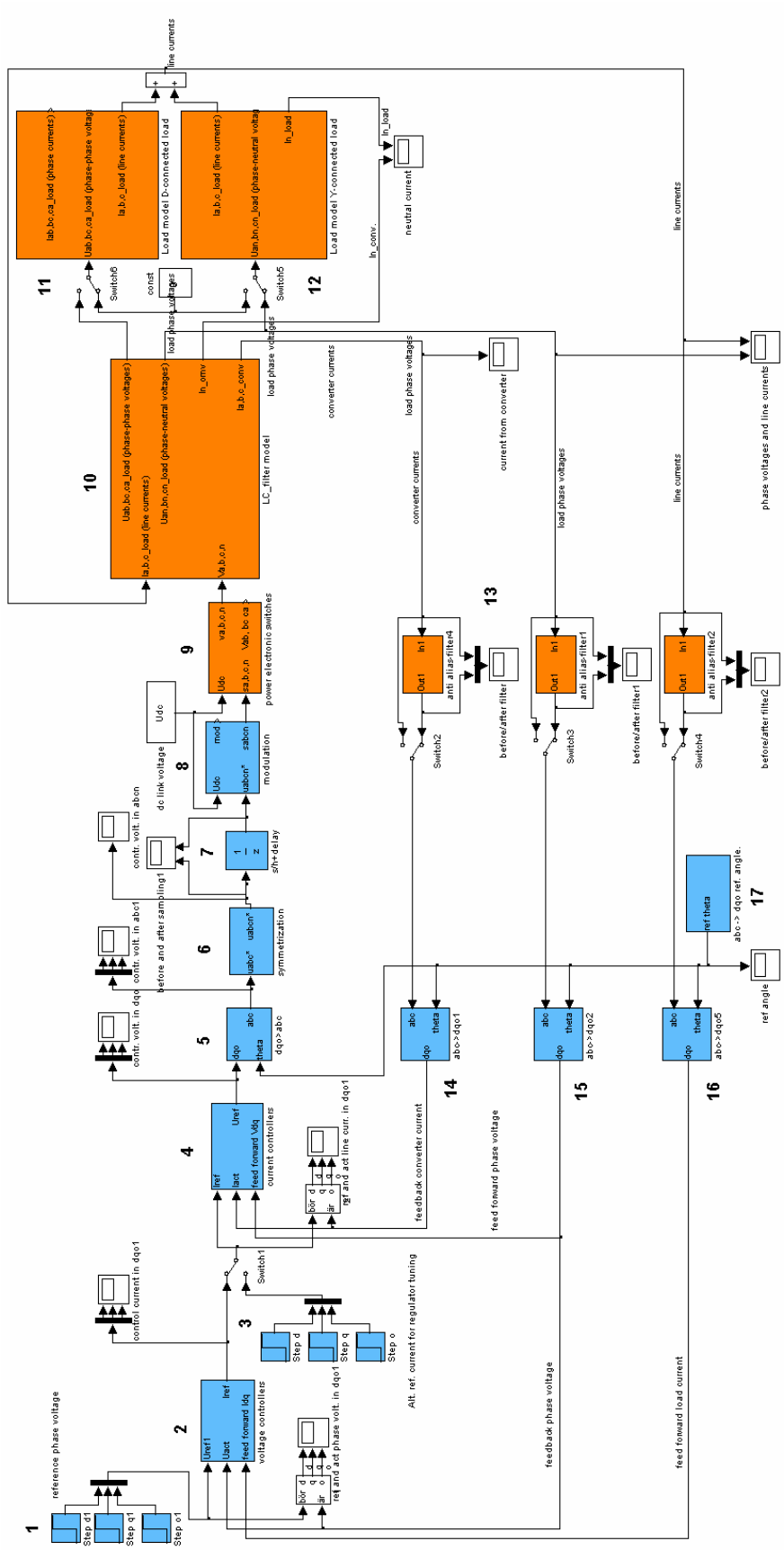


Figure 3.1-1. Layout of the simulink model.

Block 1.

The phase-neutral reference voltages in channel d, q and 0 are created here. See section 2.1.5 and 2.1.6 for information about d-q-0-representation.

Block 2.

This block contains the voltage controllers for channel d, q and 0 respectively. Section 2.7, and especially section 2.7.4, gives information about the used control methods.

The voltage controllers are the *outer loop* controllers in the cascade control. The feedback controllers are of PI-type (eq. 2.7.8). They use the differences between the reference voltage signals from block 1 and the measured output voltages from the converter, as input signals (error signals). The signals they return works as the reference current signals for the inner loop current controllers in the following block 4.

The block also contains the decoupling and load current feed-forward functions, whose signals are added to the signals from the voltage PI-controllers.

A function called anti-windup is integrated in the block as well. Windup occurs when the control error remains for a longer time and the integral part of the PI-controller becomes very large. Anti-windup puts a limit to the maximal value of the signal contribution from the integral part of the PI-controller.

Block 3.

During tuning of the regulator parameters of the current controllers (the inner loop controllers), is it useful to disconnect the outer voltage loop. Then the reference values for the currents in channel d, q and 0 are provided here.

Block 4.

This block contains the current controllers for channel d, q and 0 respectively. Section 2.7, and especially section 2.7.4, gives information about the used control methods.

The current controllers are the *inner loop* controllers in the cascade control. The feedback controllers are of PI-type (eq. 2.7.8). They use the differences

between the reference current signals from the voltage controllers in block 2 and the measured converter currents, as input signals (error signals). The signals they return works, after some modifications, as the reference voltage in the pulse width modulation later in block 8.

The block also contains the decoupling and output voltage feed-forward functions, whose signals are added to the signals from the current PI-controllers.

The anti-windup function is integrated in this block as well. (See *Block 2* above).

The final function of the block is a limitation of the output signals. Since the dc-link voltage limits the attainable output voltages there is no use in providing the pulse width modulator with higher reference voltages.

Block 5.

This block transforms the reference voltage signals in channel d, q and 0 to control voltage signals for phase a, b and c (section 2.1.5, eq. 2.1.21). The rotating reference angle is attained from block 17.

Block 6.

This block extracts the zero sequence component from the reference voltage signals of phase a, b and c (See fig. 3.1-2). The zero sequence component is also recalculated for symmetrized modulation (described in section 2.3.3, eq. 2.3.3 - 2.3.6).

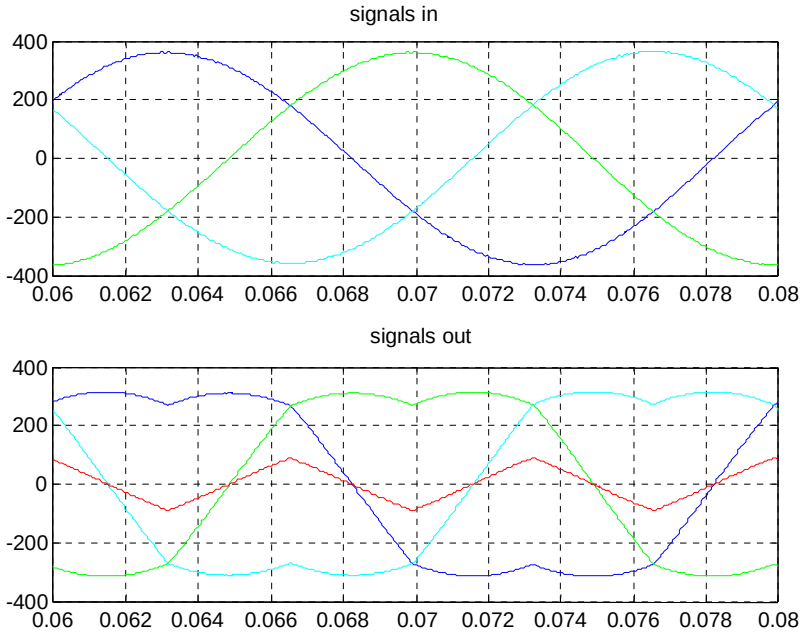


Figure 3.1-2. Reference signals into (above) and out of (below) block 6, symmetrization.

Block 7.

This block simulates the effects of a digital control (see section 5.1). The reference signals, which until here have been continuous, are sampled and delayed one sample period (See fig. 3.1-3). The delay is added because it is assumed the digital signal processor needs one sample period to calculate the new reference signals.

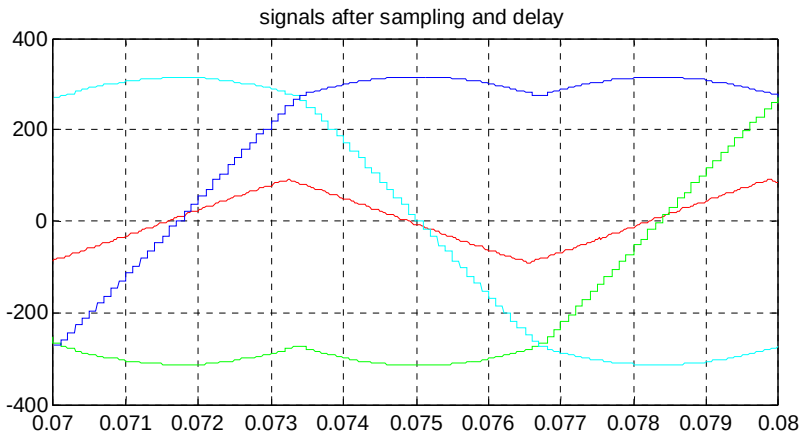


Figure 3.1-3. Reference signals out of block 7, sampling and delay.

Block 8.

The pulse-width modulation (PWM) is performed here. The carrier wave (the triangular wave) is created and compared to the reference voltages of phase a, b and c. The output signals are the switch signals (duty cycles) for the power electronic switches. The signals are represented as pulse trains (See fig. 3.1-4). Section 2.3.2 covers the theory of the PWM.

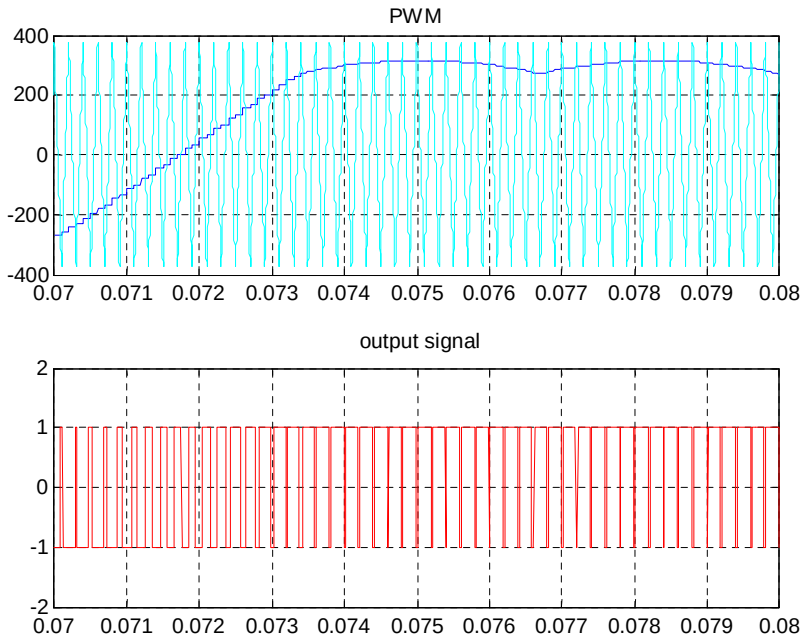


Figure 3.1-4. Pulse width modulation of phase a. Reference signal and carrier wave (above), output signal to the power electronic switches (below).

Block 9.

This block simulates the power electronic switches. The input signals are the pulse trains provided by block 8. The outputs (v_a, v_b, v_c, v_n) are voltage pulses of $\pm V_{DC}/2$ with the duty-cycles provided from the input signals (see section 2.3.2 and fig. 2.5.1).

Block 10.

This block simulates the 2:nd order LC-filters of the converter. The voltage pulses provided from block 9 are filtrated to achieve output voltages and currents at the fundamental frequency as well as with low ripple. Section 2.5.1 covers the circuit schemes (fig. 2.5-1) and equations for the filters. The filter model is based on equations 2.5.1-2.5.4.

Fig. 3.1-5 and 3.1-6 shows examples of voltages and currents in phase a of the filter during a simulation. Compare them with the circuit schematic in fig. 2.5-1.

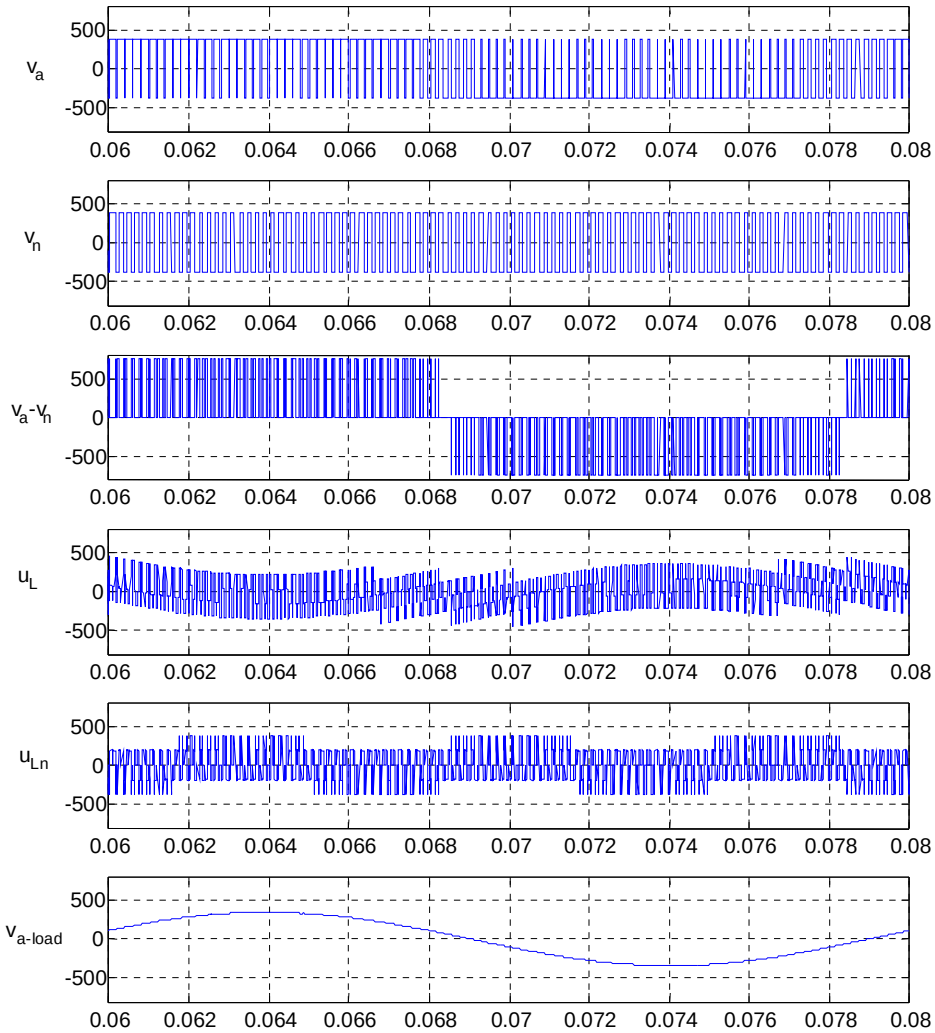


Figure 3.1-5. Voltages in the LC-filter of the converter.
From top to bottom: v_a, v_n, v_{an}, u_L, u_{Ln},v_{a_load}.

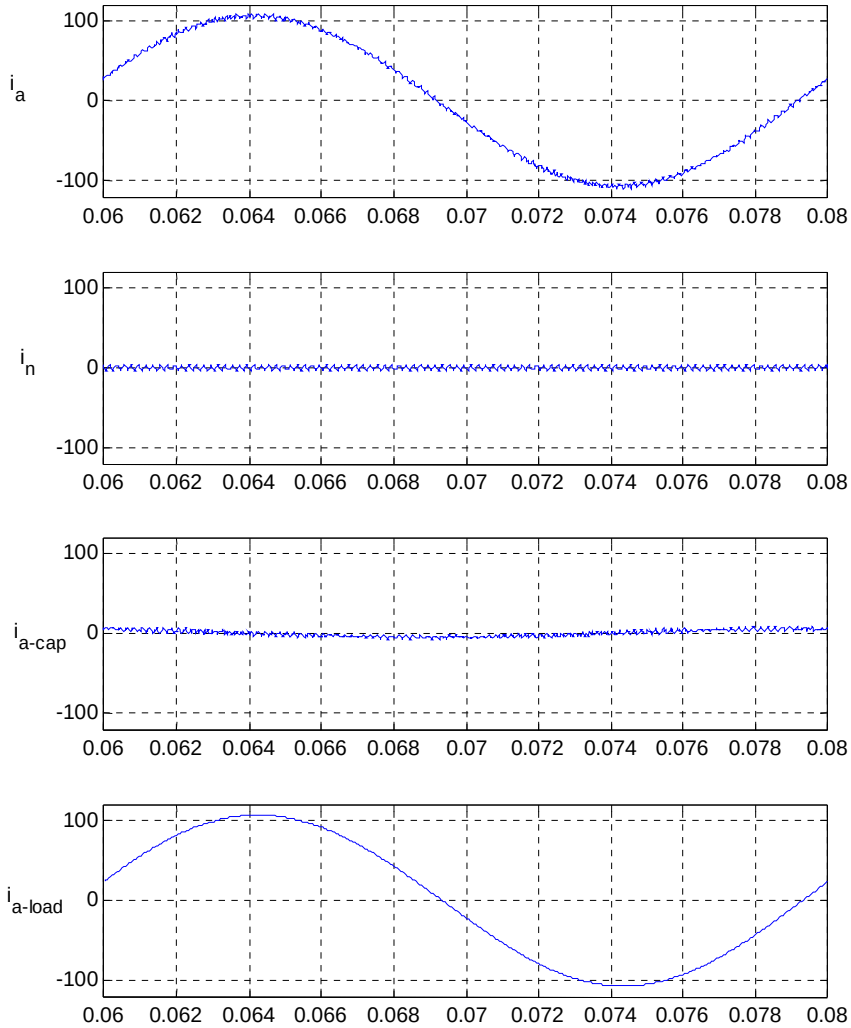


Figure 3.1-6. Currents in the LC-filter of the converter.
From top to bottom: i_a, i_n, i_{a_cap}, i_{a_load}.

Block 11 and 12

Block 11 and 12 simulates loads connected to the converter. Block 11 is a Δ-connected load model and block 12 is a Y-connected load model. They calculate the load currents corresponding to the voltage applied to the load models. (See section 2.5.1 and eq. 2.5.5) The loads may be made resistive, inductive, balanced or unbalanced, constant or variable in time as steps.

Block 13.

These blocks low pass filter the signals measured for control purposes. The reason for the filters in a real converter is to avoid aliasing (see section 5.1). The reason for adding the filters to the model as well is that they, in a real converter, add some delay to the measured signals, which may affect the control. The filters are modeled as 2:nd order Bessel filters with cut-off frequencies at half the switching frequency.

Block 14.

This block transforms the measured and filtered converter currents (i_a, i_b, i_c in fig 2.5-1) for phase a, b and c to d-q-0-coordinates (see section 2.1.5, eq. 2.1.20). The converter currents are used for the feedback control of the inner current loop (see section 2.7.4).

Block 15.

This block transforms the measured and filtered load voltages (v_{a_load}, v_{b_load}, v_{c_load} in fig 2.5-1) for phase a, b and c to d-q-0-coordinates (see section 2.1.5, eq. 2.1.20). The load voltages are used for the feedback control of the outer voltage loop and the feed forward to the output of the current controllers (see section 2.7.4).

Block 16.

This block transforms the measured and filtered load current (i_{a_load}, i_{b_load}, i_{c_load} in fig 2.5-1) for phase a, b and c to d-q-0-coordinates (see section 2.1.5, eq. 2.1.20). The load voltages are used for the feed forward to the output of the voltage controllers (see section 2.7.4).

Block 17.

This block provides the rotating reference angle used in the coordinate transformations between a-b-c- and d-q-0-coordinates (See fig. 3.1-7).

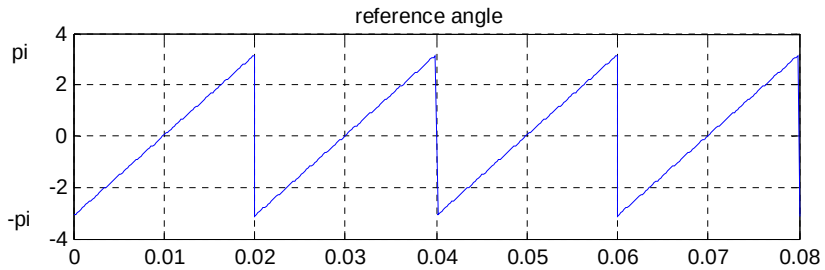


Figure 3.1-7. Reference angle for the creation of the rotating d-q-0-coordinate system.

3.2 Simulations and tests

The simulations of the Simulink model will be based on the five load scenarios specified in section 2.2 and the dimensioning of the components made in section 2.6.6.

3.2.1 Simulated load scenarios

The loads are all connected line to neutral (balanced or unbalanced Y-connection).

The load currents $(i_{a\_load}, i_{b\_load}, i_{c\_load})$ are shown in the circuit scheme of the converter in fig. 2.5-1. The load impedances (Z_a, Z_b, Z_c) are calculated from eq. 2.5.5, where $(v_{a\_load}, v_{b\_load}, v_{c\_load})$ are the ideal line to neutral load voltages.

		I_{a_load} (current (A)/ powerfactor)	I_{b_load} (current (A)/ powerfactor)	I_{c_load} (current (A)/ powerfactor)	Z_a (imedance (Ω)/ pf)	Z_b (imedance (Ω)/ pf)	Z_c (imedance (Ω)/ pf)
Scenario 1	Before step:	0 A/ 1	0 A/ 1	0 A/ 1	∞ Ω	∞ Ω	∞ Ω
	After step:	72.2 A/ 1	72.2 A/ 1	72.2 A/ 1	3.17 Ω / 1	3.17 Ω / 1	3.17 Ω / 1
Scenario 2	Before step:	0 A/ 0.2	0 A/ 0.2	0 A/ 0.2	∞ Ω	∞ Ω	∞ Ω
	After step:	72.2 A/ 0.2	72.2 A/ 0.2	72.2 A/ 0.2	3.17 Ω/ 0.2	3.17 Ω/ 0.2	3.17 Ω/ 0.2
Scenario 3	Constant load:	72.2 A/ 0.8	0 A	0 A	3.17 Ω/ 0.8	∞ Ω	∞ Ω
Scenario 4	Before step:	72.2 A/ 0.8	36.1 A/ 0.8	36.1 A/ 0.8	3.17 Ω/ 0.8	6.34 Ω/ 0.8	6.34 Ω/ 0.8
	After step:	36.1 A/ 0.8	0 A	0 A	6.34 Ω/ 0.8	∞ Ω	∞ Ω
Scenario 5	Constant load:	72.2 A/ 1	0 A	72.2 A/ 0.2	3.17 Ω / 1	∞ Ω	3.17 Ω / 0.2

Table 3.2-1. Simulation scenarios based on the load scenarios specified in section 2.2.

3.2.2 Settings of simulated converter model

To be able to repeat the simulations, one need to know the settings for the model when the simulations are performed. They are presented below:

Misc. data:

Dc-link voltage	750 V
Reference phase-neutral load voltage	230 V
Switching frequency	5 kHz
Sampling frequency	10 kHz

LC-filter:

Inductance line inductors	3 mH
Parasitic resistance line inductors	0.1 Ω
Inductance neutral inductor	1.5 mH
Parasitic resistance line inductors	0.1 Ω
Capacitance line to line capacitors	33.8 μF
Parasitic resistance (ESR) capacitors	0.1 Ω

Current controller (inner loop controller):

Kp feedback controller (d and q)	12
Ti feedback controller (d and q)	0.022
Kp feedback controller (0)	40
Ti feedback controller (0)	0.089
Max control signal	375 V
Min control signal	-375 V

A factor 1 of the load voltages (in d, q and 0) is used for the feed forward control.
A factor 1 of the converter currents (in d and q) is used in the calculations of the decoupling terms.

Voltage controller (outer loop controller):

Kp feedback controller (d and q)	0.075
Ti feedback controller (d and q)	0.00047
Kp feedback controller (0)	0.11
Ti feedback controller (0)	0.00047

A factor 0.8 of the load currents (in d, q and 0) is used for the feed forward control.
A factor 0.8 of the load voltages (in d and q) is used in the calculations of the decoupling terms.

Software

The simulink model is included in appendix B and the initiation file in appendix C. The used initiation file is init_ver050726.m and the used simulation model is converter_ver050726.mdl. Appendix D contains the file losscalc.m, performing the loss calculations for the converter.

4. Results

This chapter presents the results from the simulations described in chapter 3. From each of the five simulated scenarios following data are provided:

- Line to neutral load voltages (output voltage) of each phase.
- Line currents in each phase.
- Current in the neutral conductor.
- Control voltage in d, q and 0.
- Control voltage and load voltage (output voltage) in the a - b - g - coordinate system. (The data providing the plots are measured when steady state is achieved during t = 0.10-0.12s.)

More detailed presentations of the control signals during the simulations are provided in appendix E. Losses in the semiconductors are presented in appendix F.

Scenario 1

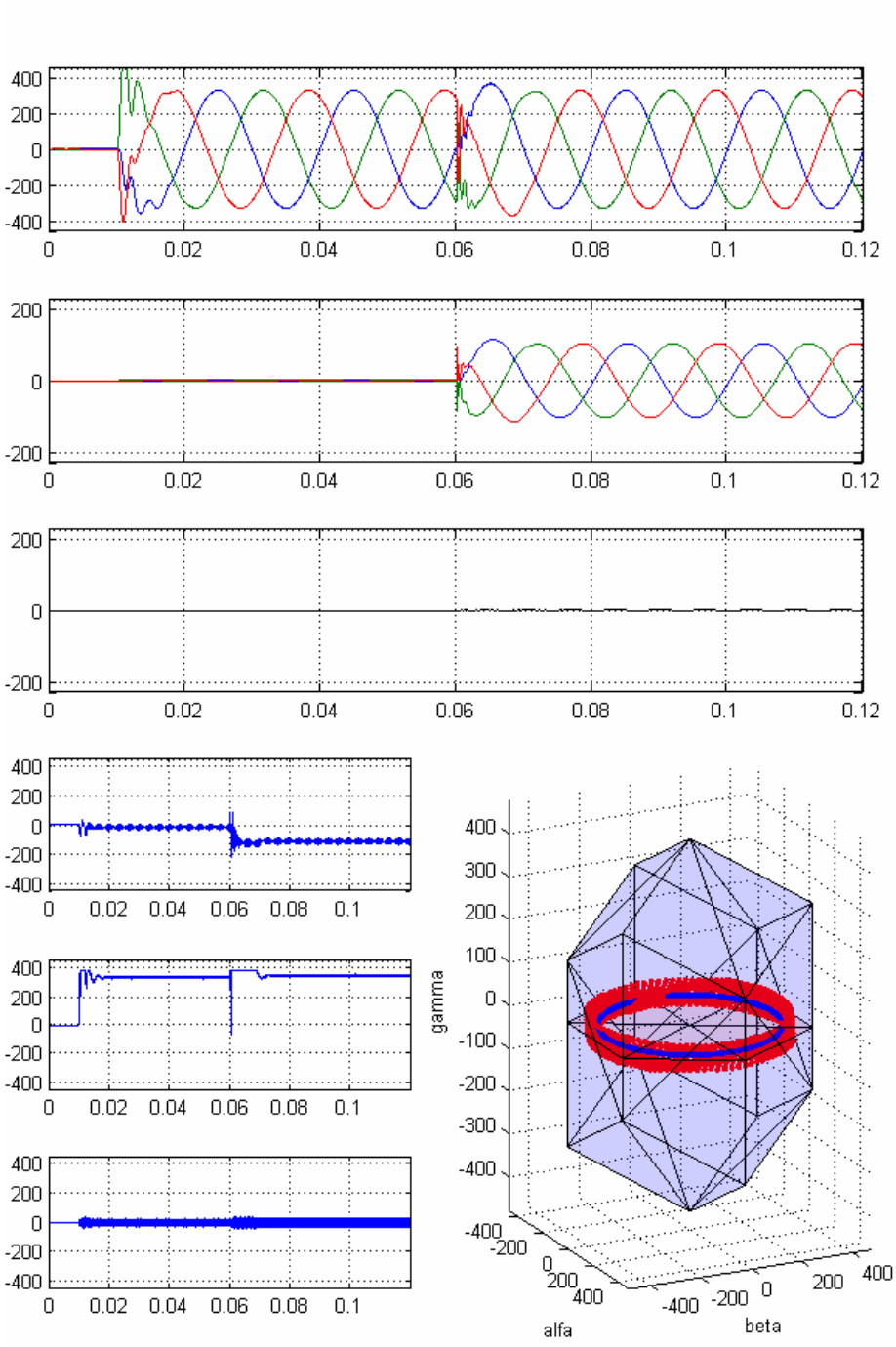


Figure 5.1-1.

The three plots on top (from top):
Line to neutral load voltages (output voltage) of each phase, line currents in each phase, and current in the neutral conductor.

The three plots below left (from top):
Control voltage in d, control voltage in q, and control voltage in 0.

The plot below right:
Control voltage (red) together with load voltage (output voltage) (blue) in the a *-* b *-* g *- coordinate system.*

- Due to oscillations in the LC-filter, some transients occur in the output voltage during start at t=0.01s (peaking at 560 V), but the output voltage is stabilized when t = 0.02s.
- The load is connected at t = 0.06s. At t = 0.07s the output voltage is again stabilized at 230V (325V peak value).
- The load currents are 72A (102A peak value).
- There is no current flowing through the neutral.

The converter model copes well with this load scenario.

Scenario 2

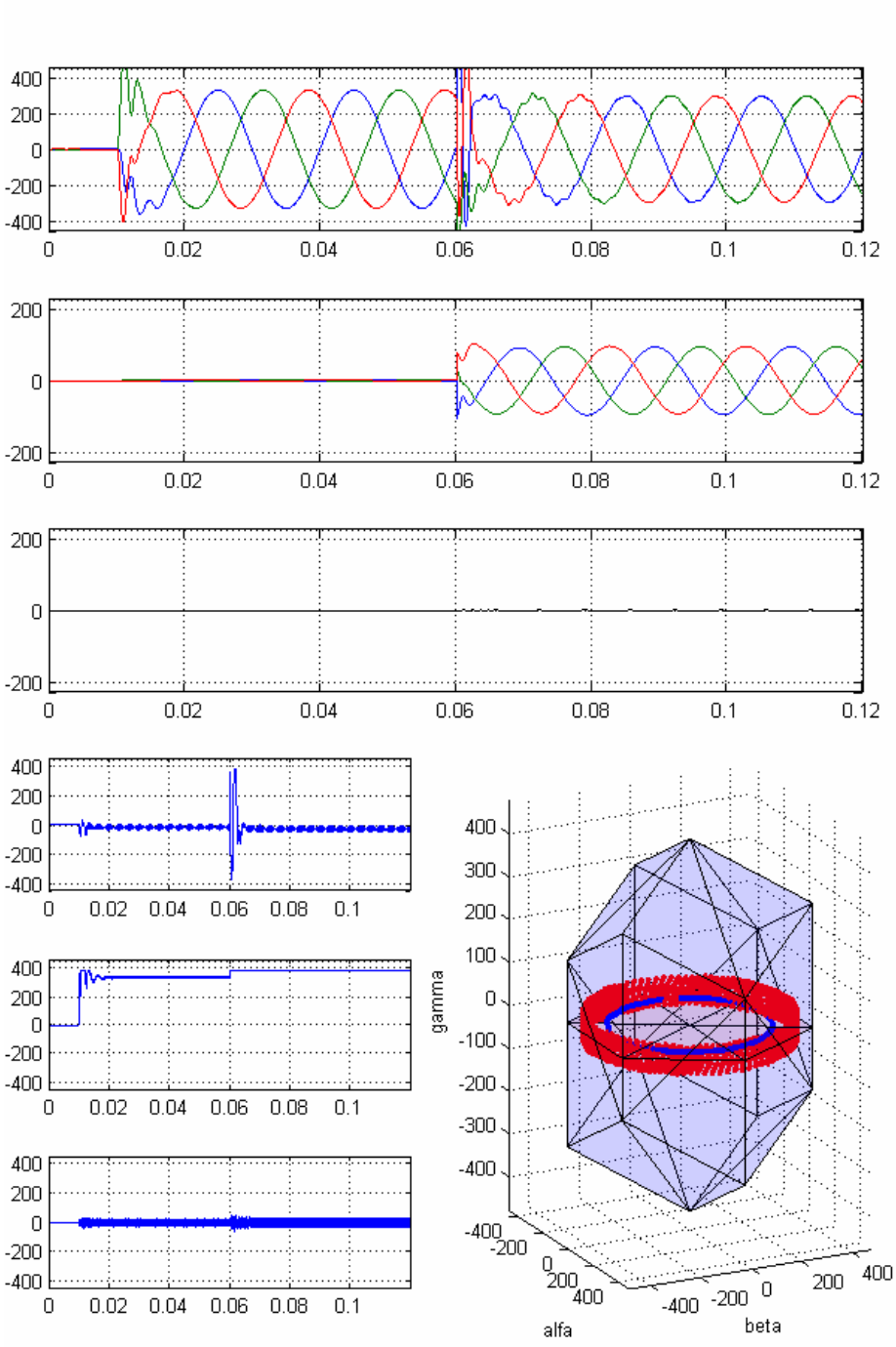


Figure 5.1-2.

The three plots on top (from top):
Line to neutral load voltages (output voltage) of each phase, line currents in each phase, and current in the neutral conductor.

The three plots below left (from top):
Control voltage in d, control voltage in q, and control voltage in 0.

The plot below right:
Control voltage (red) together with load voltage (output voltage) (blue) in the a *-* b *-* g *- coordinate system.*

- Due to oscillations in the LC-filter, some transients occur in the output voltage during start at t=0.01s (peaking at 560 V), but the output voltage is stabilized when t = 0.02s.

- The load is connected at t = 0.06 s. There are once again transients (peaking at 860 V). At t = 0.08 s the output voltage is stabilized, but not at the rated voltage of 230V. The output voltage only reaches 208V (294V peak value). The control voltage (of channel q) saturates because the available dc-link voltage is to low.

- The load currents are 66A (93A peak value).

- There is no current flowing through the neutral.

The converter model has some problems keeping the output voltage at rated level.

Scenario 3

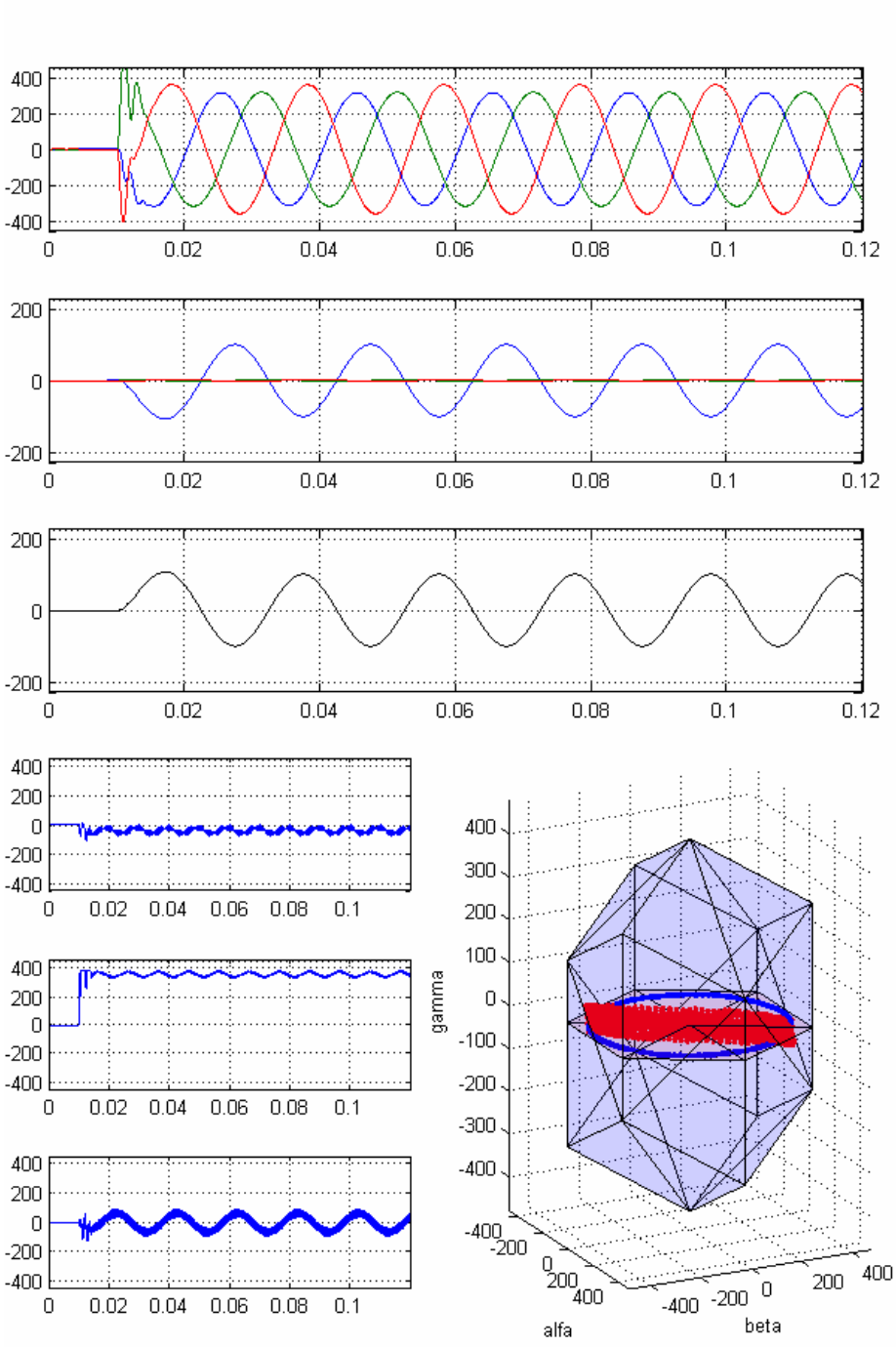


Figure 5.1-3.

The three plots on top (from top):
Line to neutral load voltages (output voltage) of each phase, line currents in each phase, and current in the neutral conductor.

The three plots below left (from top):
Control voltage in d, control voltage in q, and control voltage in 0.

The plot below right:
Control voltage (red) together with load voltage (output voltage) (blue) in the a *-* b *-* g *- coordinate system.*

- Due to oscillations in the LC-filter, some transients occur in the output voltage during start at t=0.01s (peaking at 560 V), but the output voltage is stabilized when t = 0.02s.

- Due to the unbalance there are voltage oscillations in channel d, q and 0 of the control voltage (100 Hz in d and q and 50 Hz in 0) and the control of the converter is put on test. It can bee seen that the converter copes quite well in controlling the output voltages. However, there are deviations. The output voltages vary between 223 – 251V (315 -355V peak value).

- The load current of phase a is 70A (99A peak value).

- Since only phase a is connected to a load, the current in phase a (70 A) flows back through the neutral connection.

The converter model controls the output voltages quite well. There are however deviations between the voltages of the different phases. Due to the unbalanced load, current is flowing through the neutral connection.

Scenario 4

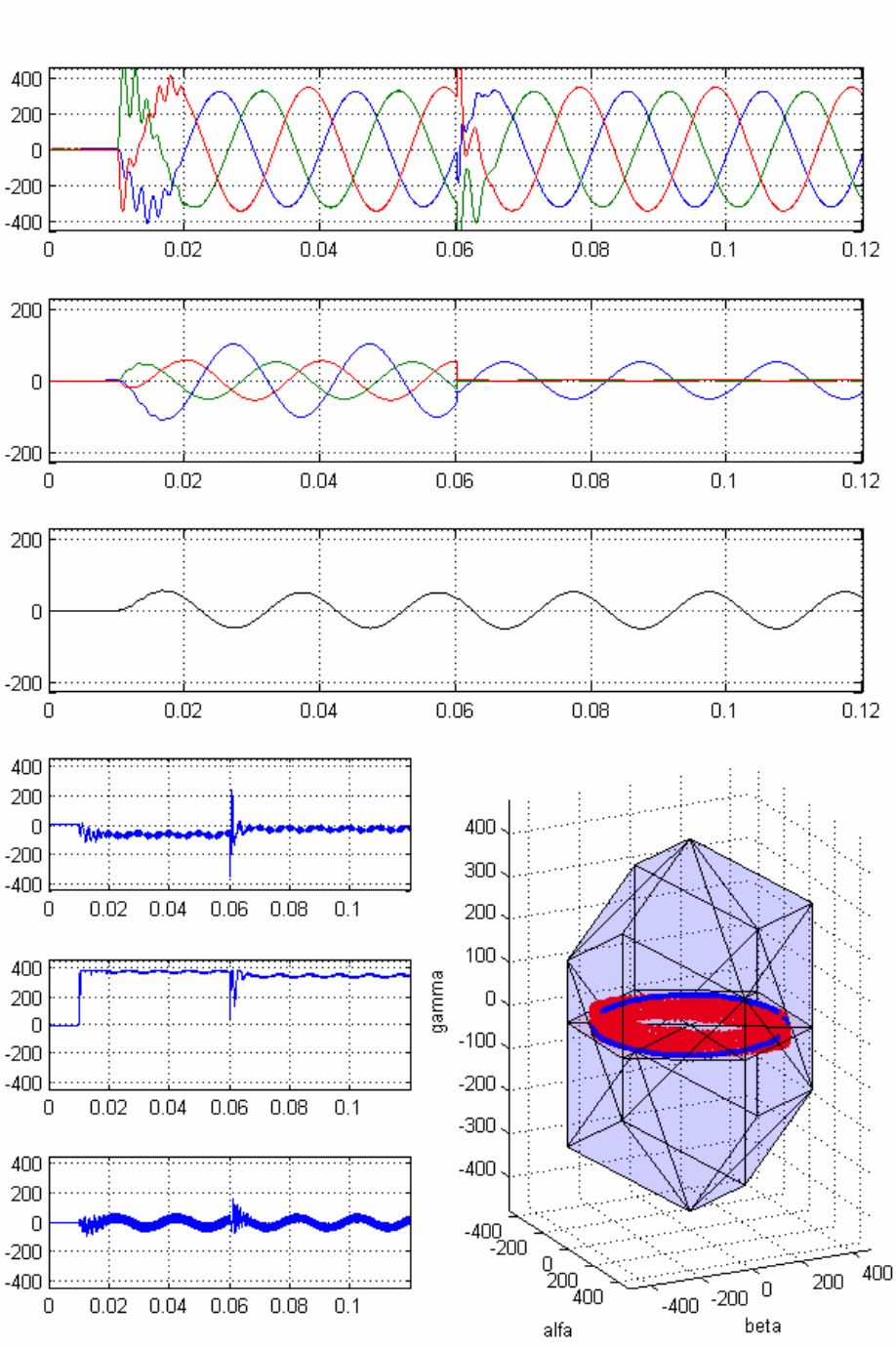


Figure 5.1-4.

The three plots on top (from top):
Line to neutral load voltages (output voltage) of each phase, line currents in each phase, and current in the neutral conductor.

The three plots below left (from top):
Control voltage in d, control voltage in q, and control voltage in 0.

The plot below right:
Control voltage (red) together with load voltage (output voltage) (blue) in the a *-* b *-* g *- coordinate system.*

- Due to oscillations in the LC-filter, some transients occur in the output voltage during start at t=0.01s (peaking at 470 V), but the output voltage is stabilized when t = 0.02s. In this scenario a load is connected from start.

- Due to the unbalance there are voltage oscillations in channel d, q and 0 of the control voltage (100 Hz in d and q and 50 Hz in 0). It can be seen that the converter copes quite well in controlling the output voltages. However, there are errors. The output voltages vary between 225 – 240V (318 -340V peak value).

- The load currents are 36A, 38A and 71A (51A, 54A and 100A peak value).

- The current trough the neutral connection is 35A (49A peak value).

- A t = 0.06 s the change in the load occur. There are once again transients (peaking at 680 V). At t = 0.07s the output voltage is stabilized, but there are still errors in the output voltages. They vary between 226 – 240V (320 -340V peak value).

- The load current in phase a is now 36A (51A peak value).

- Since now only phase a is connected to a load, the current in phase a (36 A) flows back though the neutral connection.

Also in this case the output voltages look nice. There are however deviations between the voltages of the different phases during both of the load scenarios. Due to the unbalanced loads, current is flowing through the neutral connection.

Scenario 5

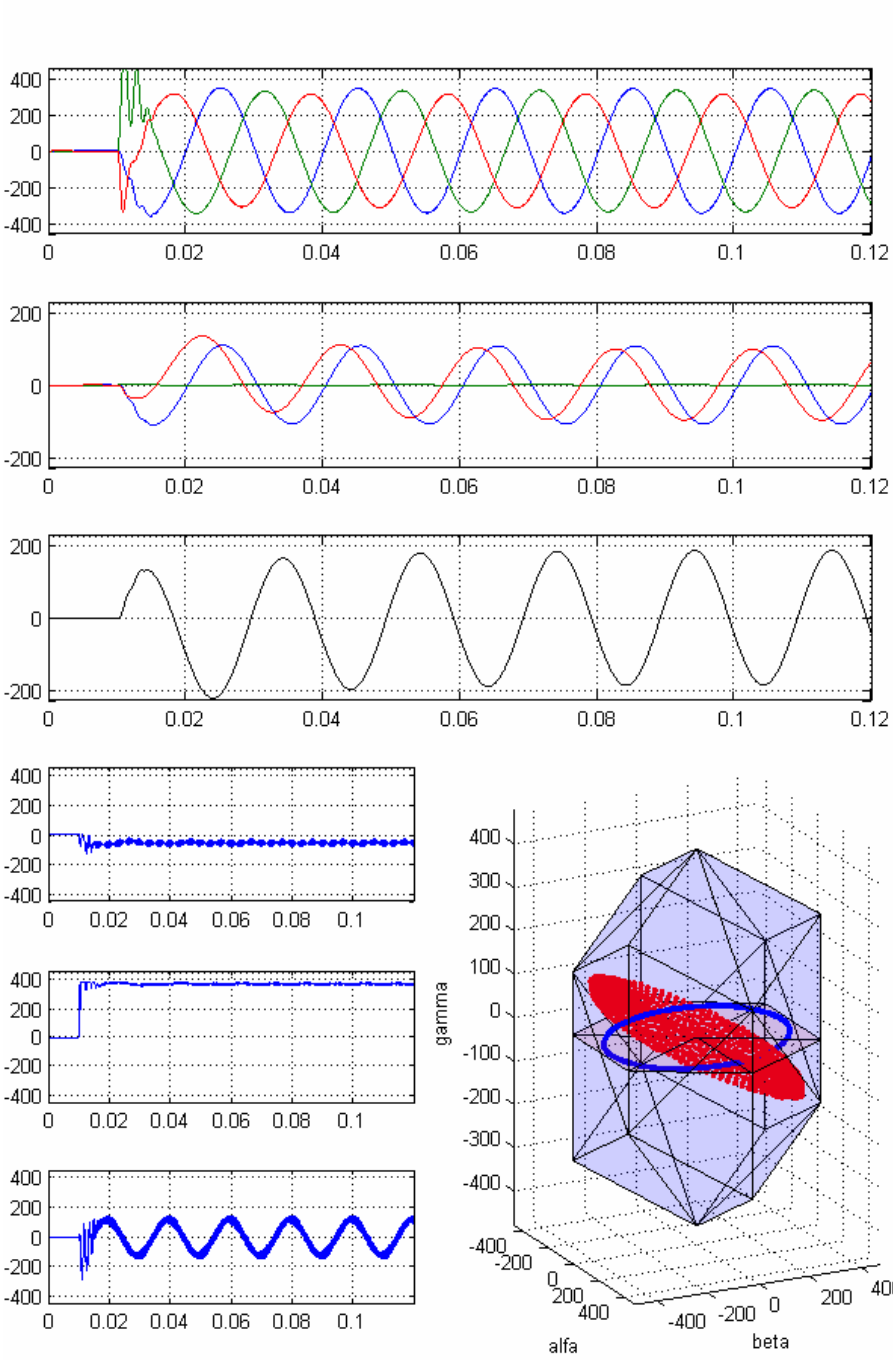


Figure 5.1-5.

The three plots on top (from top):
Line to neutral load voltages (output voltage) of each phase, line currents in each phase, and current in the neutral conductor.

The three plots below left (from top):
Control voltage in d, control voltage in q, and control voltage in 0.

The plot below right:
Control voltage (red) together with load voltage (output voltage) (blue) in the a *-* b *-* g *- coordinate system.*

- Due to oscillations in the LC-filter, some transients occur in the output voltage during start at t=0.01s (peaking at 550 V), but the output voltage is stabilized when t = 0.02s.

- Due to the unbalance there are voltage oscillations in channel d, q and 0 of the control voltage (100 Hz in d and q and 50 Hz in 0). It can be seen that the converter copes quite well in controlling the output voltages. However, there are errors. The output voltages vary between 219 – 240V (310 -340V peak value).

- The load currents are 69A and 75A (97A and 106A peak value).

- The current trough the neutral connection is 129A (182A peak value).

The converter model controls the output voltages quite well. There are however deviations between the voltages of the different phases. Due to the heavy unbalanced load, a large current is flowing through the neutral connection.

Effects of low dc link voltage

To see the effects of a too low dc link voltage two more simulations are performed.

The first scenario is the same as the later part of scenario 1, but with the difference that the dc link voltage starts to decrease at t = 0,04 (see fig. 5.1-6).

At t = 0.072 the converter starts to lose the control of the output voltage and the control voltage (of channel q) saturates. At this point the dc link voltage is 571V. Since the minimal dc link voltage is calculated to 564V (section 2.6.2) and some voltage is lost in the filters, this seems reasonable.

The same simulation was performed on scenario 5, with similar result (see fig. 5.1-7).

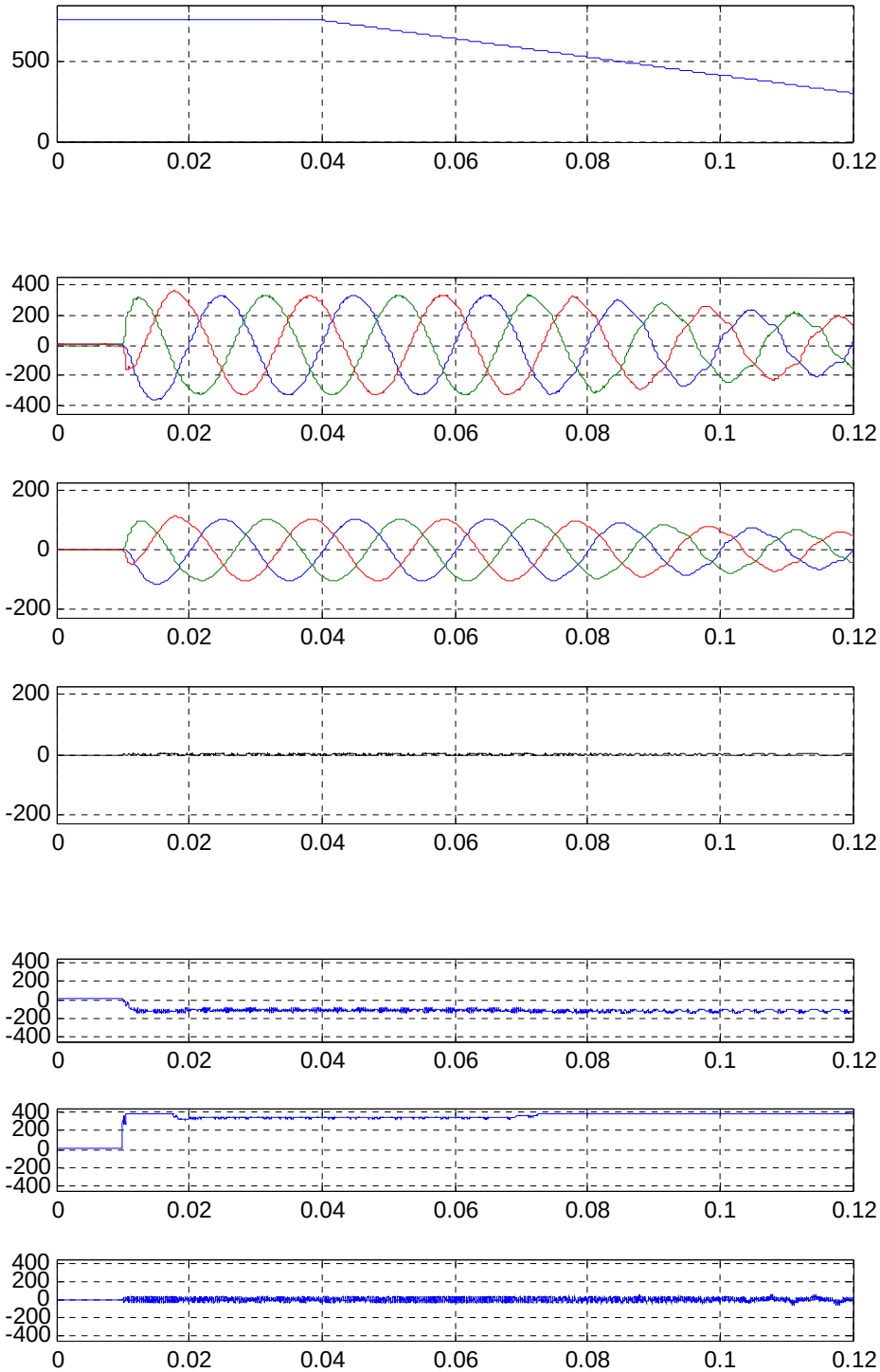


Figure 5.1-6.

The plot on top:
Dc link voltage.

The three following plots (from top):
Line to neutral load voltages (output voltage) of each phase, line currents in each phase, and current in the neutral conductor.

The three plots below (from top):
Control voltage in d, control voltage in q, and control voltage in 0.

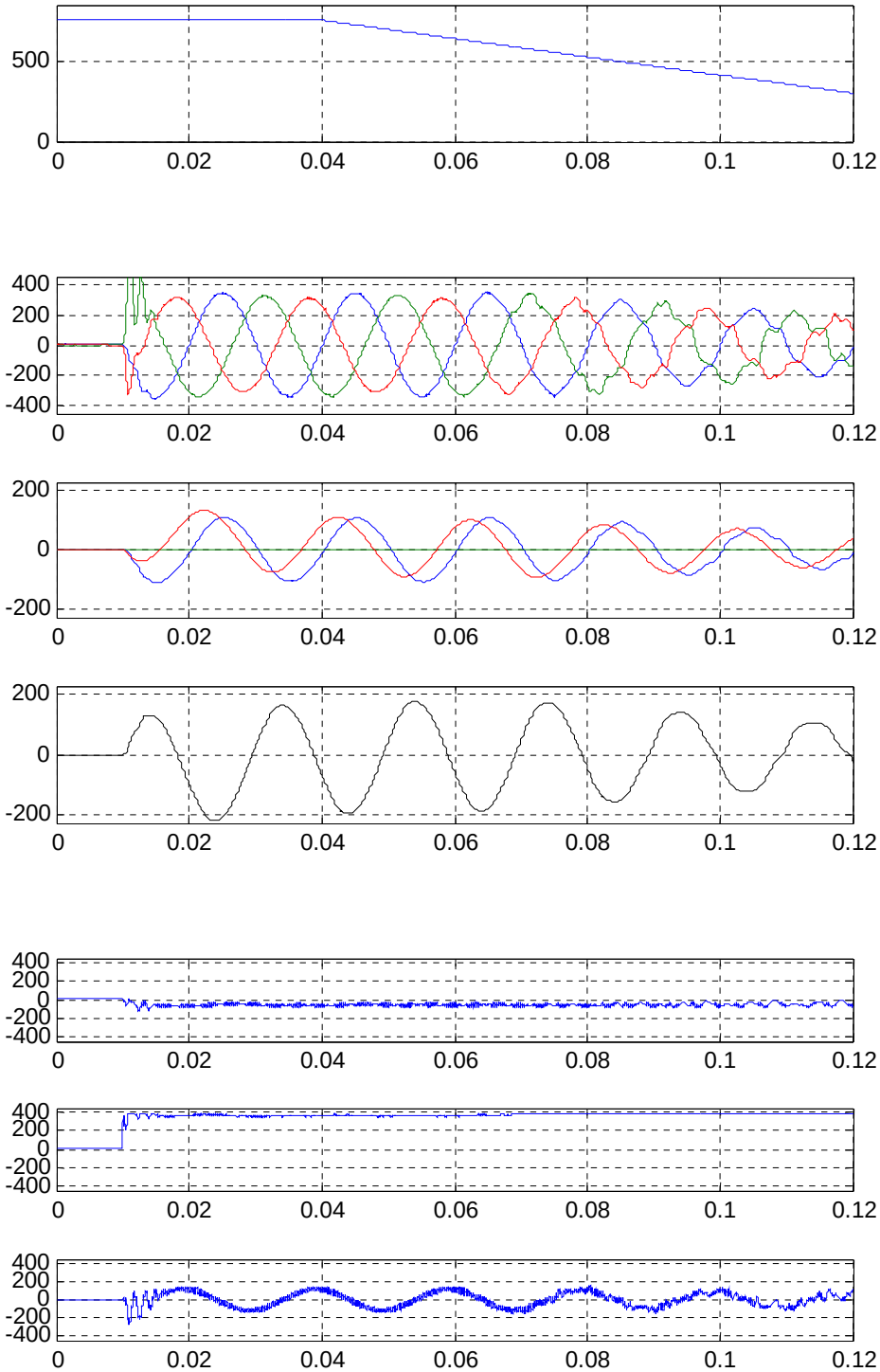


Figure 5.1-7.

The plot on top:
Dc link voltage.

The three following plots (from top):
Line to neutral load voltages (output voltage) of each phase, line currents in each phase, and current in the neutral conductor.

The three plots below (from top):
Control voltage in d, control voltage in q, and control voltage in 0.

5. Implementation

This chapter concerns the implementation of a physical converter in short. For example, some issues concerning an implementation of a digital controller are covered. The chapter also includes suggestion of what hardware to use for the main components in the design.

5.1 Digital control

All control methods in section 2.7 are made with continuous controllers. The control algorithms for a real converter will however most probably be made digital and calculated by a digital signal processor (DSP). Because of this some phenomenon concerning the digitalization of the control needs to be considered. This section will in short mention subjects like: sampling, anti-alias, delays, digital PI-controllers, digital algorithms and "dummy" software code.

Sampling

The measured signals (for example the inductor currents or the output voltages) will be sampled (See fig. 5.1-1).

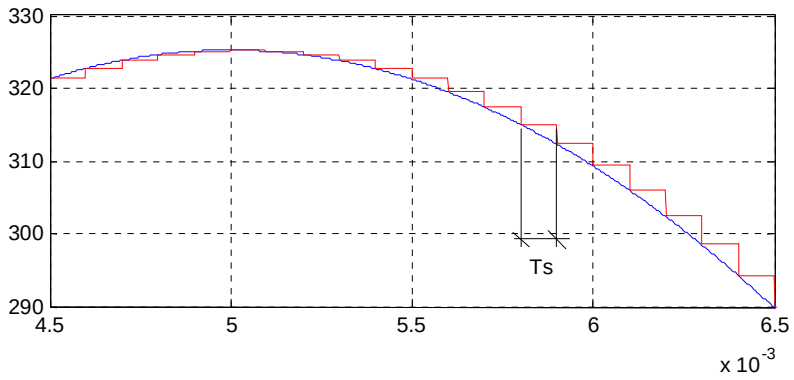


Figure 5.1-1.Sampling of the measured signals.

The sampling will be at a rate twice the switching frequency of the converter. The reason for this rate is that the reference value in the PWM then can be updated every time the triangular wave reaches its maximum and minimum value (See fig. 5.1-2). In this way it is assured that only two switchings per triangular wave period is possible.

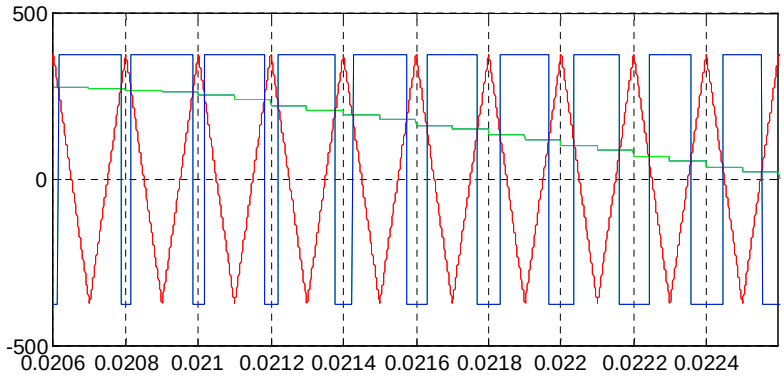


Figure 5.1-2.By sampling at a rate twice the switching frequency, the reference for the PWM can be updated every time the triangle wave reaches its maximum and minimum.

Slow computer

It is assumed that the digital signal processor (DSP) is able to perform the calculations of the new output signals in less than one sample period and update them at the end of the sample period. By this, the DSP always provides a control signal that is based on the measurements made at the beginning of the previous sampling interval. (See fig. 5.1-3) This causes a delay of one sample period.

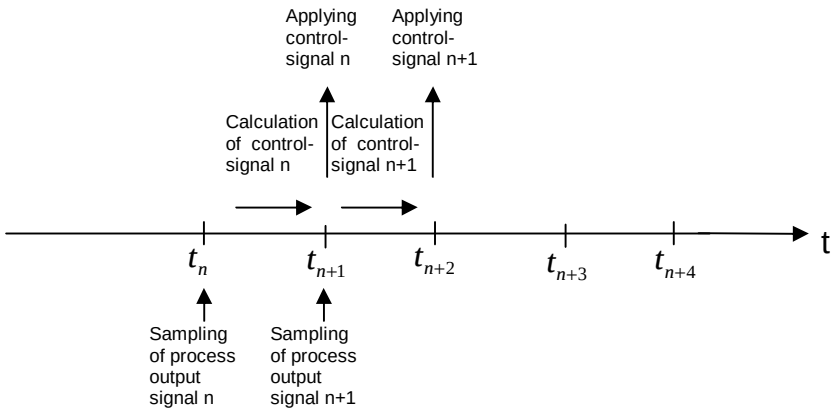


Figure 5.1-3.Control signal updates related to sampling time instants.

Anti-alias

When sampling an analogue signal, there is always the risk of aliasing caused by high frequency disturbances. Frequencies higher than half the sampling frequency (the Nyqvist frequency) may in the sampled signal cause new frequencies that didn't exist in the original analogue signal. To avoid this, the analogue signal is low-pass filtered before it is sampled. The cut-off frequency

of the filter should be half the sampling frequency. This filter also adds some delay to the control loop.

Delays

A drawback of the digital implementation of the controllers is the delay it causes in the control loop. As mentioned above, the calculation and update of the control signal takes 1 sample period. If using a second order Bessel filter as the low pass filter, a delay of 0.4 more sample periods is added as well [12]. The total delay caused by the digital implementation will then be 1.4 sample periods.

Digital PI controller

The continuous PI controller has the equation:

$$u(t) = K\left(e(t) + \frac{1}{T_i}\int^{t} e(s)ds \right) = K \cdot e(t) + \frac{K}{T_i}\int^{t} e(s)ds = P(t) + I(t)$$

Equation 5.1.1

Where *e(t)* is the input signal to the controller, *u(t)* is the control signal, *K* is the proportional gain and T_i is the integral time.

The digital PI controller is similarly given by [12]:

$$u(kh) = P(kh) + I(kh)$$ Equation 5.1.2

Where *k* is the sample, *h* is the sample period and:

$$P(kh) = K \cdot e(kh)$$ Equation 5.1.3

and

$$I(kh+h) = I(kh) + \frac{K \cdot h}{T_i} \cdot e(kh)$$ Equation 5.1.4

The discreet input signal *e(kh)* at sample k, when the sample period is h, is calculated as:

$$e(kh) = ref(kh) - y(kh)$$ Equation 5.1.5

Where ***ref(kh)*** is the value of the reference signal and ***y(kh)*** is the actual measured value at time instant ***kh***.

Computer algorithms

A simple code that calculates the algorithms above for digital PI controller may look like this:

```
y = yIn.get();          //read the systems output signal
e = yref - y;           //calculate the error (eq. 5.1.5)

u = K*e+ I;             //calculate the control signal (eq. 5.1.2)

I = I + (K*h/Ti)*e;     //update the integral term (eq. 5.1.4)

waitUntil(t)            //wait for right moment

uOut.put(u);            //update the control signal
```

To prevent integrator windup, which occur when the actuators gets saturated and the integral term of the controller increases to much, an anti windup function may be implemented as well.

```
if (I>I_max)  {
    I= I_max;
}
if (I< I_min)  {
    I= I_min
}
```

This function limits the maximal value of the integral term and may be implemented between *calculate the control signal* and *update the integral term* in the code above. When calculating I_max and I_min, respect should be taken to the present proportional part of the control signal and the present maximum available control voltage level.

5.2 Proposed main components

In section 2.6.6, the main components of the converter are dimensioned, using the methods covered in section 2.6.1-2.6.5. Table 5.2-1 presents these components.

Component type	Component	Manufacturer	Size (mm)/weight(kg)
IGBT, phases	200GB123D	Semikron	106x61x30/ 0.325
IGBT, neutral	300GB124D	Semikron	106x61x30/ 0.325
Output filter capacitors	B323 35µF, 250V	Epcos	Diameter=35, height=71
* Output filter inductors, phases	3.0mH, 90A (one phase)	TRAMO-ETV AB	200x160x310/ 27
* Output filter inducor, phases	3.0mH, 90A (three phase)	TRAMO-ETV AB	420x180x420/ 70
Output filter inducor, neutral	1.5mH, 140A	TRAMO-ETV AB	240x160x360/ 35

*Table 5.2-1. Suggestions of main components for the converter. * Three one phase inductors, or one three phase inductor may be used.*

With this choice of components, it is obvious that the filter components, especially the inductors, will dominate the total size and weight of the converter. Even without covers and cooling devices, the total mass of the inductors are above 100kg and their total volume about $0.04m^3$.

Except from the components above, there are of cause a need for: DSP, DSP-card, drivers, current sensors, voltage sensors, transient protection devices, anti-alias filters, cooling devices and more. Since the physical design of the converter not is the target of the project, these are not dealt with.

6. Conclusions

The thesis presents the bases for a future design of a DC/AC power electronic converter with four half bridges, providing a three-phase four-wire 230/400V 50Hz AC voltage source. The goal is a high power converter that is able to deliver a balanced load voltage during specified load scenarios. Unbalanced three-phase loads and single-phase loads are highlighted. The theory of the power electronic converter and the control of the converter are the main objectives of the thesis. The design of the main components are covered, but not highlighted. Efforts are not made to reach a specified specification. The focus is on understanding and evaluation of possibilities. A model of the converter and the control systems is built and simulations based on the specified load scenarios are performed on the model.

First, a summary of the work and obtained results is given. Second, some suggestions of future work and research are provided.

6.1 Summary

In this section, the results from the project are summarized.

The control system

The control of the converter is performed in the rotating d-q-0 coordinate system. A cascade control with an inner inductor current control loop and an outer load voltage control loop for each channel (d, q and 0) is proposed. To increase the bandwidth, feed forward control of the load currents and load voltages are used. The cross couplings between channel d and q, due to the filter components, are reduced by decoupling.

This control gives the converter a fast response in all channels. This is important because of the constant 100 Hz disturbance signals in channel d and q, and the 50 Hz disturbance signals in channel 0, during control of unbalanced loads. It also gives a fast load voltage regulation during load changes. A disadvantage of this control method is the large amount of sensors needed.

In this converter, where high power and high quality of the load voltage are required, limitations of the control bandwidth are due the switching frequency and the output filter.

The simulation model

By using the theory and equations provided in the thesis, the model made in Matlab/Simulink simulates the important aspects of the converter. The main aspects are: control systems, coordinate transformations, effects of the DSP, pulse width modulation, power electronic switches, output filters and loads.

The model gives a verification and understanding of the converter theory. It also provides simulated results of what possibilities, limitations and behavior to expect from a physical converter.

Results

The simulated converter is tested with specified load scenarios. The scenarios are chosen to simulate possible loads for a converter working as a multi purpose voltage source.

The converter copes well with the simulated scenarios. Deviations between the load voltages of the phases are small, even under heavily unbalanced load. This is due to a high control bandwidth. A slower control leads unavoidable to a lower quality of the load voltages, especially during unbalanced conditions. By avoiding the most extreme scenarios of unbalance a high quality of the load voltage is achievable.

The need of a high dc link voltage is apparent. Simulation shows the limit of the dc link voltage to maintain a controlled load voltage. Especially heavily inductive loads, and LC-filter, require a high dc link voltage.

During start of the converter, or sudden load changes, oscillations in the filter cause high transient voltage peaks in the load voltages. These oscillations are to fast to be controllable by the converter, but may be limited by devices for over voltage protection (varistors).

Components and physical size

A dimensioning is performed of the main components of the simulated converter. Since the physical size and weight of the converter is of importance much is focused on the physical size and weight of the components. The dominating components in size and weight are the filter inductors. The semiconductors and filter capacitors weight will be reduced to a few kilos.

To reduce the current ripple through the semiconductors and filter inductors to a reasonable level of a few percent, the phase filter inductances are set to 3mH and the neutral inductance to 1.5mH. With a nominal power of 50kVA of the converter this leads to physically large inductor components (≈ 105 kg in total). By reducing the filter inductances by 1/3 and increasing the filter capacitances by 3, (and keep the output voltage ripple unchanged) the total weight of the inductors was reduced to 57 kg. Allowing a larger current ripple may however lead to increased losses in the inductors, which leads to the need of inductors with higher rate and more weight. Due to the worst case scenario of unbalance, the neutral inductor is dimensioned for almost twice the current in a phase inductor. However, by limiting the maximal allowed case of unbalance, the physical size of this inductor may be largely reduced.

6.2 Discussion for the future

The simulation model may be extended with a model of the dc link. Simulations of the dc link voltage, during different load scenarios of the converter, would give a deeper understanding of the converters effects on the total electric system and the design of dc link capacitors.

Simulations of nonlinear load scenarios are not performed on the model. An extension of the load model to simulate nonlinear loads would be interesting since nonlinear loads are common and plausible loads for this converter.

The effects of the delay in the control, due to the calculation time of the DSP, may be reduced by implementing a smith predictor in the control [4].

This solution demands a certain level of dc-link voltage. The definitive limit is $400 \cdot \sqrt{2}$ (the peak value of the line-line voltage), but a more reasonable level is 700-750V. If this voltage is not available other solutions must be considered. One solution may be a step-up converter between the dc-link of the SEP and the ACM. Another solution may be a three half-bridge inverter and $\Delta - \mathrm{Y}$ -connected transformer to achieve the neutral connection.

The main improvement of the understanding of the converter would of cause be obtained by specify, design and build a prototype of the converter. Then the results achieved from the simulations could be verified. This thesis, and the model of the converter, would provide a base for the design process.

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Appendix A – Dimensioning the dc link capacitance

Following text concerns the dimensioning of the dc link capacitor, with and without the use of a split dc link capacitor as the neutral connection to highlight the differences. The method is received from [2].

Without split dc-link capacitance as neutral connection

The ripple power delivered to the load is caused by the negative sequence power due to the unbalanced load and can be expressed as:

$$P_n = [v_{an}, v_{bn}, v_{cn}] \cdot [i_{a\_n}, i_{b\_n}, i_{c\_n}]^T \qquad \text{Equation A.1}$$

Where $[i_{a\_n}, i_{b\_n}, i_{c\_n}]$ are the negative sequence load currents. The negative sequence power can from this be expressed as:

$$P_n = \frac{3}{2} \cdot \hat{v} \cdot \hat{i}_n \cos(2wt + j_n) \qquad \text{Equation A.2}$$

where $\hat{v}$ is the peak AC output voltage and $\hat{i}_n$ is the peak negative sequence load current. The $2w$ frequency is visible here. From eq. A.2, the peak to peak energy ripple required by the load is:

$$\Delta E_{pp} = \frac{3 \cdot \hat{v} \cdot \hat{i}_n}{2 \cdot w} \qquad \text{Equation A.3}$$

The peak to peak energy ripple across the dc link capacitor can also be expressed as:

$$\Delta E_{pp} = \frac{1}{2} C_{dc} (V_{DC} + \Delta V_{DC})^2 - \frac{1}{2} C_{dc} (V_{DC} - \Delta V_{DC})^2 = 2 \cdot C_{dc} \cdot V_{DC} \cdot \Delta V_{DC}$$

Equation A.4

By using eq. A.3 and eq. A.4, following expression for the minimum dc link capacitance $C_{DC-\min\_n}$ for a voltage ripple ΔV_{DC} is given by:

$$C_{dc-\min\_n} = \frac{3 \cdot \hat{v} \cdot \hat{i}_n}{4 \cdot w \cdot V_{DC} \cdot \Delta V_{DC}} \qquad \text{Equation A.5}$$

By this, eq. A.5 expresses the minimum size of the dc link capacitance, with respect to only negative sequence ripple.

$C_{DC-\min\_n}$ can also be expressed as [13]:

$$C_{dc-\min\_n} = \frac{I_q \cdot V_q}{2 \cdot w \cdot V_{DC} \cdot \Delta V_{DC}} = \frac{\sqrt{3} \cdot I_f \cdot V_q}{2 \cdot w \cdot V_{DC} \cdot \Delta V_{DC}} \qquad \text{Equation A.6}$$

where V_q is the value of the rms scaled output voltage vector, I_q is the value of the rms scaled negative sequence line current vector and I_f is the rms scaled negative sequence phase current vector.

With a split dc-link capacitance as neutral connection

If a split dc link capacitance is used, the capacitors, that are then connected in series, are each expressed as $2 \cdot C_{dc}$. Since the neutral current, expressed in eq. A.6, flows through the middle point of the two dc link capacitors, equivalently these two dc link capacitors appear to be in parallel ($4 \cdot C_{dc}$) from the neutral current point of view.

$$i_{neutral} = \hat{i}_{neutral} \cos(wt + r_0) = 3 \cdot \hat{i}_0 \cos(wt + r_0) \qquad \text{Equation A.7}$$

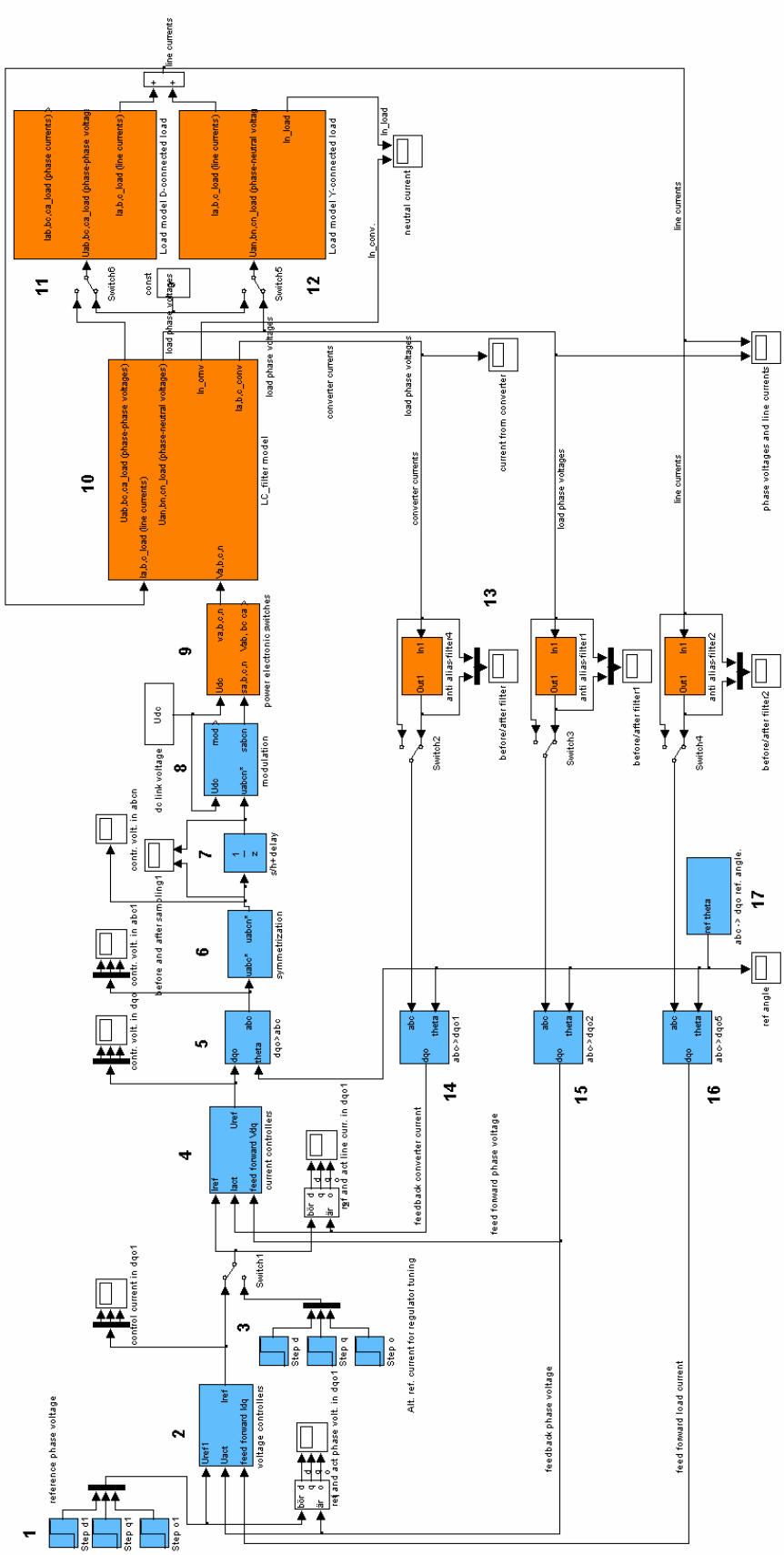
where $\hat{i}_{neutral}$ is the peak of the neutral current and $\hat{i}_0$ is the peak of the zero sequence current. Therefore the peak voltage ripple across each of the dc link capacitors, caused by the neutral current, is expressed as:

$$\Delta V_{C_{dc}} = \frac{3 \cdot \hat{i}_0}{2 \cdot 2 \cdot w \cdot C_{dc}} = \frac{1}{2} \cdot \Delta V_{DC} \qquad \text{Equation A.8}$$

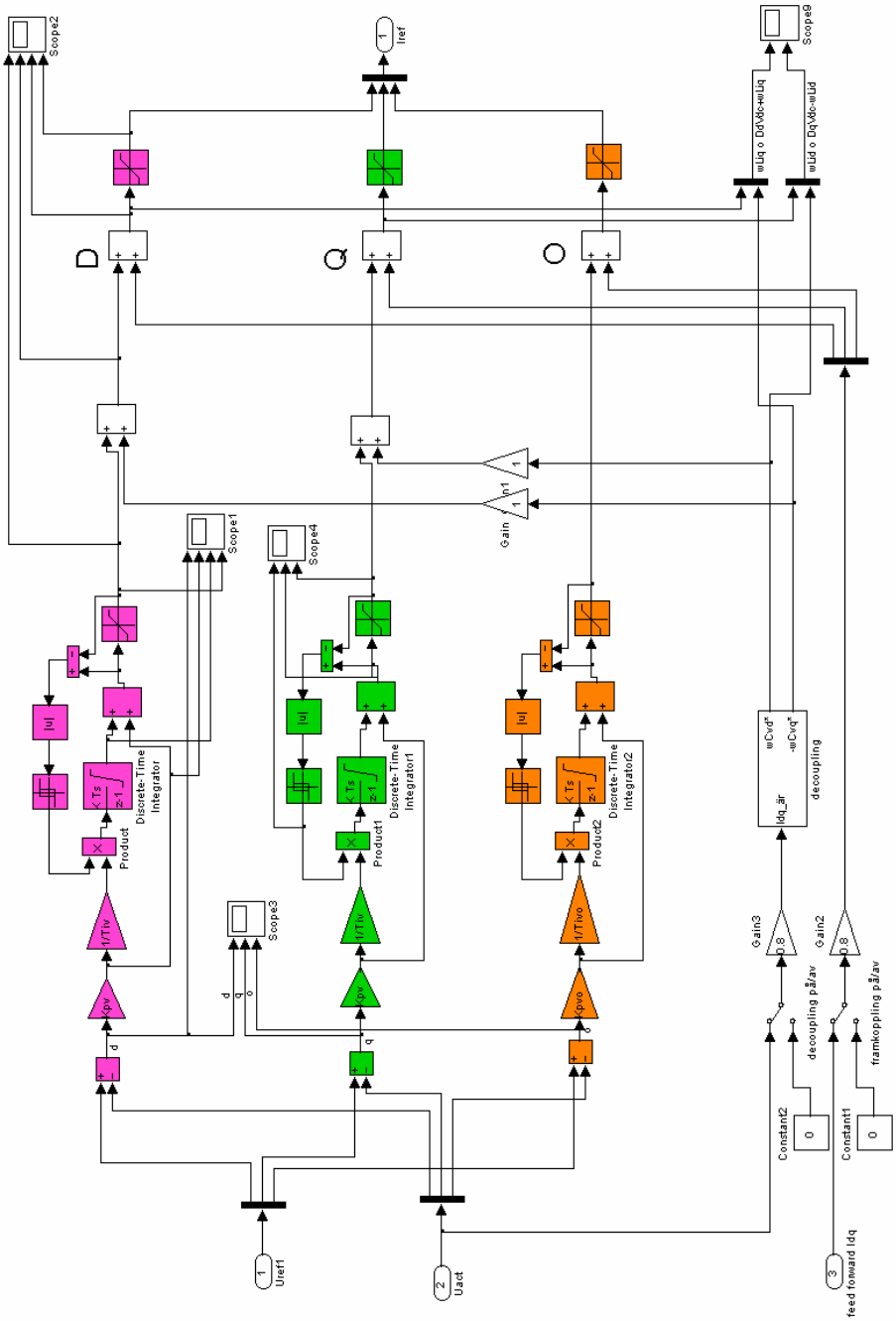
From eq. A.7, finally the minimum dc link capacitance with respect to the zero sequence load current is expressed as:

$$C_{dc\_\min\_0} = \frac{3 \cdot \hat{i}_0}{2 \cdot w \cdot \Delta V_{DC}}$$ Equation A.9

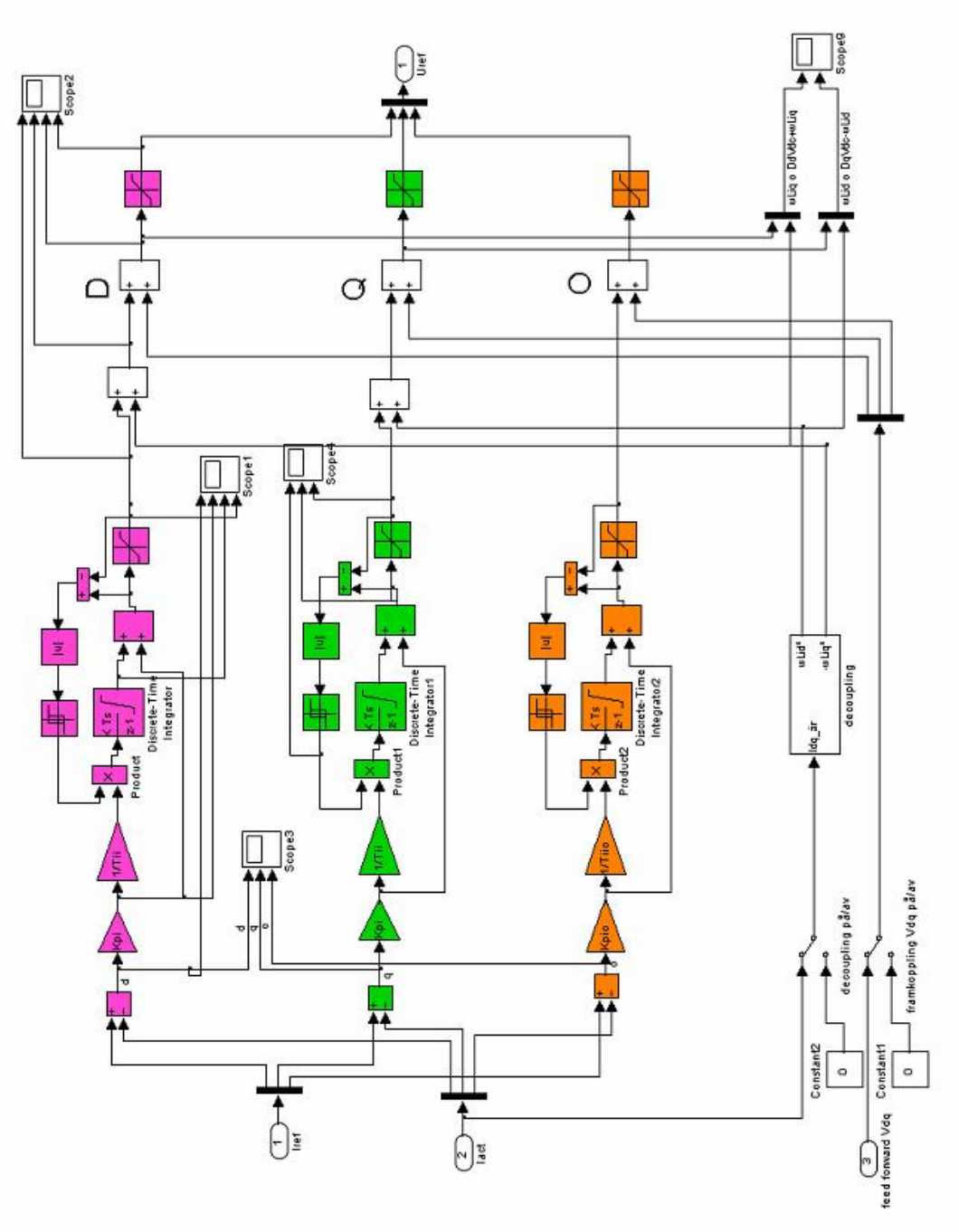
Appendix B –The Simulink model



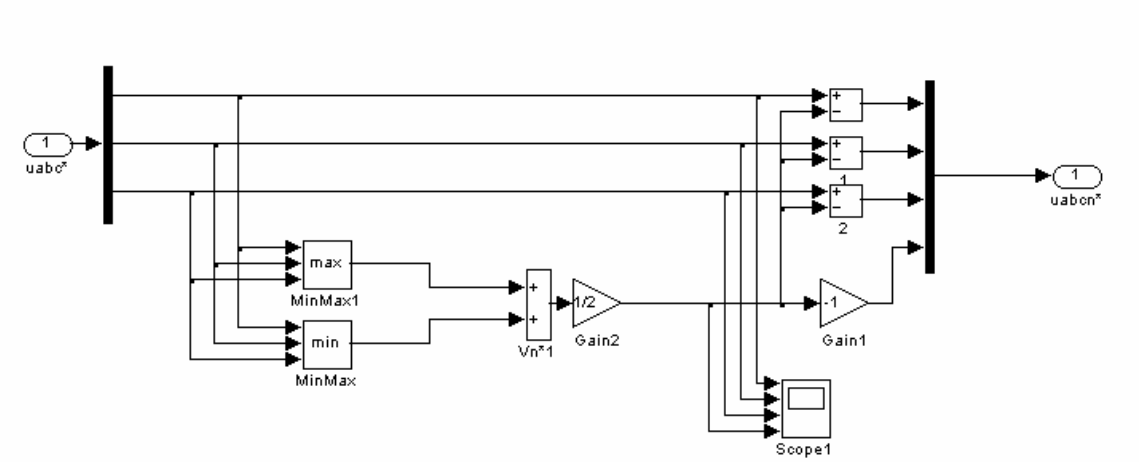
Block 2. Voltage controller



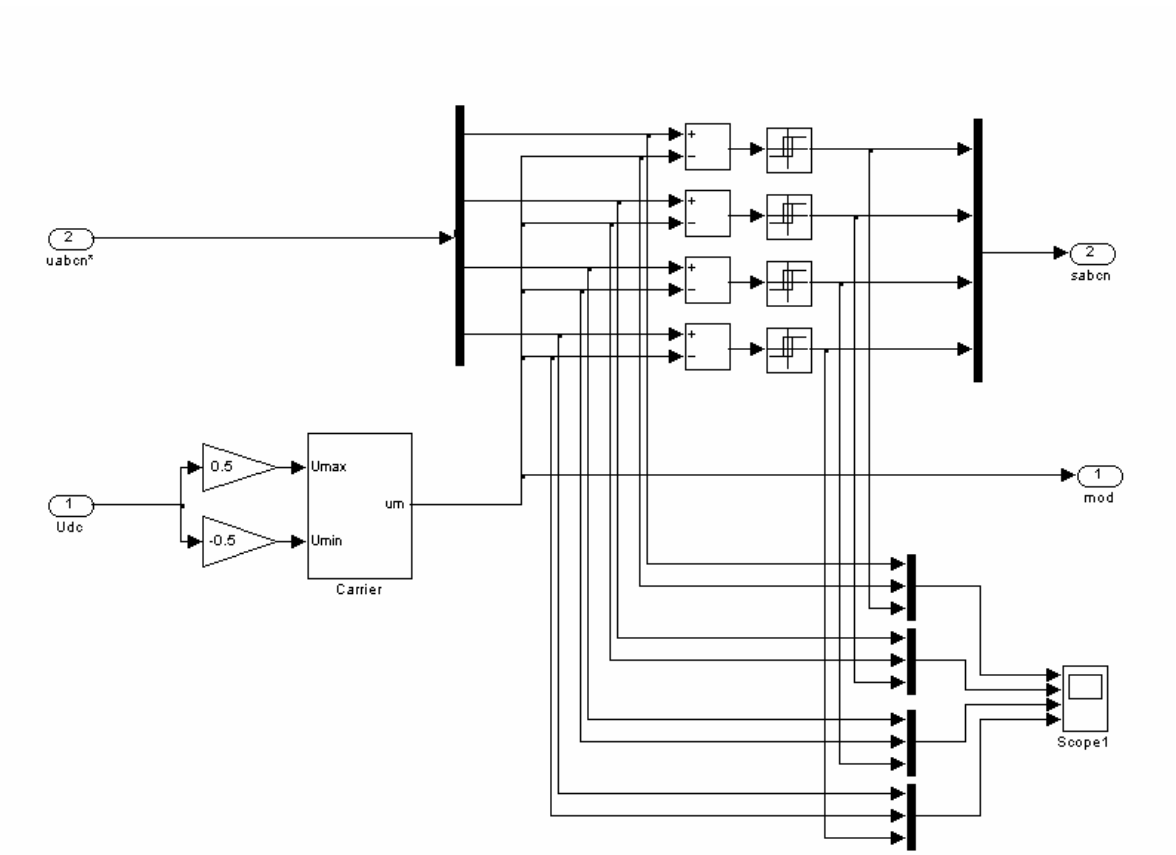
Block 4. Current controller



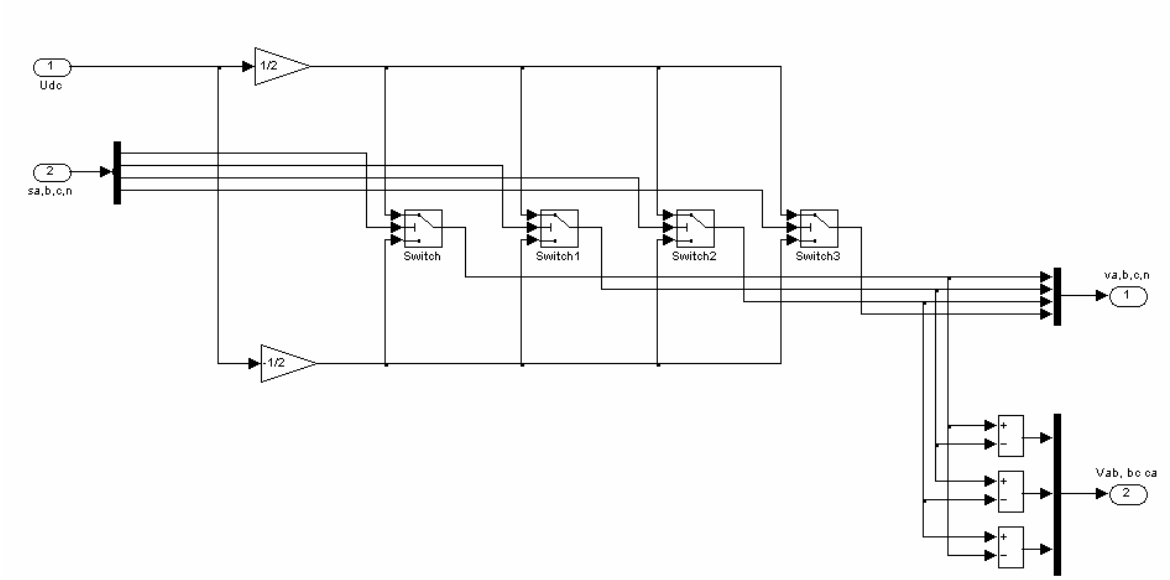
Block 6. Symmetrization



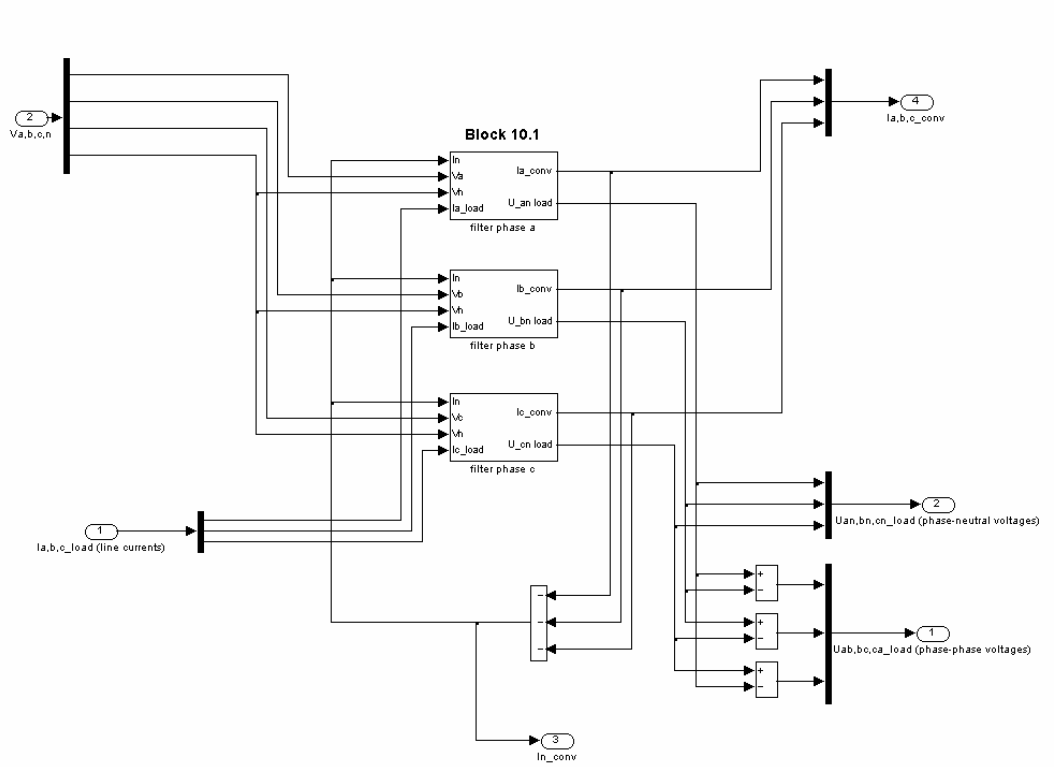
Block 8. Modulation



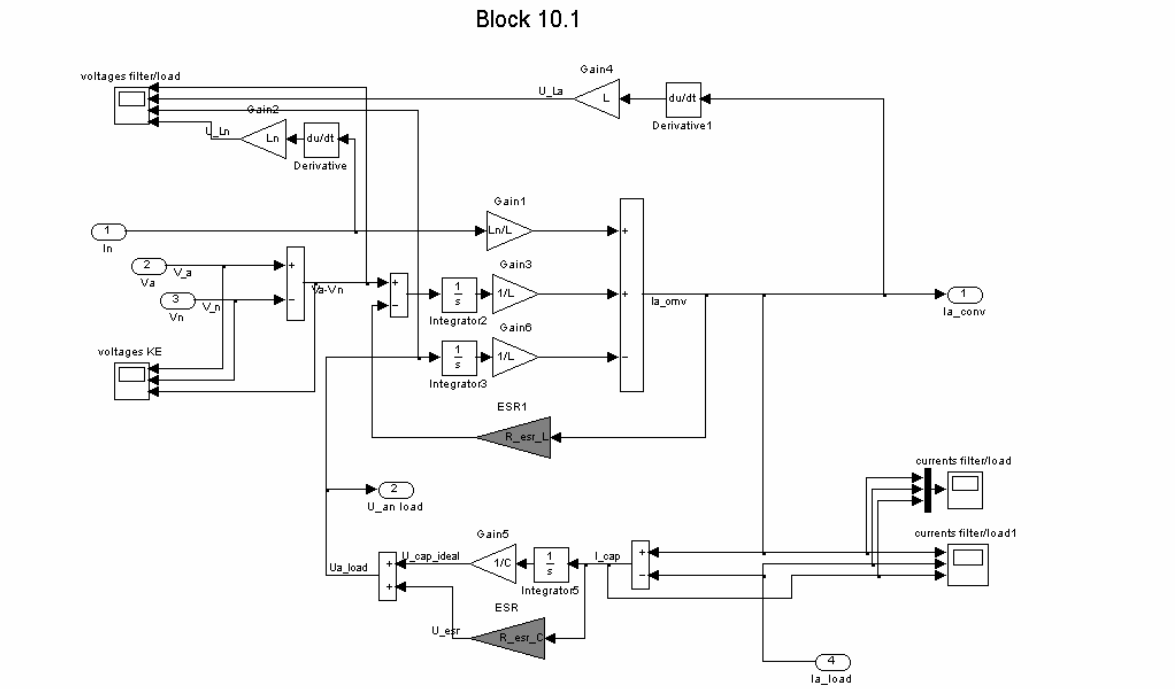
Block 9. Power electronic switches



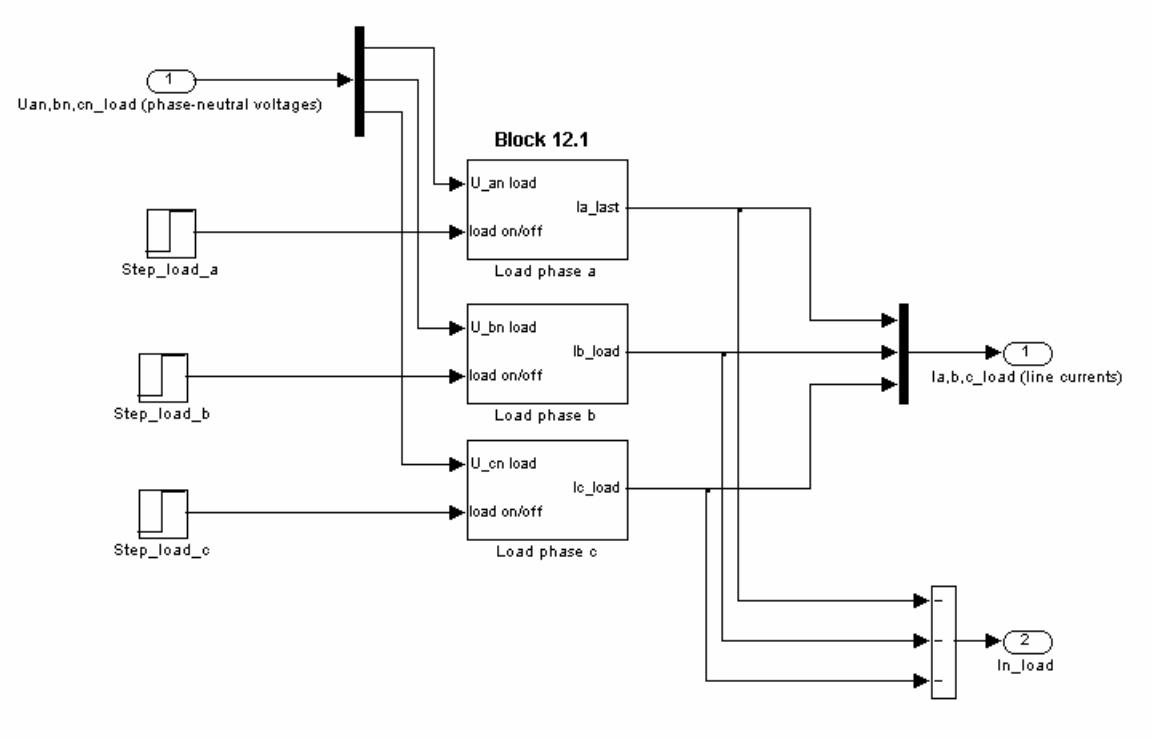
Block 10. LC-filter model



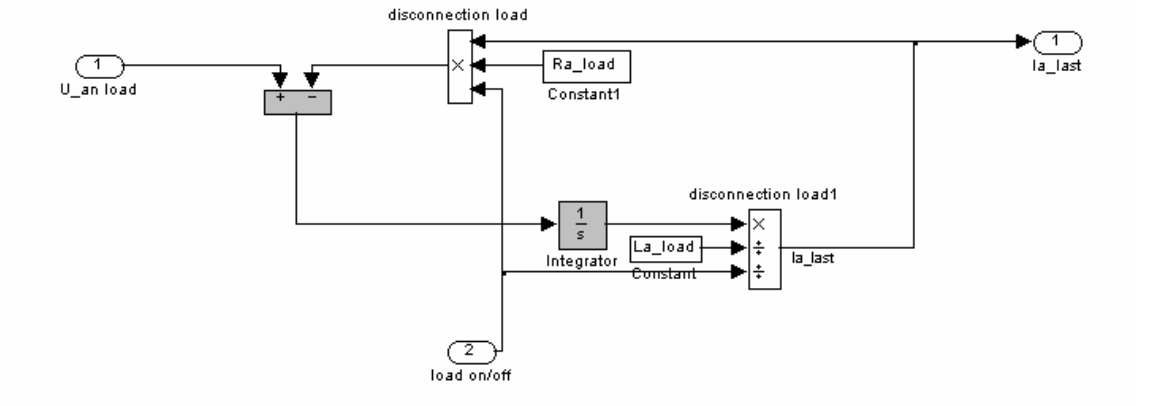
Block 10.1. LC-filter model phase a



Block 12. Load model Y-connected load



Block 12.1. Load model Y-connected load phase a



Appendix C – init.m

```
%-------------------------------------------------------------------
%Misc data:

Udc=750;                        %dc link voltage

Uref=230*sqrt(2);               %reference voltage

Fsw=5e3;                        %switching frequency
Tsw=1/Fsw;                      %switching interval
Ts=Tsw/2;                       %sampling interval

%-------------------------------------------------------------------
%Filter:

L=0.003;                        %filter inductor phase
R_esr_L=0.1;

Ln=L/2;                         %filter inductor neutral
R_esr_Ln=0.1;

C=33.8e-6;                      %filter capacitor phase
R_esr_C=0.1;

%-------------------------------------------------------------------
%Current controller:

Umax=Udc/2;                      %Limited control signal
Umin=-Udc/2;                     %Limited control signal

Kpi=12;                         %P-part controller (d och q)
Tii=0.022;                      %I-part controller (d och q)

Kpio=40;                        %P-part controller(o)
Tiio=0.089;                     %I-part controller(o)

%-------------------------------------------------------------------
%Voltage controller:

Imax=200;                       %Limited control signal
Imin=-200;                      %Limited control signal

Kpv=0.075;                      %P-part controller (d och q)
Tiv=0.00047;                    %I-part controller (d och q)

Kpvo=0.11;                      %P-part controller (o)
Tivo=0.00047;                    %I-part controller (o)
```

Appendix D – losscalc.m

%m-file calculating total losses in semoconductors of ACM (code includes phase a only):

%data used in calculations of losses phase half bridges:

```
Eon_n=24e-3;                    %turn on energy for IGBT(phase) at Vdc=600V and I=150
Eoff_n=17e-3;                   %turn off energy for IGBT(phase) (IGBT with diode
included) at Vdc=600V and I=150
Vdcn=600;                        %Vdc nominal
Inom=150;                       %I nominal
Vdc=750;


V_IGBT0=1.8;                    %treshold voltage drop of IGBT(phase)
R_IGBTon=12.66e-3;              %on state resistance of IGBT(phase)

V_diode0=1.2;                    %treshold voltage drop of diode(phase)
R_diodeon=7e-3;                 %on state resistance of diode(phase)
```

%data from simulink model:

```
%tid=time of simulink sample
%Va, Vb, Vc, Vn=output voltage switches
%Ia_conv,Ib_conv,Ic_conv,In_conv = current through switches
%Tsw=switch period time


pos=1;
k=1;
I_turnon=0;
I_turnoff=0;
t_turnon=0;
t_turnoff=0;


%ooooooooooooooooooooooooooooooooooooooooooooooooooooooooooooooooooooooooooooooooo
%Phase a


for n=1:length(Va)

%------------------------------------------------------------------------
%positive current (Ia>0)

      if Va(n)>0.9*Vdc/2 && pos==0 && Ia_conv(n)>0   %switch has switched from -Vdc/2 to
Vdc/2, current positive

         E_turnon=Eon_n*(Vdc*I_turnon)/(Vdcn*Inom);    %turn on energy loss, IGBT1+diode2
         E_turnoff=Eoff_n*(Vdc*I_turnoff)/(Vdcn*Inom);  %turn off energy loss, IGBT1+diode2

         I_avr=(I_turnon+I_turnoff)/2;                  %avrage current during on state, IGBT1
         V_IGBTon=V_IGBT0+R_IGBTon*I_avr;               %forward voltage drop of IGBT1
         E_cond_IGBT=I_avr*V_IGBTon*(t_turnoff-t_turnon);   %conduction energy loss,
IGBT1

         I_avr=(I_turnoff+Ia_conv(n))/2;                %avrage current during on state, diode2
         V_diodeon=V_diode0+R_diodeon*I_avr;       %forward voltage drop of diode2
         E_cond_diode=I_avr*V_diodeon*(tid(n)-t_turnoff);  %conduction energy loss, diode2
```

```
        P_loss_a(k)=(E_turnon+E_turnoff+E_cond_IGBT+E_cond_diode)/Tsw; % avrage
dissapated power during one switch period. Losses from


        t_turnon=tid(n);            %time at turn on for IGBT1 (turn off for diode2)
        I_turnon=Ia_conv(n);        %current at turn on for IGBT1 (turn off for diode2)

        t_loss_a(k)=tid(n);

        pos=1;                      %switch value high
        k=k+1;

    end

    if Va(n)<0.9*-Vdc/2 && pos==1 && Ia_conv(n)>0   %switch has switched from Vdc/2 to -
Vdc/2, current positive

        t_turnoff=tid(n);           %time at turn off for IGBT1 (turn on for diode2)
        I_turnoff=Ia_conv(n);       %current at turn off for IGBT1 (turn on for diode2)

        pos=0;

    end

%-------------------------------------------------------------------------
%negative current (Ia_conv<0)


    if Va(n)>0.9*Vdc/2 && pos==0 && Ia_conv(n)<0   %switch has switched from -Vdc/2 to
Vdc/2, current positive

        E_turnon=Eon_n*(Vdc*I_turnon)/(Vdcn*Inom);    %turn on energy loss, IGBT2+diode1
        E_turnoff=Eoff_n*(Vdc*I_turnoff)/(Vdcn*Inom);  %turn off energy loss, IGBT2+diode1

        I_avr=(I_turnon+I_turnoff)/2;                 %avrage current during on state, diode
        V_diodeon=V_diode0+R_diodeon*I_avr;           %forward voltage drop of diode1
        E_cond_diode1=I_avr*V_diodeon*(t_turnoff-t_turnon);  %conduction energy loss,
diode1

        I_avr=(I_turnoff-Ia_conv(n))/2;               %avrage current during on state, IGBT2
        V_IGBTon=V_IGBT0+R_IGBTon*I_avr;              %forward voltage drop of IGBT2
        E_cond_IGBT2=I_avr*V_IGBTon*(tid(n)-t_turnoff);  %conduction energy loss, IGBT2

        P_loss_a(k)=(E_turnon+E_turnoff+E_cond_IGBT2+E_cond_diode1)/Tsw; % avrage
dissapated power during one switch period. Losses from


        t_turnon=tid(n);            %time at turn off for IGBT2 (turn on for diode1)
        I_turnon=-Ia_conv(n);       %current at turn off for IGBT2 (turn on for diode1)

        t_loss_a(k)=tid(n);

        pos=1;    %switch value high
        k=k+1;


    end

    if Va(n)<0.9*-Vdc/2 && pos==1 && Ia_conv(n)<0   %switch has switched from Vdc/2 to -
Vdc/2, current positive

        t_turnoff=tid(n);           %time at turn off for IGBT2 (turn on for diode1)
        I_turnoff=-Ia_conv(n);      %current at turn off for IGBT2 (turn on for diode1)

        pos=0;
```

```
        end


end

%ooooooooooooooooooooooooooooooooooooooooooooooooooooooooooooooooooooooooooooooooooooooooooooooo

%Average losses phase a:
%---1:st:

P_loss_a_tot=0;
i=0;


for n=1:length(t_loss_a)

    if  t_loss_a(n)>0.04 && t_loss_a(n)<0.06

        P_loss_a_tot=P_loss_a_tot + P_loss_a(n);



        i=i+1;

    end
end
P_loss_a_average=P_loss_a_tot/i;

%---2:nd:

P_loss_a_tot=0;
i=0;


for n=1:length(t_loss_a)

    if  t_loss_a(n)>0.10 && t_loss_a(n)<0.12

        P_loss_a_tot=P_loss_a_tot + P_loss_a(n);



        i=i+1;

    end
end
P_loss_a_average2=P_loss_a_tot/i;

%ooooooooooooooooooooooooooooooooooooooooooooooooooooooooooooooooooooooooooooooooooooooooooooooo


subplot(5,1,1),plot(t_loss_a, P_loss_a)
hold on
subplot(5,1,1),plot(t_loss_a(200:300), P_loss_a_average,'red')
AXIS([0 0.12 0 1200])
subplot(5,1,1),plot(t_loss_a(500:590), P_loss_a_average2,'red')
YLABEL('a')
Grid minor
```

Appendix E - Detailed representation control signals

In chapter four, the results from the simulation of the load scenarios were presented. To provide a simpler presentation, focus was put on the output voltages and load currents in phase representation.

For deeper studies of the signals in the control system, following plots are provided. The results are from the same scenarios as in chapter four. However, to give a more detailed presentation, interesting moments of the simulations are highlighted and the time scales of these moments are narrowed. All control signals are represented in d-q-0. The signals in the following plots are shown in fig. E-1.

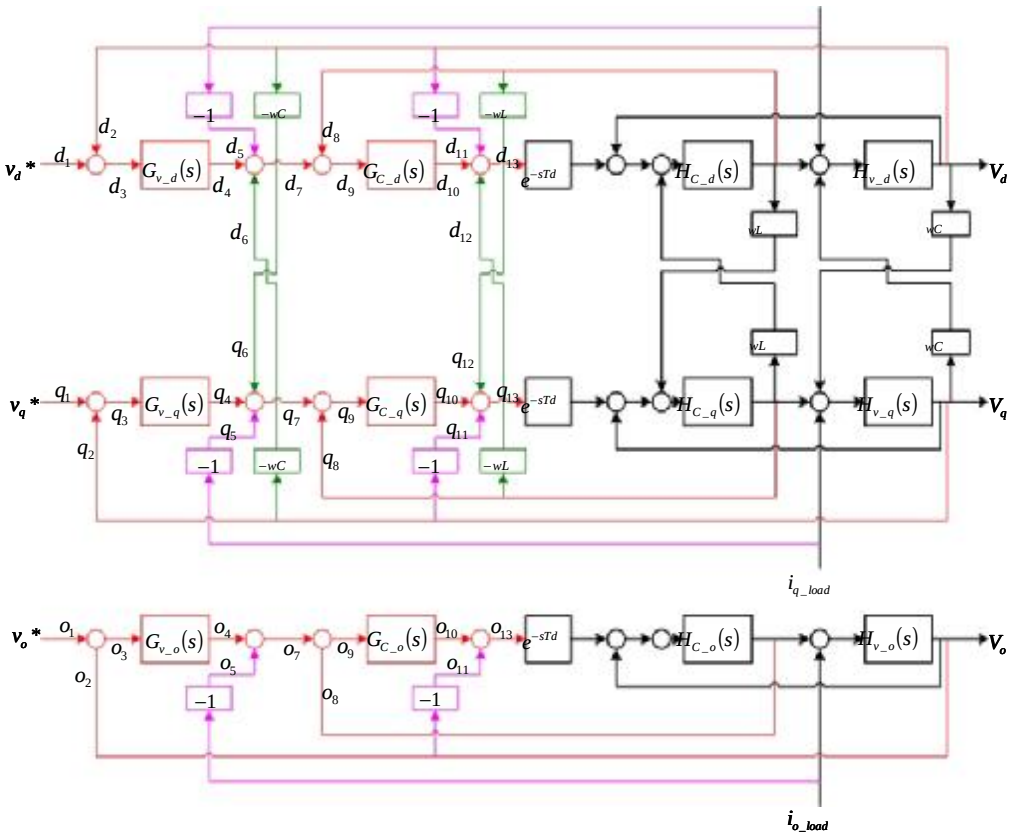


Figure E-1.Layout of the control system and signal paths.

Scenario 1:

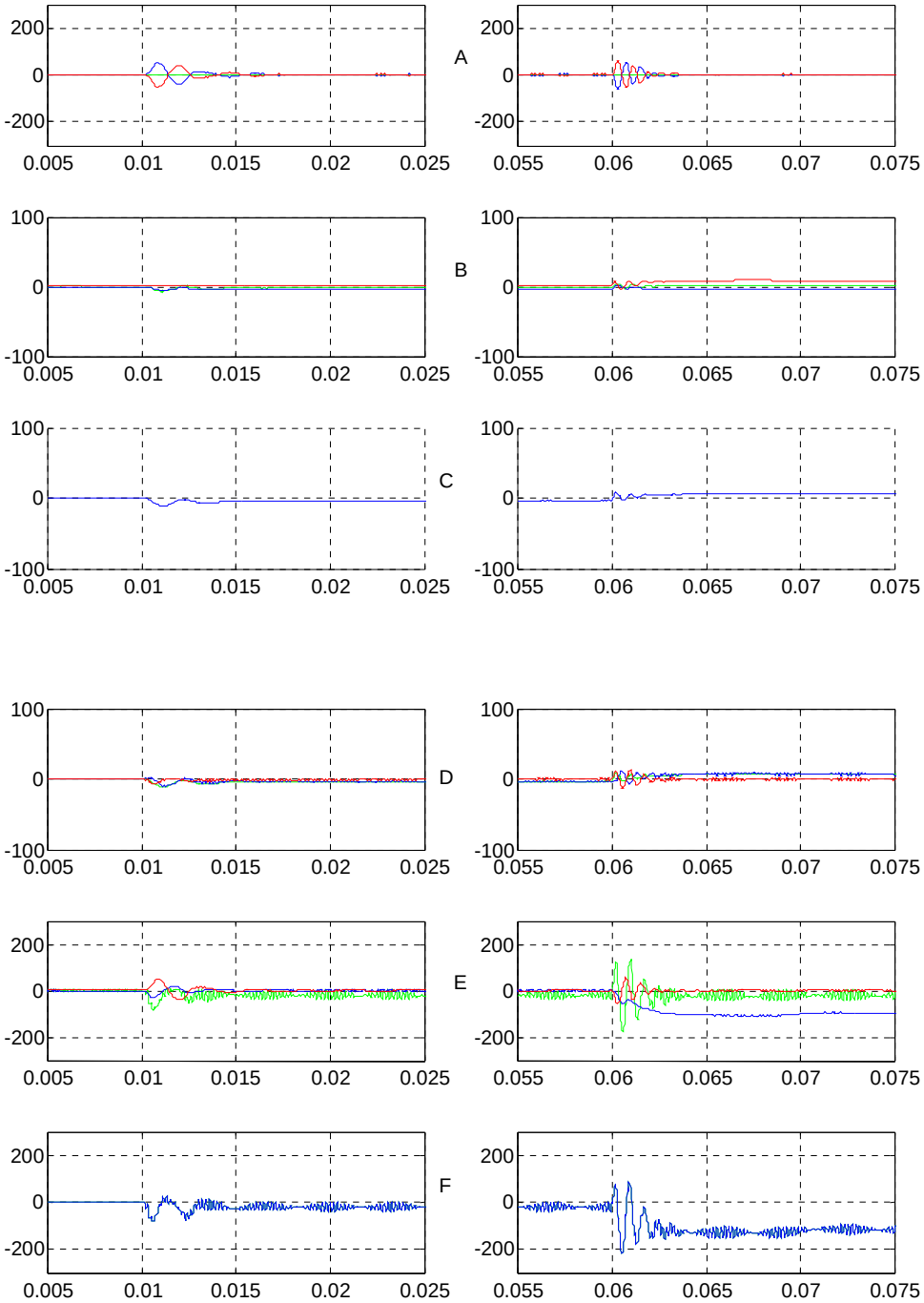


Figure E-2. Signals scenario 1, channel d.

A: Reference output voltage d1 (green), output voltage d2 (blue), error signal d3 (red).
B: control signal PI controller d4 (green), load current feed forward signal d5 (red), decoupling signal d6 (blue).
C: Reference current d7 (blue).
D: Reference current d7 (green), converter current d8 (blue), error signal d9 (red).
E: Control signal PI controller d10 (green), output voltage feed forward signal d11 (red), decoupling signal d12 (blue).
F: Reference voltage converter d13 (blue).

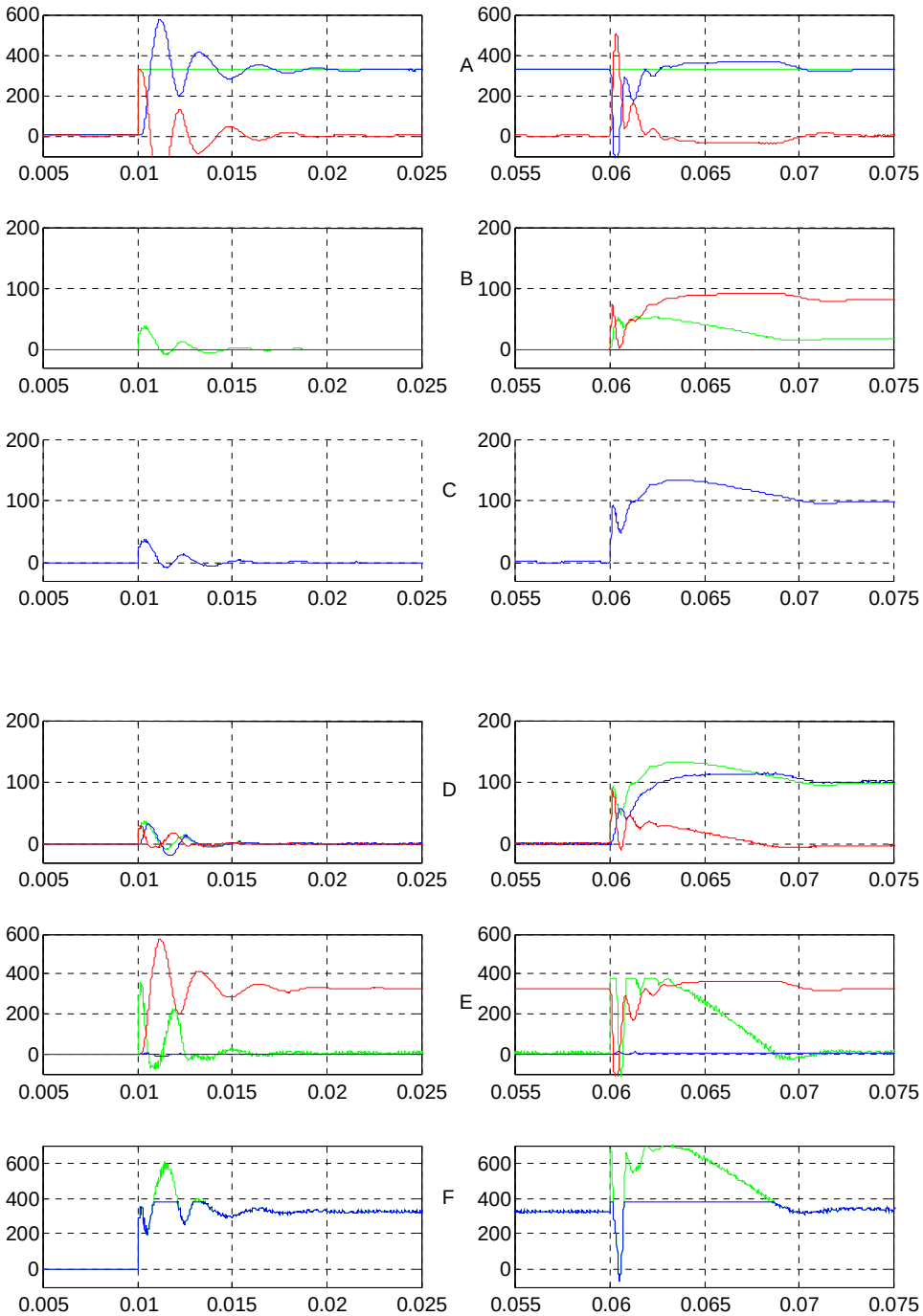


Figure E-3. Signals scenario 1, channel q.

A: Reference output voltage q1 (green), output voltage q2 (blue), error signal q3 (red).
B: control signal PI controller q4 (green), load current feed forward signal q5 (red), decoupling signal q6 (blue).
C: Reference current q7 (blue).
D: Reference current q7 (green), converter current q8 (blue), error signal q9 (red).
E: Control signal PI controller q10 (green), output voltage feed forward signal q11 (red), decoupling signal q12 (blue).
F: Reference voltage converter q13 (blue).

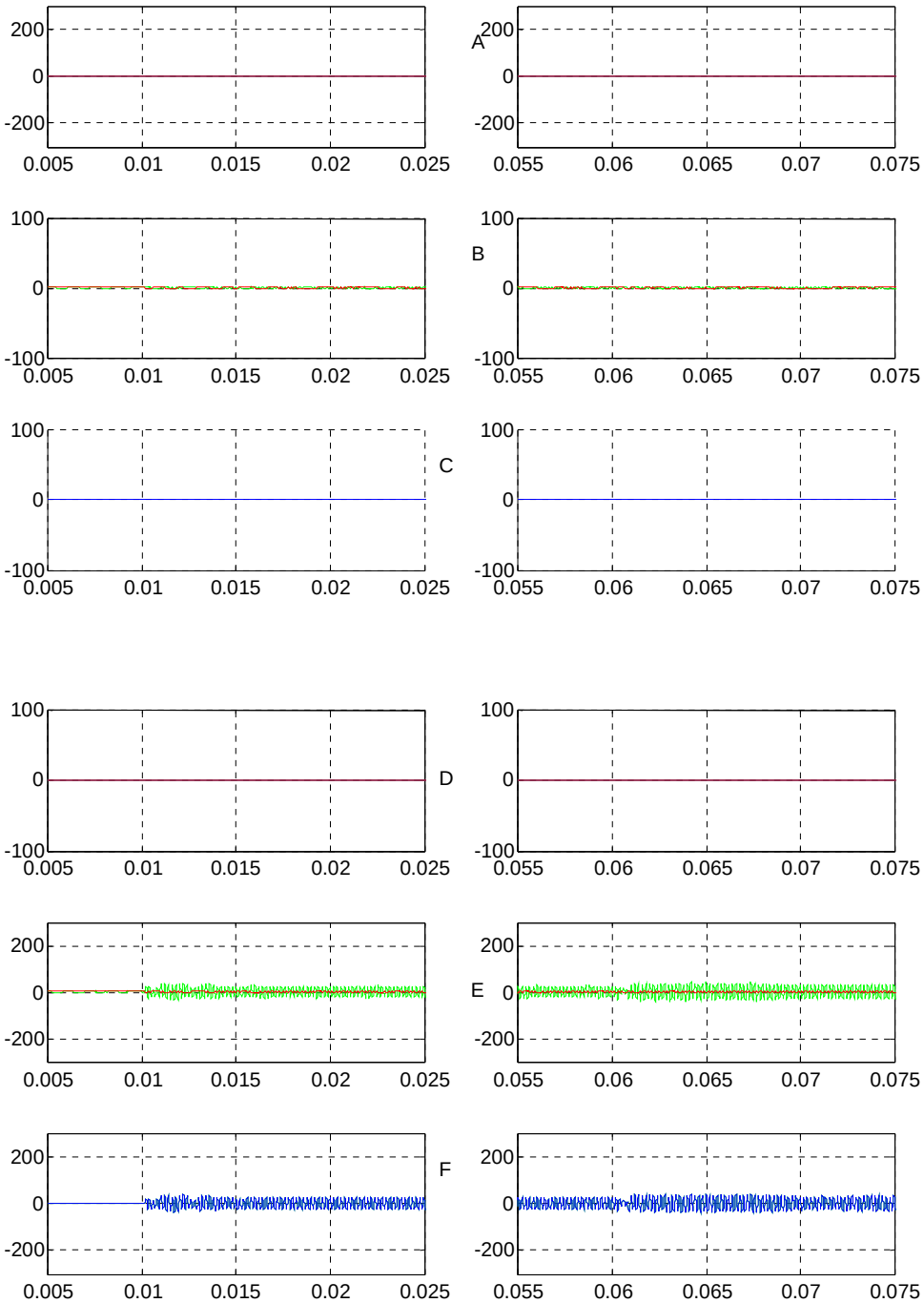


Figure E-4. Signals scenario 1, channel 0.

A: Reference output voltage 0-1 (green), output voltage 0-2 (blue), error signal 0-3 (red).
B: control signal PI controller 0-4 (green), load current feed forward signal 0-5 (red).
C: Reference current 0-7 (blue).
D: Reference current 0-7 (green), converter current 0-8 (blue), error signal 0-9 (red).
E: Control signal PI controller 0-10 (green), output voltage feed forward signal 0-11 (red).
F: Reference voltage converter 0-13 (blue).

Scenario 2:

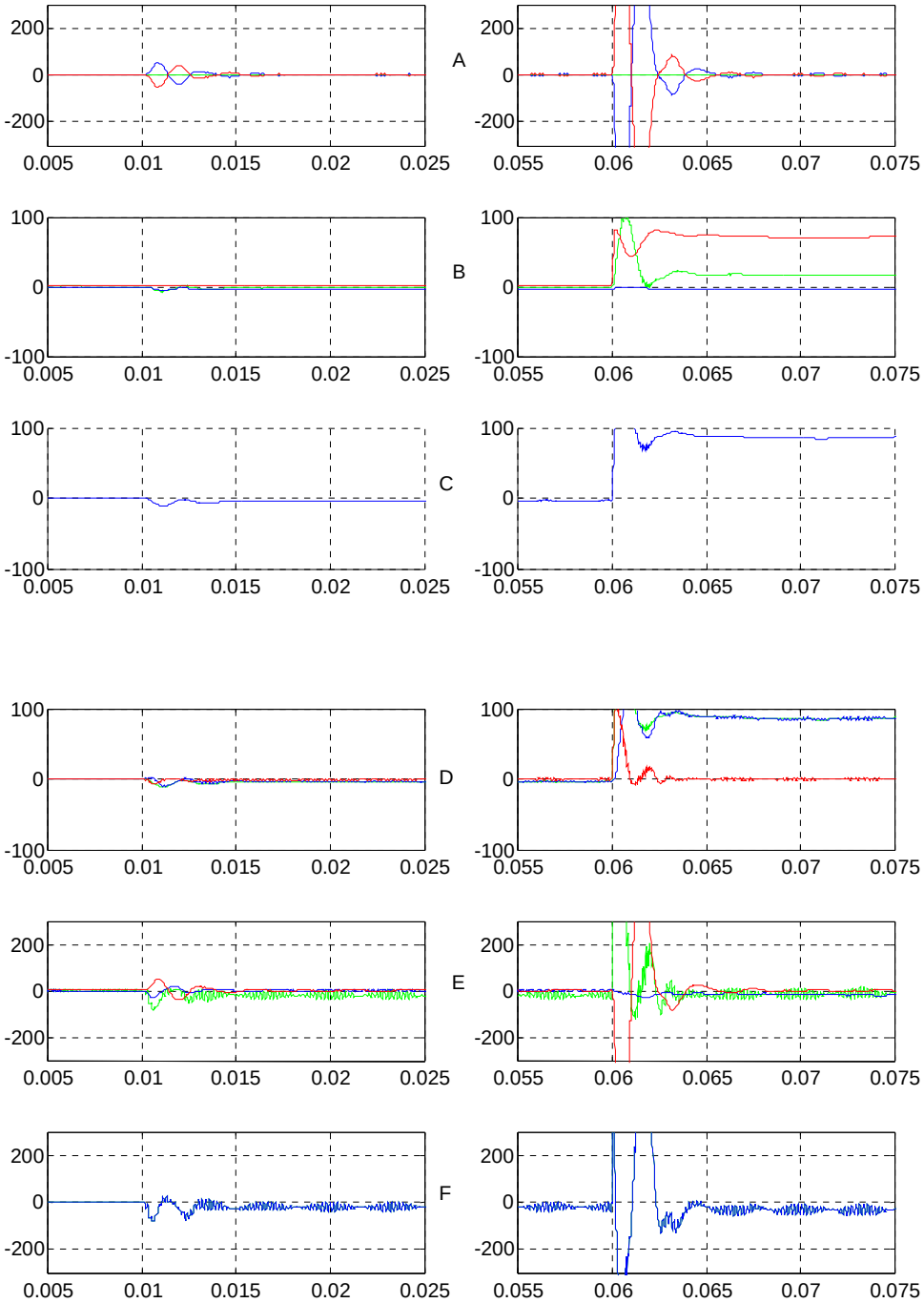


Figure E-5. Signals scenario 2, channel d.

A: Reference output voltage d1 (green), output voltage d2 (blue), error signal d3 (red).
B: control signal PI controller d4 (green), load current feed forward signal d5 (red), decoupling signal d6 (blue).
C: Reference current d7 (blue).
D: Reference current d7 (green), converter current d8 (blue), error signal d9 (red).
E: Control signal PI controller d10 (green), output voltage feed forward signal d11 (red), decoupling signal d12 (blue).
F: Reference voltage converter d13 (blue).

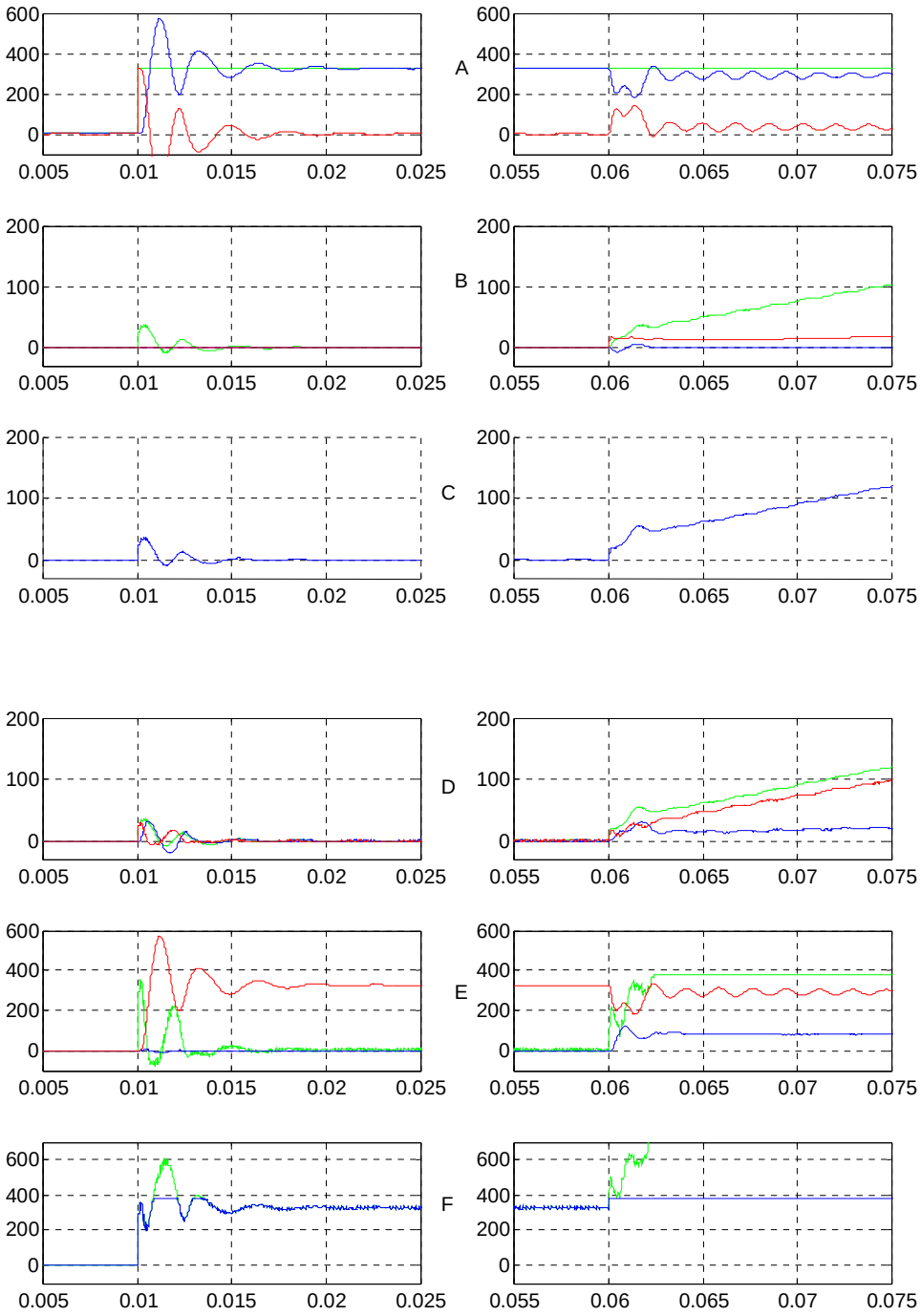


Figure E-6. Signals scenario 2, channel q.

A: Reference output voltage q1 (green), output voltage q2 (blue), error signal q3 (red).
B: control signal PI controller q4 (green), load current feed forward signal q5 (red), decoupling signal q6 (blue).
C: Reference current q7 (blue).
D: Reference current q7 (green), converter current q8 (blue), error signal q9 (red).
E: Control signal PI controller q10 (green), output voltage feed forward signal q11 (red), decoupling signal q12 (blue).
F: Reference voltage converter q13 (blue).

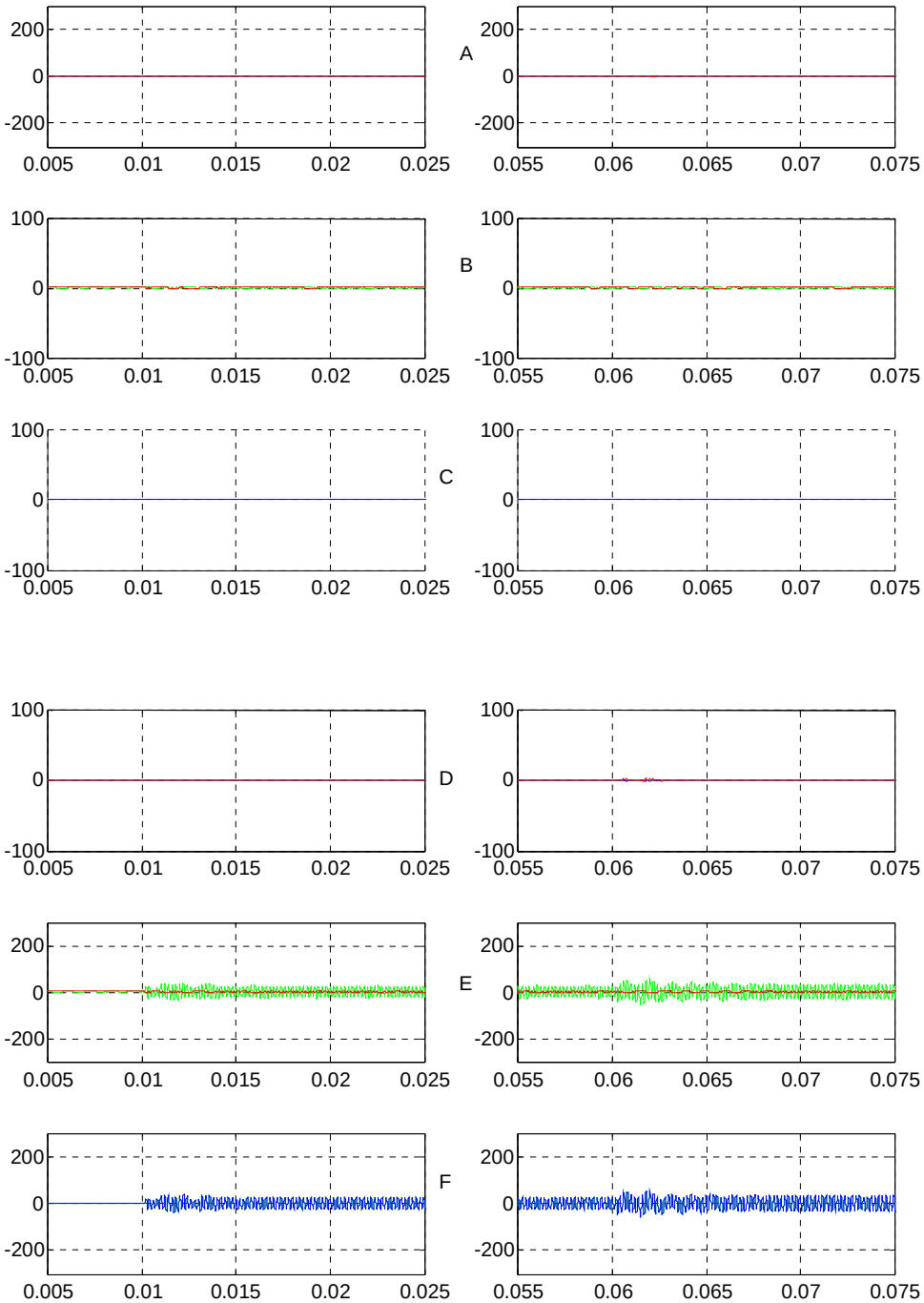


Figure E-7. Signals scenario 2, channel 0.

A: Reference output voltage 0-1 (green), output voltage 0-2 (blue), error signal 0-3 (red).
B: control signal PI controller 0-4 (green), load current feed forward signal 0-5 (red).
C: Reference current 0-7 (blue).
D: Reference current 0-7 (green), converter current 0-8 (blue), error signal 0-9 (red).
E: Control signal PI controller 0-10 (green), output voltage feed forward signal 0-11 (red).
F: Reference voltage converter 0-13 (blue).

Scenario 3:

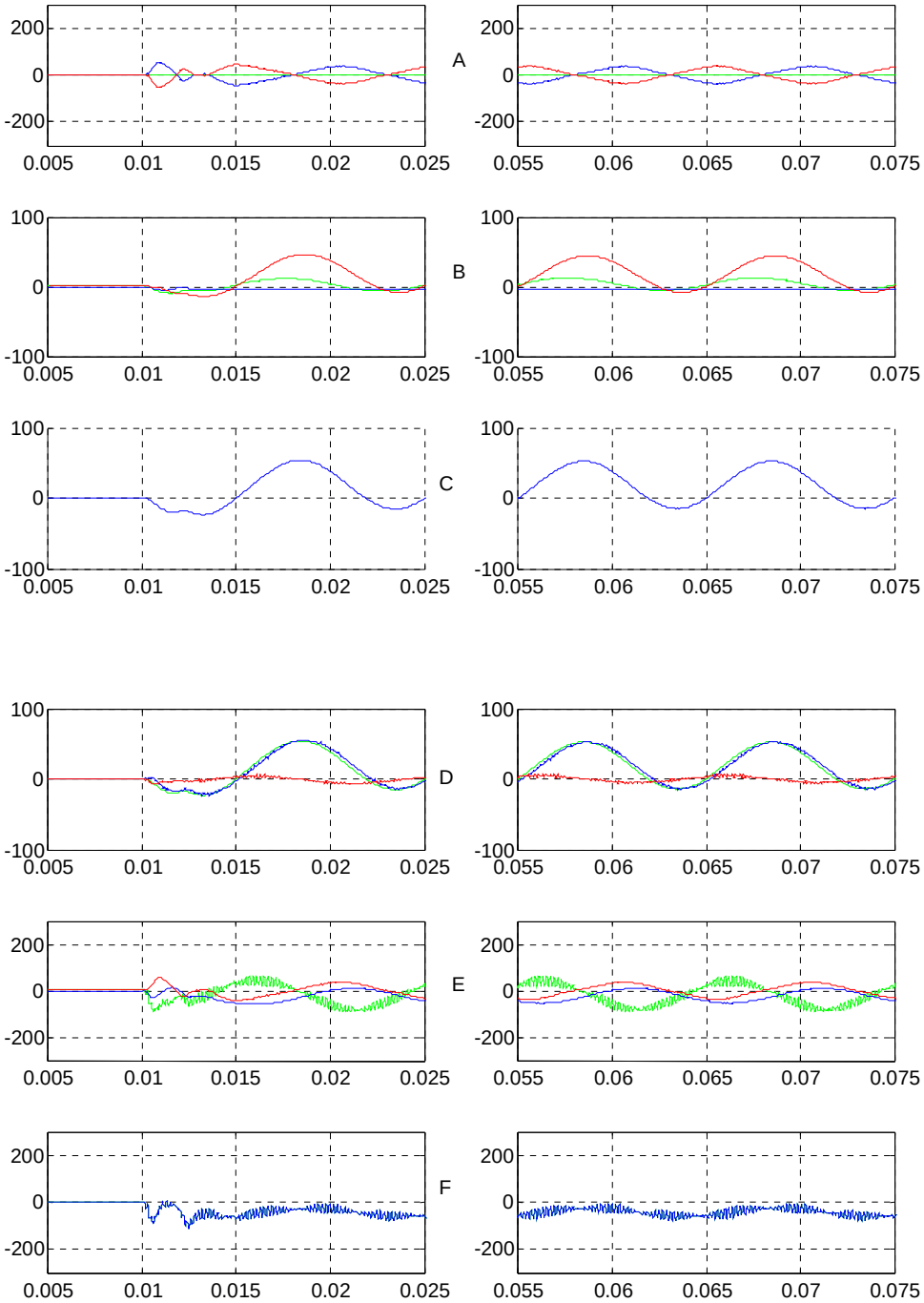


Figure E-8. Signals scenario 3, channel d.

A: Reference output voltage d1 (green), output voltage d2 (blue), error signal d3 (red).
B: control signal PI controller d4 (green), load current feed forward signal d5 (red), decoupling signal d6 (blue).
C: Reference current d7 (blue).
D: Reference current d7 (green), converter current d8 (blue), error signal d9 (red).
E: Control signal PI controller d10 (green), output voltage feed forward signal d11 (red), decoupling signal d12 (blue).
F: Reference voltage converter d13 (blue).

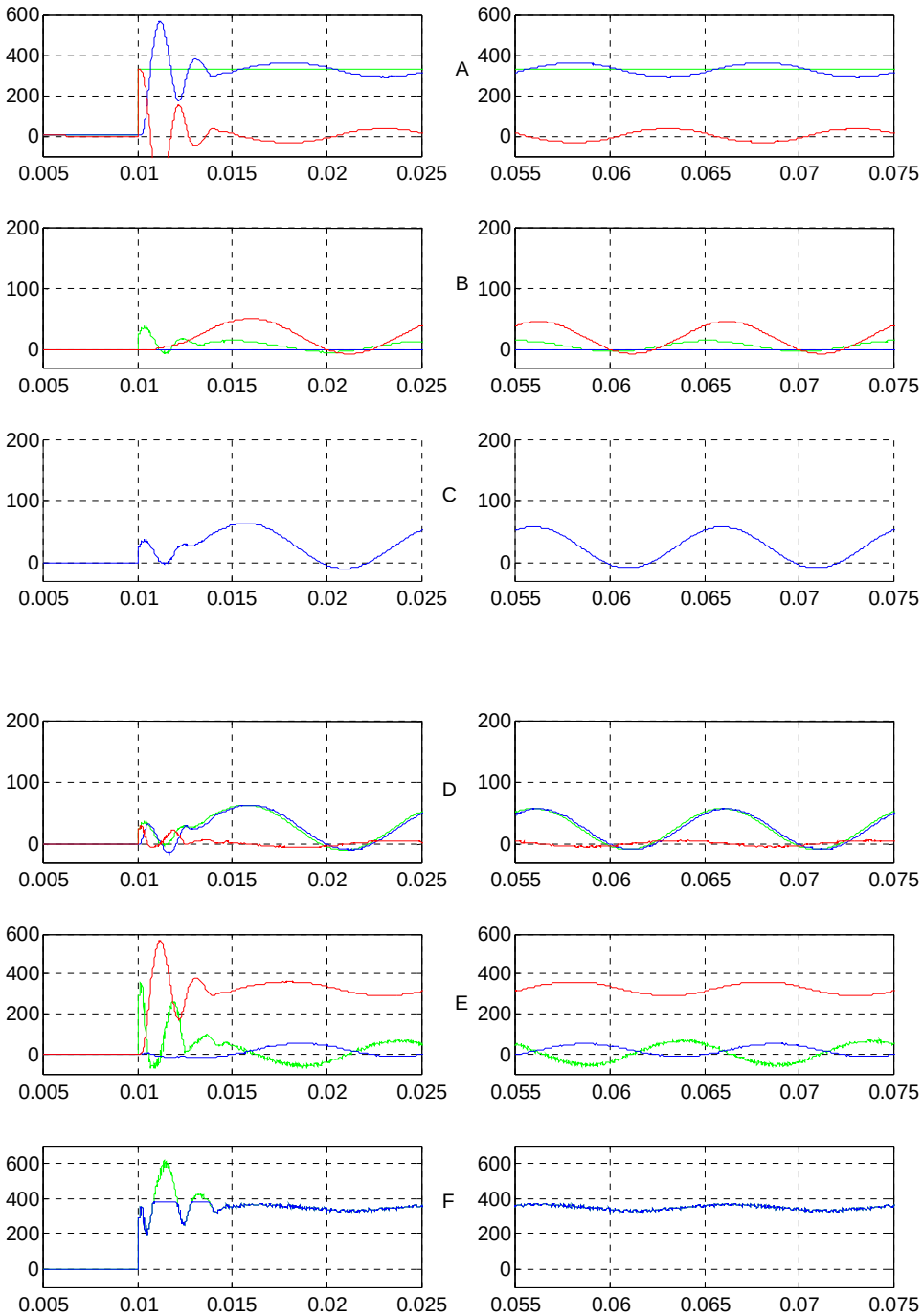


Figure E-9. Signals scenario 3, channel q.

A: Reference output voltage q1 (green), output voltage q2 (blue), error signal q3 (red).
B: control signal PI controller q4 (green), load current feed forward signal q5 (red), decoupling signal q6 (blue).
C: Reference current q7 (blue).
D: Reference current q7 (green), converter current q8 (blue), error signal q9 (red).
E: Control signal PI controller q10 (green), output voltage feed forward signal q11 (red), decoupling signal q12 (blue).
F: Reference voltage converter q13 (blue).

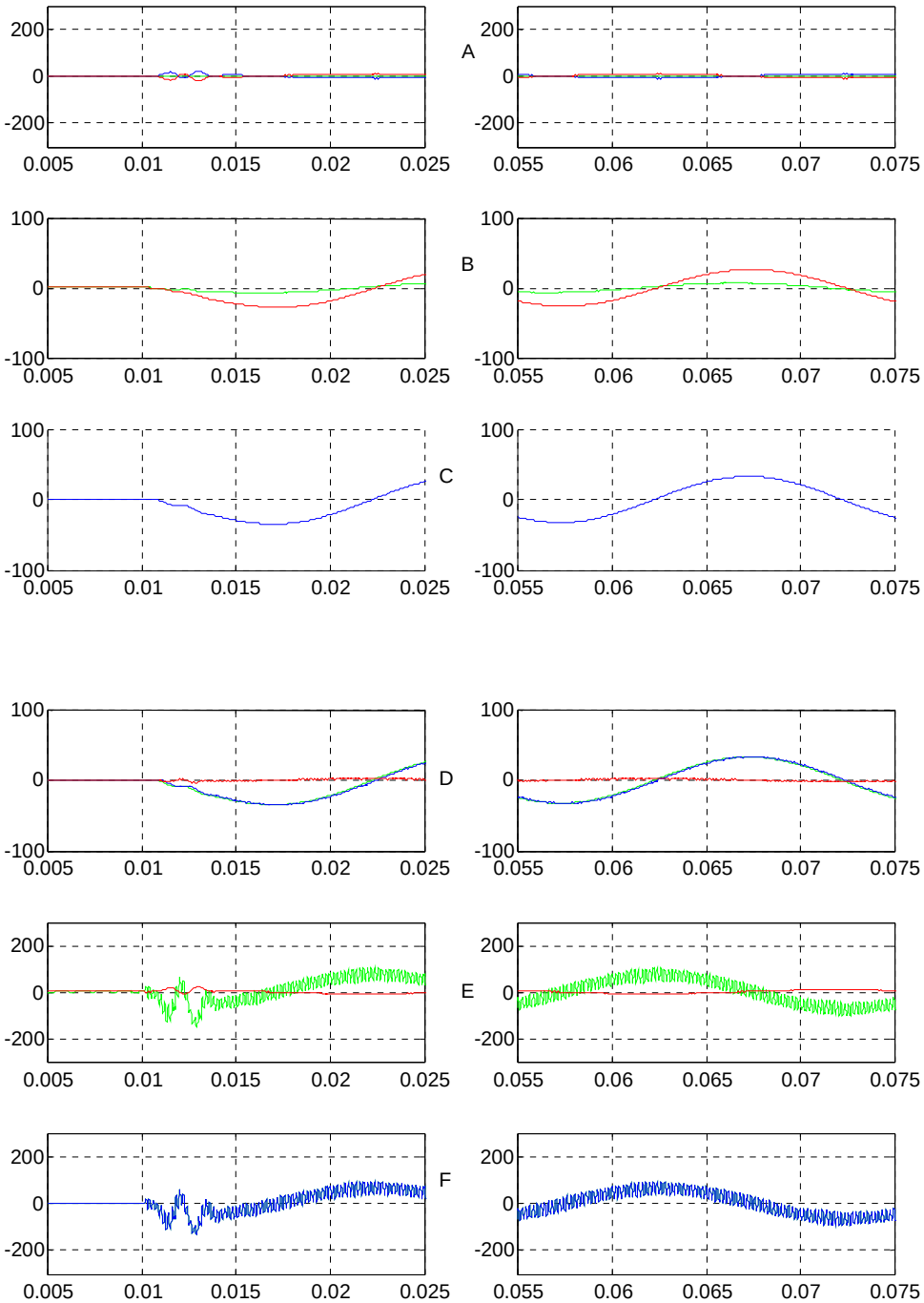


Figure E-10. Signals scenario 3, channel 0.

A: Reference output voltage 0-1 (green), output voltage 0-2 (blue), error signal 0-3 (red).
B: control signal PI controller 0-4 (green), load current feed forward signal 0-5 (red).
C: Reference current 0-7 (blue).
D: Reference current 0-7 (green), converter current 0-8 (blue), error signal 0-9 (red).
E: Control signal PI controller 0-10 (green), output voltage feed forward signal 0-11 (red).
F: Reference voltage converter 0-13 (blue).

Scenario 4:

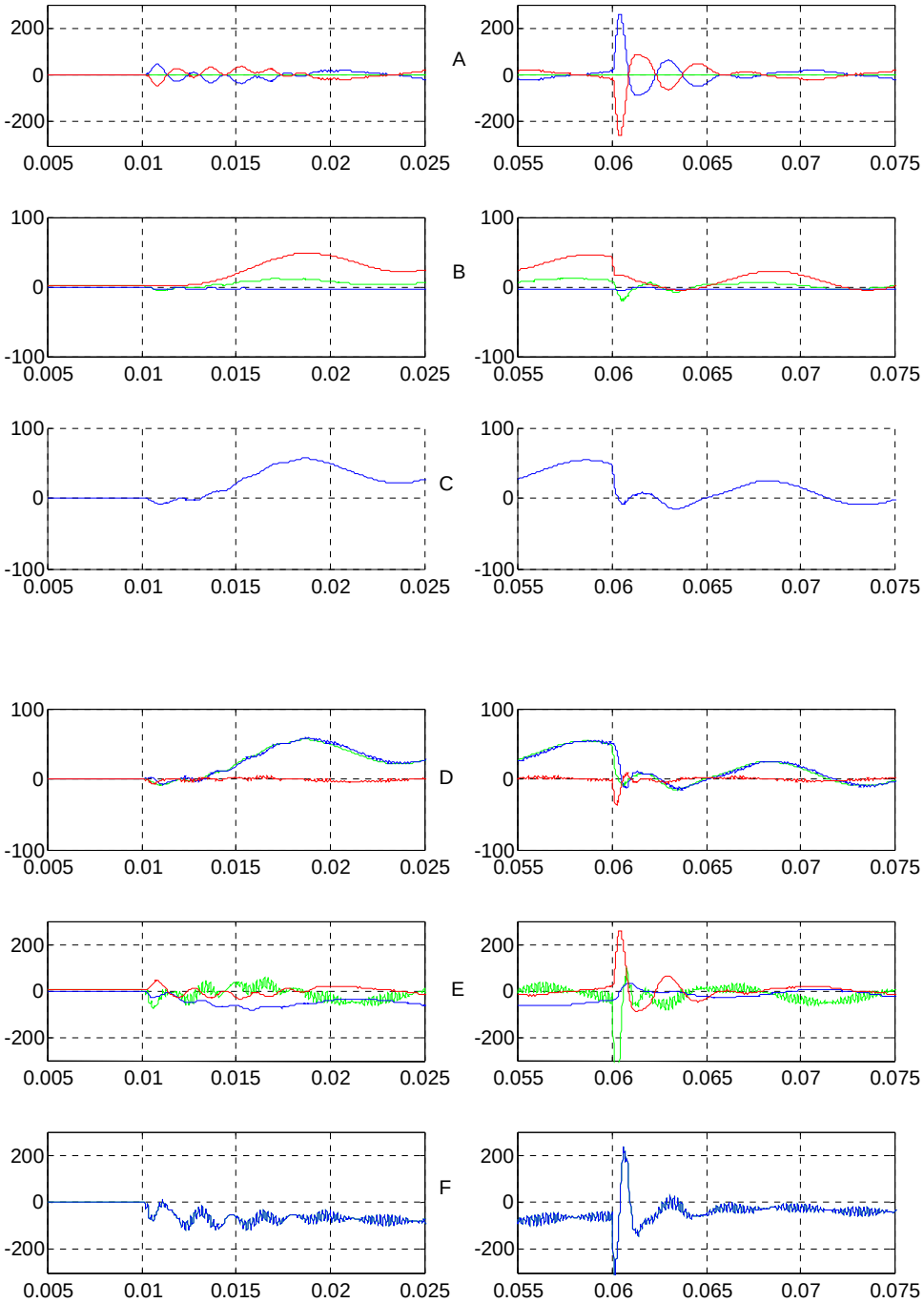


Figure E-11. Signals scenario 4, channel d.

A: Reference output voltage d1 (green), output voltage d2 (blue), error signal d3 (red).
B: control signal PI controller d4 (green), load current feed forward signal d5 (red), decoupling signal d6 (blue).
C: Reference current d7 (blue).
D: Reference current d7 (green), converter current d8 (blue), error signal d9 (red).
E: Control signal PI controller d10 (green), output voltage feed forward signal d11 (red), decoupling signal d12 (blue).
F: Reference voltage converter d13 (blue).

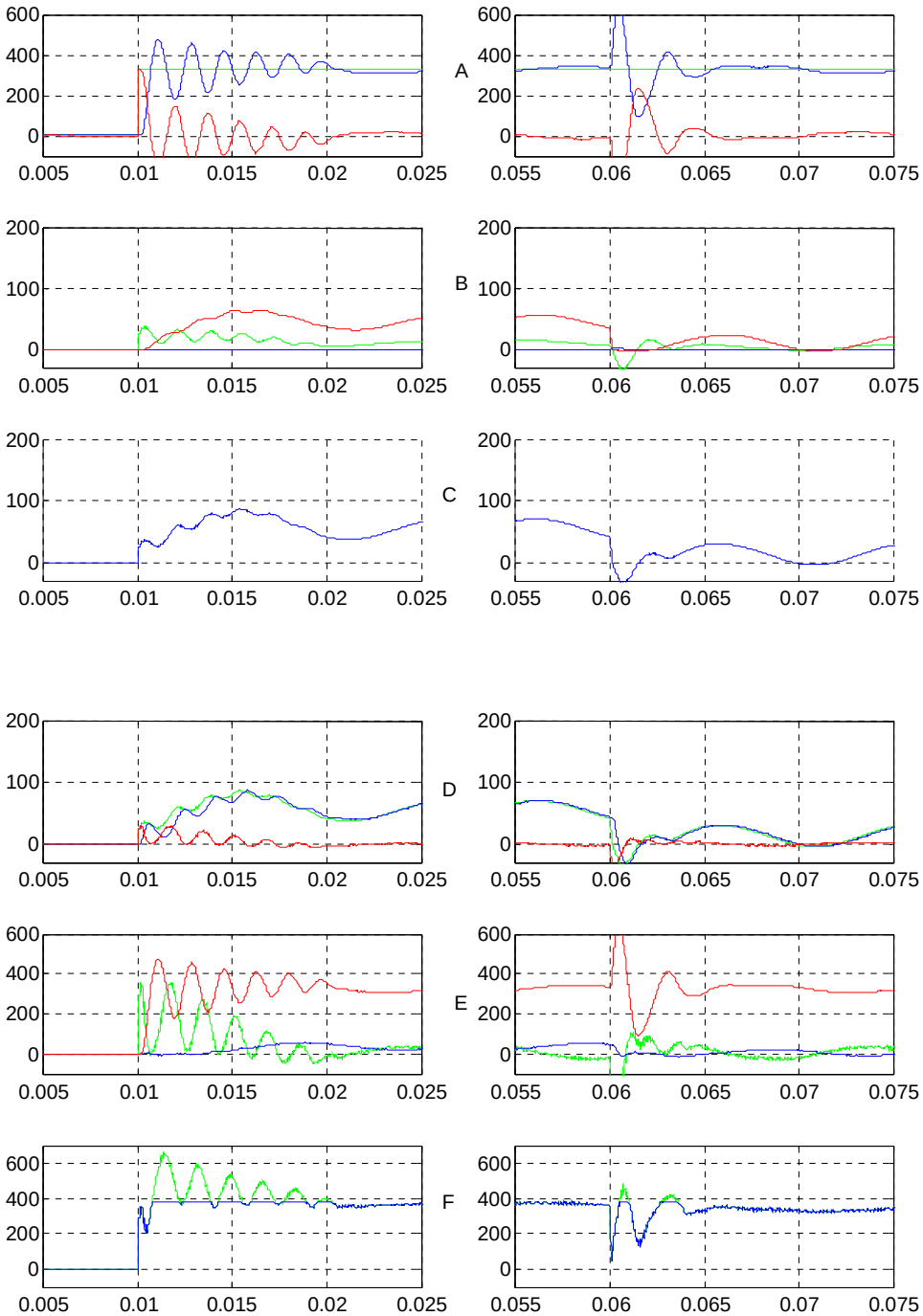


Figure E-12. Signals scenario 4, channel q.

A: Reference output voltage q1 (green), output voltage q2 (blue), error signal q3 (red).
B: control signal PI controller q4 (green), load current feed forward signal q5 (red), decoupling signal q6 (blue).
C: Reference current q7 (blue).
D: Reference current q7 (green), converter current q8 (blue), error signal q9 (red).
E: Control signal PI controller q10 (green), output voltage feed forward signal q11 (red), decoupling signal q12 (blue).
F: Reference voltage converter q13 (blue).

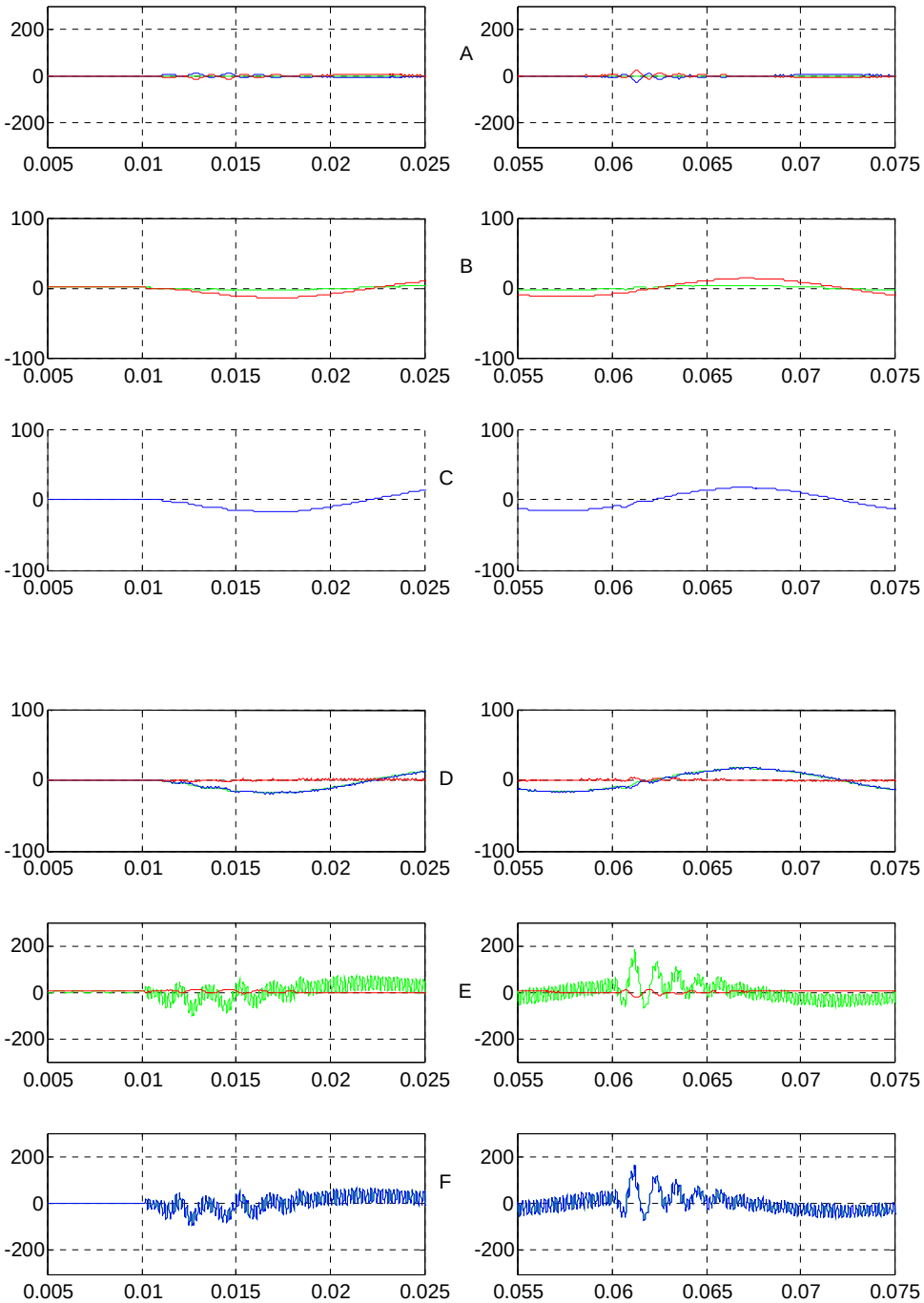


Figure E-13. Signals scenario 4, channel 0.

A: Reference output voltage 0-1 (green), output voltage 0-2 (blue), error signal 0-3 (red).
B: control signal PI controller 0-4 (green), load current feed forward signal 0-5 (red).
C: Reference current 0-7 (blue).
D: Reference current 0-7 (green), converter current 0-8 (blue), error signal 0-9 (red).
E: Control signal PI controller 0-10 (green), output voltage feed forward signal 0-11 (red).
F: Reference voltage converter 0-13 (blue).

Scenario 5:

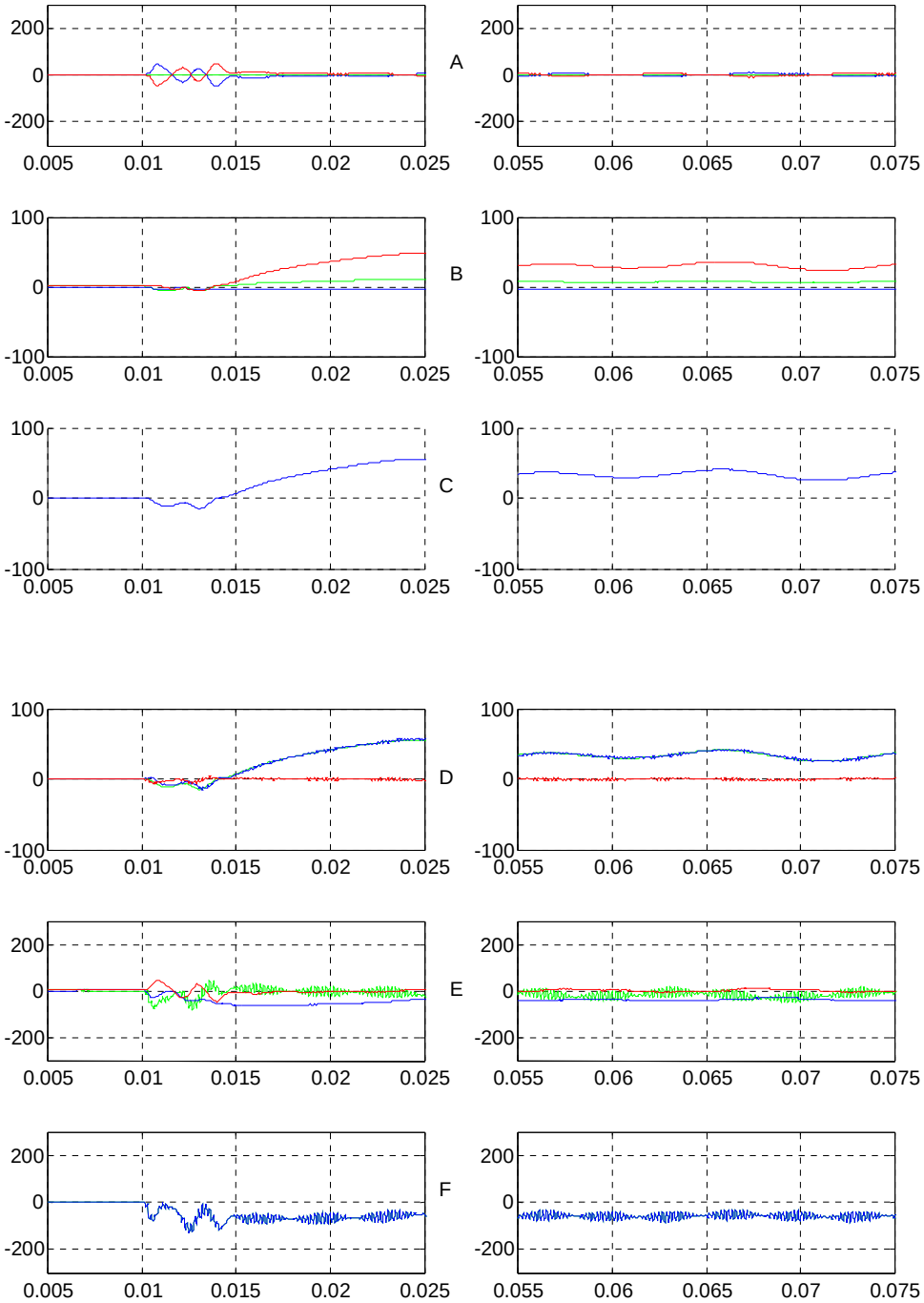


Figure E-14. Signals scenario 5, channel d.

A: Reference output voltage d1 (green), output voltage d2 (blue), error signal d3 (red).
B: control signal PI controller d4 (green), load current feed forward signal d5 (red), decoupling signal d6 (blue).
C: Reference current d7 (blue).
D: Reference current d7 (green), converter current d8 (blue), error signal d9 (red).
E: Control signal PI controller d10 (green), output voltage feed forward signal d11 (red), decoupling signal d12 (blue).
F: Reference voltage converter d13 (blue).

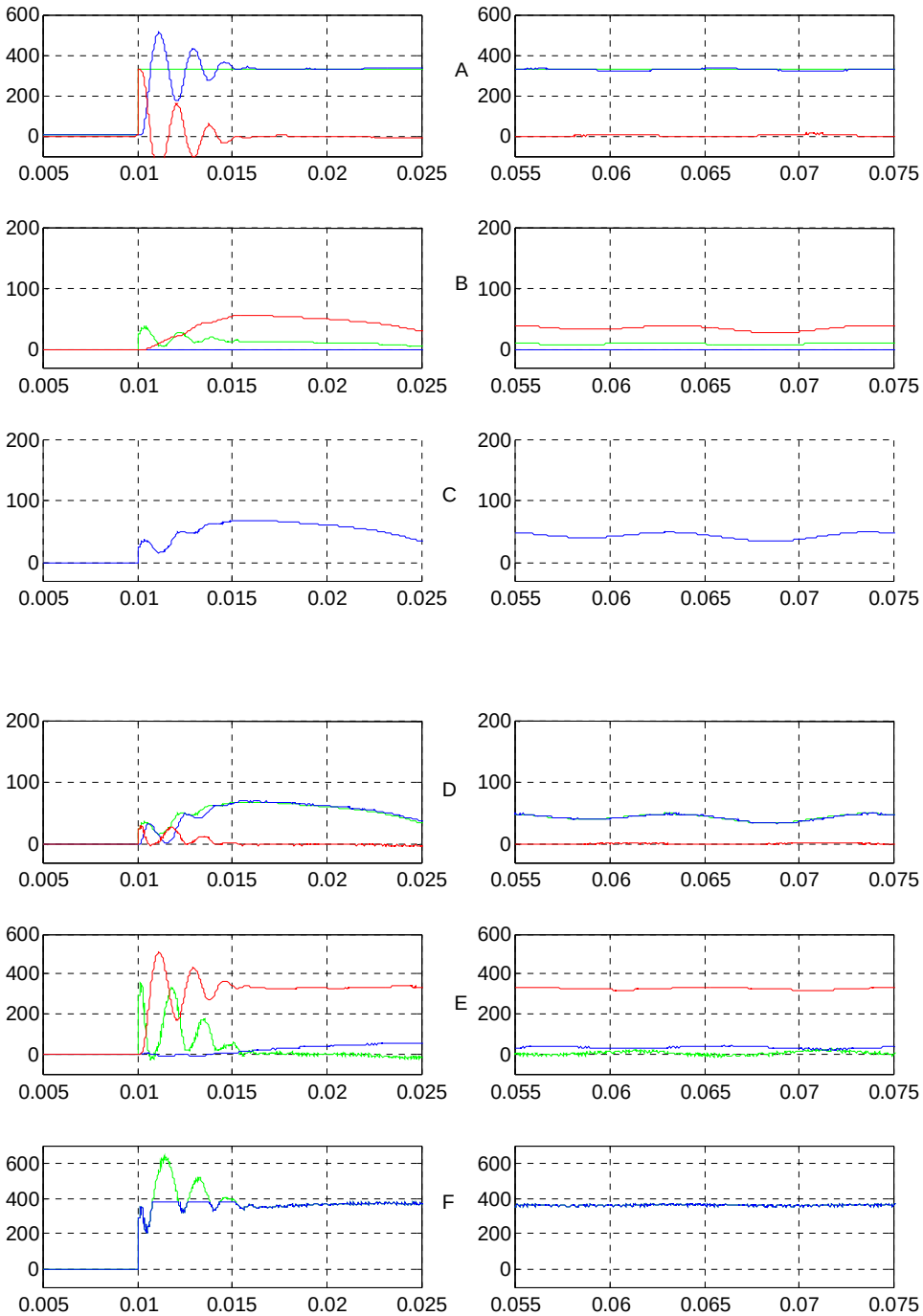


Figure E-15. Signals scenario 5, channel q.

A: Reference output voltage q1 (green), output voltage q2 (blue), error signal q3 (red).
B: control signal PI controller q4 (green), load current feed forward signal q5 (red), decoupling signal q6 (blue).
C: Reference current q7 (blue).
D: Reference current q7 (green), converter current q8 (blue), error signal q9 (red).
E: Control signal PI controller q10 (green), output voltage feed forward signal q11 (red), decoupling signal q12 (blue).
F: Reference voltage converter q13 (blue).

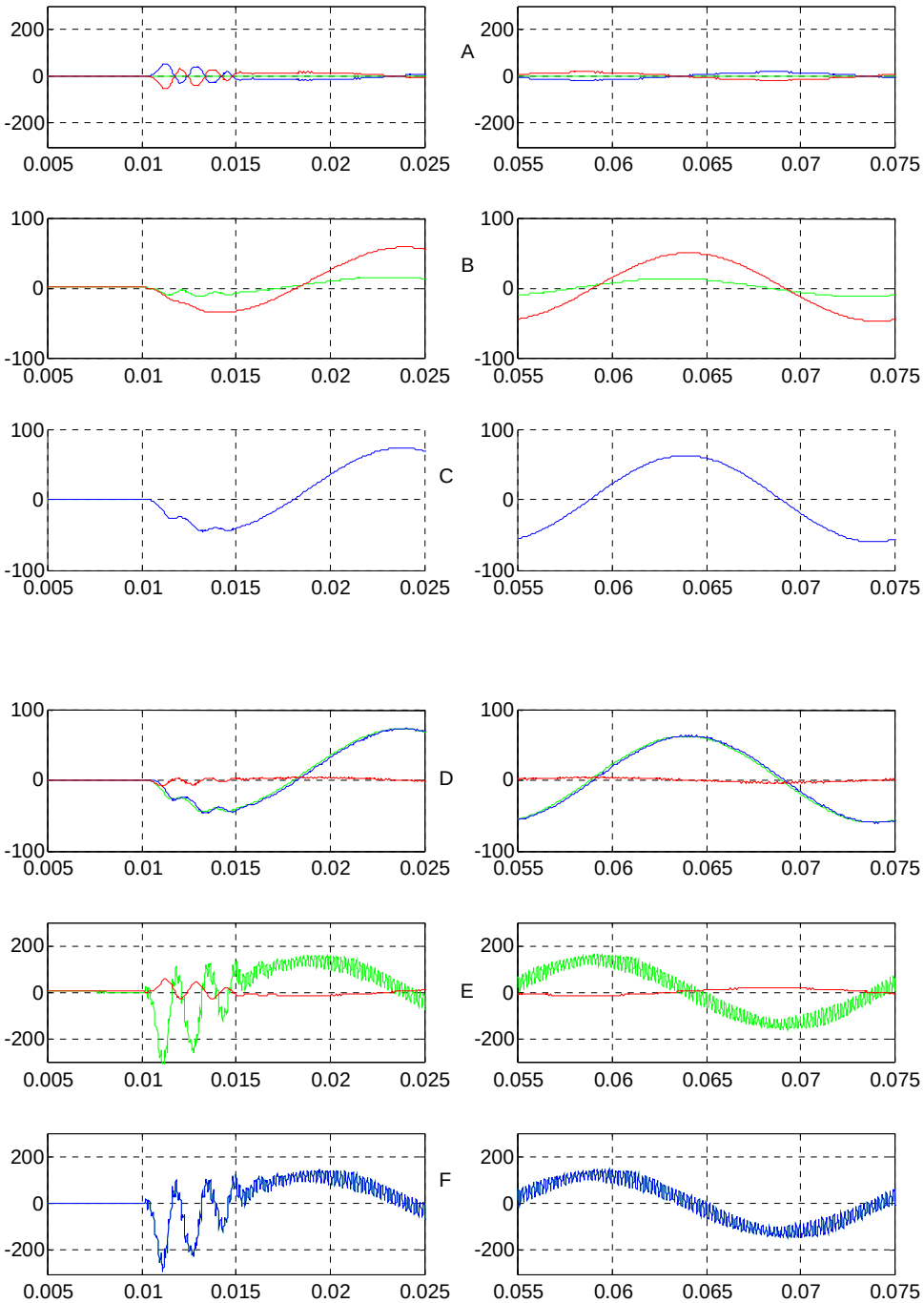


Figure E-16. Signals scenario 5, channel 0.

A: Reference output voltage 0-1 (green), output voltage 0-2 (blue), error signal 0-3 (red).
B: control signal PI controller 0-4 (green), load current feed forward signal 0-5 (red).
C: Reference current 0-7 (blue).
D: Reference current 0-7 (green), converter current 0-8 (blue), error signal 0-9 (red).
E: Control signal PI controller 0-10 (green), output voltage feed forward signal 0-11 (red).
F: Reference voltage converter 0-13 (blue).

Appendix F - Losses semiconductors

The losses for each half bridge, as well as total loss for the converter, during the simulated scenarios are calculated here. Both continues losses and average losses are presented. (The data providing the average loss calculations are measured when steady state is achieved during t = 0.04-0.06s and during t = 0.10-0.12s.)

Data are taken from data sheets of IGBT-modules; Semikron 200GB123D (on phase a, b and c half bridges) and Semikron 300GB124D (on neutral half bridge).

Scenario 1

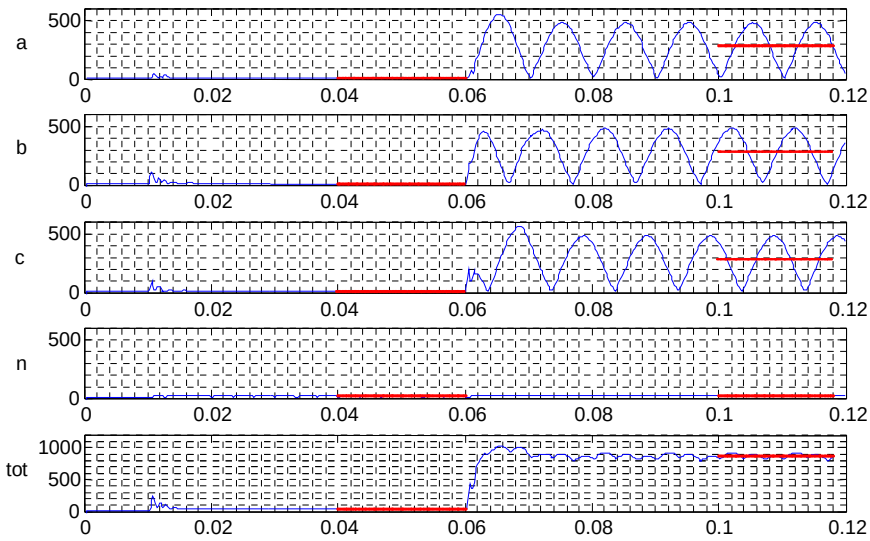


Figure F-1.Losses for each half bridge and total loss of the converter. Continuous losses (blue) and average losses during steady state (red).

The largest average loss of a half bridge is equal in all of the phase half bridges and about 300 W. The largest total average loss of the converter is about 900 W.

Scenario 2

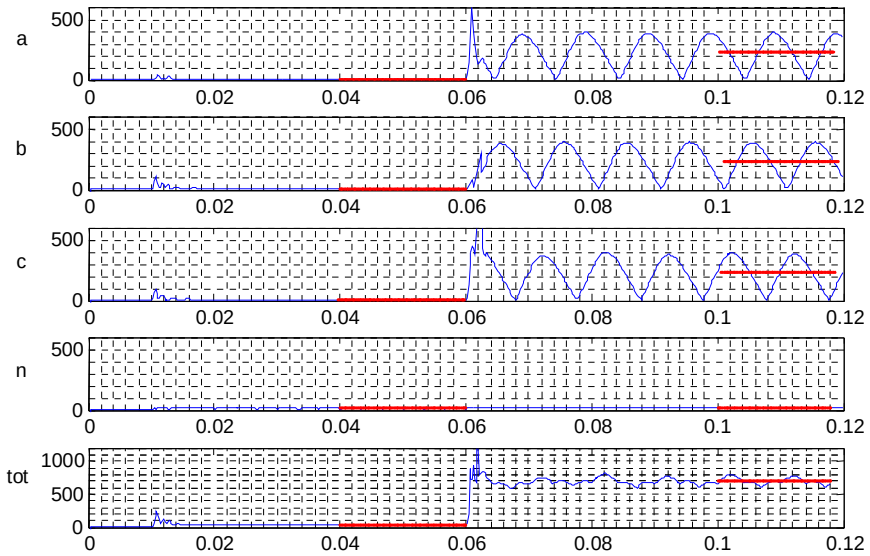


Figure F-2.Losses for each half bridge and total loss of the converter. Continuous losses (blue) and average losses during steady state (red).

The largest average loss of a half bridge is equal in all of the phase half bridges and about 250 W. The largest total average loss of the converter is about 750 W.

Scenario 3

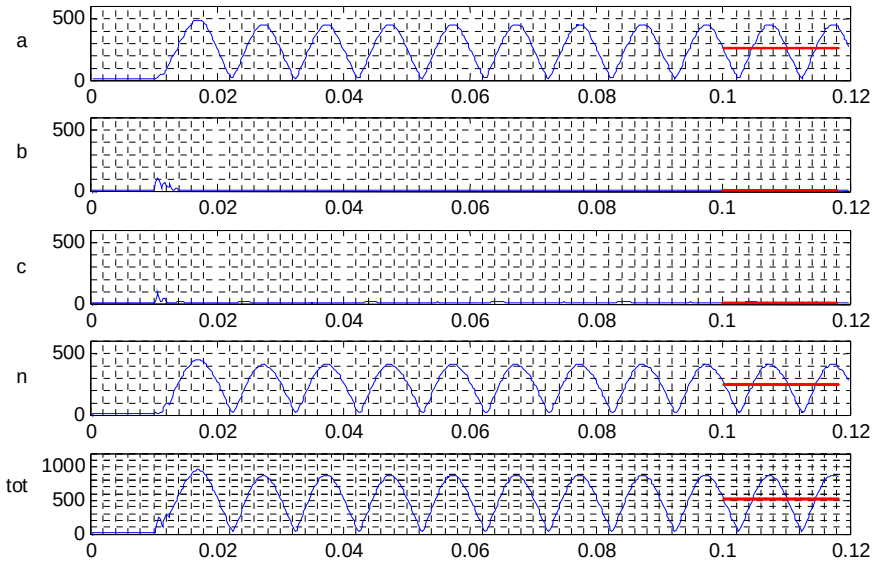


Figure F-3.Losses for each half bridge and total loss of the converter. Continuous losses (blue) and average losses during steady state (red).

The largest average loss of a half bridge is equal in the half bridge of phase a and the neutral half bridge and are about 275 W. The largest total average loss of the converter is about 550 W.

Scenario 4

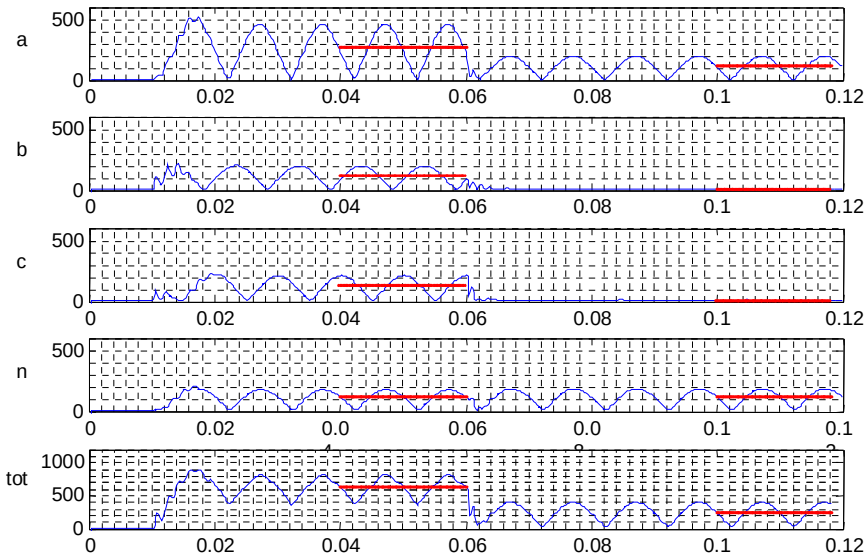


Figure F-4.Losses for each half bridge and total loss of the converter. Continuous losses (blue) and average losses during steady state (red).

The largest average loss of a half bridge is in the half bridge of phase a and is about 275 W. The largest total average loss of the converter is about 650 W.

Scenario 5

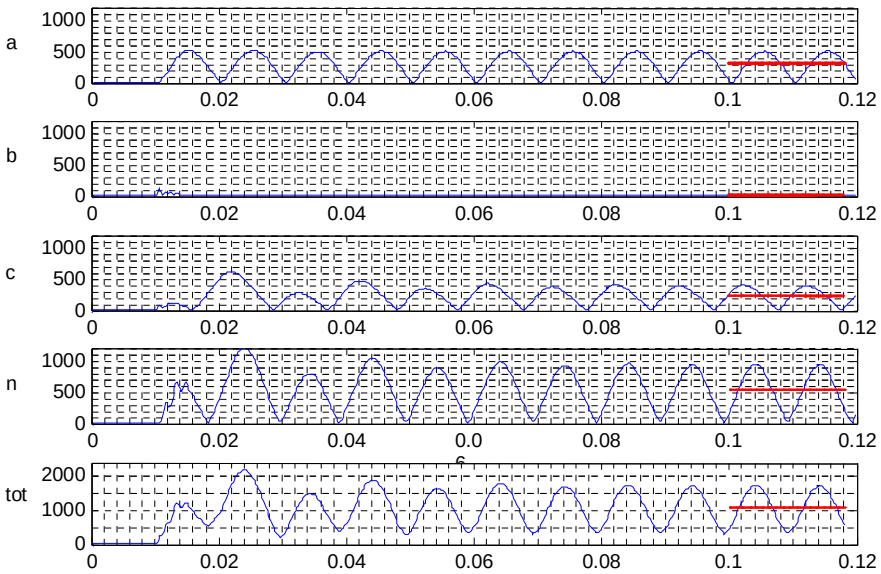


Figure F-5.Losses for each half bridge and total loss of the converter. Continuous losses (blue) and average losses during steady state (red).

The largest average loss of a half bridge is in the neutral half bridge and is about 550 W. The largest total average loss of the converter is about 1100 W.

Appendix G - Nomenclature

Abbreviations

ACM	Auxiliary Converter Module
DSP	Digital Signal Processor
ESR	Equivalent Series Resistance
IGBT	Isolated Gate Bipolar Transistors
PWM	Pulse-Width Modulation
SEP	Splitterskyddad Enhets Plattform
UPS	Uninteruptable Power Supply

Symbols

C	output filter capacitance
d_{an}	phase a to neutral duty ratio
d_{bn}	phase b to neutral duty ratio
d_{cn}	phase c to neutral duty ratio
d_d	duty ratio in d-direction in d-q-0 coordinates
d_{diode2}	duty cycle for diode2
d_{IGBT1}	duty cycle for $IGBT1$
d_q	duty ratio in q-direction in d-q-0 coordinates
d_0	duty ratio in 0-direction in d-q-0 coordinates
$E_{Drr,n}$	reverse recovery energy of free wheeling diode
E_{off}	turn off energy of IGBT given in data sheet
E_{off_diode2}	turn off energy of diode2
E_{off_IGBT1}	turn off energy of IGBT1
E_{on}	turn on energy of IGBT given in data sheet
E_{on_diode2}	turn on energy of diode2
E_{on_IGBT1}	turn on energy of IGBT1
e	input signal to controller
f	frequency
f_{ripple}	ripple frequency
f_{sw}	switch frequency

I_i	rms current through half bridge
I_{line}	rms line current
I_{load}	rms load current
I_n	current through IGBT at which E_{on} and E_{off} are given
I_{pp_line}	peak-to-peak of the rated output current
I_{pp_ripple}	peak-to-peak current ripple
i_a	converter current phase a
i_{a_load}	load current, phase a
i_b	converter current phase b
i_{b_load}	load current, phase b
i_c	converter current phase c
i_{c_load}	load current, phase c
i_d	converter current in d-direction in d-q-0 coordinates
i_{d_load}	load current in d-direction in d-q-0 coordinates
i_i	instantaneous current through half bridge
$\hat{i}_i$	peak current through half bridge
$\overline{i_i}$	average current through half bridge
i_n	converter current in neutral line
i_q	converter current in q-direction in d-q-0 coordinates
i_{q_load}	load current in q-direction in d-q-0 coordinates
i_0	converter current in 0-direction in d-q-0 coordinates
i_{0_load}	load current in 0-direction in d-q-0 coordinates
K	proportional gain of PI-controller
Kc_P	proportional gain of current PI-controller
Kv_P	proportional gain of voltage PI-controller
L	phase line inductance
L_n	neutral line inductance
M	Modulation index
$P_{cond,diode2}$	conduction loss power for diode2
$P_{cond,IGBT1}$	conduction loss power for IGBT1

P_{loss}	continuous power loss of one half bridge
$\overline{P}_{loss}$	average power loss of one half bridge
P_{off}	turn-off power of IGBT
P_{on}	turn-on power of IGBT
$\overline{P}_{sw,diode}$	average turn-off losses of diode
$\overline{P}_{sw,IGBT}$	average turn-on and turn-off losses for one IGBT
P_Y	load power, Y-connected load
P_Δ	load power, Δ-connected load
R_{C_esr}	Equivalent Series Resistance of C
$R_{diode(on)}$	on-state resistance of diode
$R_{IGBT(on)}$	on-state resistance of IGBT
R_{L_esr}	Equivalent Series Resistance of L
S_n	load power of the converter
Tc_i	integral time of current PI controller
T_d	time delay
T_n	period time
T_i	integral time of PI controller
T_{sw}	switch period time
Tv_i	integral time of voltage PI controller
t	time
U_{ab}	line to line voltage, phase a and phase b
U_{an}	line to neutral voltage, phase a and neutral
U_{bc}	line to line voltage, phase b and phase c
U_{bn}	line to neutral voltage, phase b and neutral
U_{ca}	line to line voltage, phase c and phase a
U_{cn}	line to neutral voltage, phase c and neutral
U_{load}	load voltage over one impedance Z
$U_{line-line}$	line to line voltage
$U_{line-neutral}$	line to neutral voltage
$\hat{V}_a$	peak voltage, phase a

$\hat{V}_b$	peak voltage, phase b
$\hat{V}_c$	peak voltage, phase c
V_{DC}	DC-link voltage
$V_{dc,n}$	voltage over IGBT at which E_{on} and E_{off} are given
$V_{diode(on)}$	forward voltage drop of diode
$\overline{V}_{diode(on)}$	average forward voltage drop of diode
$V_{diode,0}$	threshold voltage of diode
$V_{IGBT(on)}$	forward voltage drop of IGBT
$\overline{V}_{IGBT(on)}$	average forward voltage drop of IGBT
$V_{IGBT,0}$	threshold voltage of IGBT
v_a	phase voltage, phase a
v_{ab}	line to line voltage, phase a and phase b
v_{a_load}	load voltage of phase a
v_{an}	negative sequence voltage component, phase a
v_{ap}	positive sequence voltage component, phase a
v_{a0}	zero sequence voltage component, phase a
V_{base}	maximum length of voltage vector in linear modulation
v_{bc}	line to line voltage, phase b and phase c
v_{b_load}	load voltage of phase b
v_{bn}	negative sequence voltage component, phase b
v_{bp}	positive sequence voltage component, phase b
v_{b0}	zero sequence voltage component, phase b
v_{ca}	line to line voltage, phase c and phase a
v_{c_load}	load voltage of phase c
v_{cn}	negative sequence voltage component, phase c
v_{cp}	positive sequence voltage component, phase c
v_{c0}	zero sequence voltage component, phase c
v_d	voltage in d-direction in d-q-0 coordinates
v_q	voltage in q-direction in d-q-0 coordinates
v_{ref}	voltage reference
v_0	voltage in 0-direction in d-q-0 coordinates
$\overline{X}_{ab}$	vector in a-b-coordinates
$\overline{X}_{abg}$	vector in a-b-g-coordinates

Z_a	load impedance, phase a
Z_b	load impedance, phase b
Z_c	load impedance, phase c
j	phase displacement
w	angular frequency