The concept of IGBT modelling

and the evaluation of the PSPICE$^{\text{â}}$ IGBT model

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Abstract

The ability to calculate power losses in the Insulated Gate Bipolar Transistors (IGBTs) embedded in a series resonant converter is of great interest at ALSTOM Power, Växjö. Correctly estimated power losses are valuable in various situations, e.g. when evaluating new types of IGBTs or different control strategies. Therefore, it is desirable to investigate and evaluate the existing computer based IGBT models, where the majority is implemented in various circuit simulators.

In this thesis, the MicroSim® PSPICE® IGBT model is evaluated with respect to the application of the series resonant converter. Particularly, this involves the issues of conduction losses and switching losses both at hard and soft switching.

To be able to characterise a specific IGBT, a major parameter extraction procedure is performed, adapted from Hefner [7]. The parameters are subsequently used in the simulations and the result is compared with reference values of the measured power losses in the series resonant converter. This procedure is carried out for three different IGBTs from different manufacturers (Eupec, Semikron and Toshiba).

The evaluated model failed to comply with the stated specifications, mainly owing to the poor performance at soft switching with a capacitive snubber, and consequently, some possible future alternatives are given.

Acknowledgements

Fist of all, I sincerely would like to thank my supervisor at the department of Industrial Electrical Engineering and Automation (IEA), Per Karlsson, for his support and advice during this thesis.
Secondly, I am also very grateful to Per Ranstad, supervisor at ALSTOM Power, Växjö, for the possibility of conducting my master thesis at ALSTOM and for the continuous assistance and encouragement during my work.
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Contents

1 Introduction

1.1 Background

ALSTOM Power Environmental Systems produces and develops high frequency power converters (20 kHz, 100kW), for power supply in industrial applications. The converter includes a full-bridge inverter, Figure 1.1, where Insulated Gate Bipolar Transistors (IGBTs) constitute the switches.

When replacing switching devices by different models, or when developing new systems and strategies, switching and conduction losses are essential to know for the evaluation of the system. At ALSTOM today, losses are partly manually measured, which is a very time consuming process. A more efficient way of estimating losses would be to use a computer-model for calculation or simulation, which may also provide a more detailed study of the various components constituting the total losses. The purpose of this thesis is to examine existing models and to evolve and evaluate an appropriate model.

The model should be characterised by either information from datasheets or from measured characteristics. The dynamic characteristics and the performance at soft switching are of special interest. Moreover, the model should hold a margin of error of no more than 10 %.
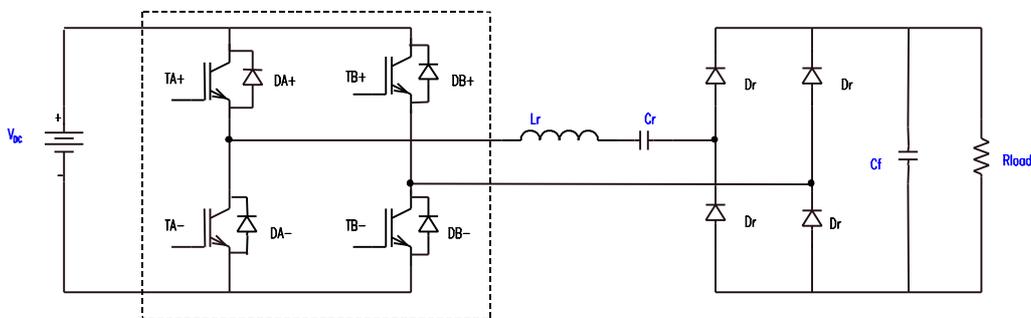
Figure 1.1 The series resonant converter including a full-bridge with IGBTs.

1.2 Working process

The starting point of this master thesis is the literary study, which starts with literature of power electronics to get basic background knowledge of converter topologies and semiconductors. To improve the understanding of converter design, the MicroSim® PSPICE® circuit simulator is used for simulations of fundamental converter topologies.

The subsequent survey of IGBT models involves a major information retrieval, basically with the Internet and the IEEE database of scientific papers, *IEEE Xplore*ä, as the principal source. After evaluation of the literary study, the conclusion is drawn that no simple model, for loss calculations only, is to be found and that a simulation model within a commercial simulator is the appropriate alternative. The final decision is made to evaluate the MicroSim® PSPICE® model since this is already available at ALSTOM and seems to have the potential of desired accuracy.

The literary study also brought forward the importance of a parameter extraction procedure to characterise different devices correctly. Hefner [3]-[8] has done extensive research in the area of modelling semiconductors and since much of his work composes the basis of the PSPICE® model, also the parameter extraction procedure developed by him is adopted. Further simulations are executed to verify the procedures and circuits for the chosen set of parameters. Subsequently, design and construction of the extraction circuits as well as gate drive units are performed.

The various measurements of the extraction procedure are logged on a computer, via an oscilloscope, to perform mathematical operations and curve fitting algorithms on the collected data. The processing of data is done in MATLAB® and the resulting parameters logged in an ordinary spreadsheet file.

The final part of the evaluation process is to design a simulation model of the series resonant converter, including the IGBTs with adherent parameters, and to simulate the different scenarios in accordance with the reference measurements of the total losses.

1.3 Thesis outline

In Chapter 2 and 3, the series resonant converter, basic snubbers and relevant semiconductors are studied in order to present the fundamental facts to the reader. Some basic circuit- and semiconductor-knowledge is required, however, the important concepts are explained in general and the detailed studies are left to the interested reader.

Chapter 4 involves the literary study made and the aspects of the evaluation. The parameter extraction procedure, as well as the designed circuits, is presented in the subsequent chapter, Chapter 5, along with results and comments. In Chapter 6 the simulation tool and the performed simulations are reviewed. Finally, the thesis is concluded in Chapter 7.

2 Converter topology

Most electrical systems like computers, battery chargers, television sets etc. are operated at other voltage levels and functions than what is delivered by the line supply voltage. To adapt the voltage to the desired level, different kinds of *converters* are used and these can be categorised into *ac/dc, dc/dc, ac/ac converters.* Here ac/dc converters are assumed to have bi-directional flow of power and no distinction is made between conversion from ac to dc (rectifier*)* or dc to ac (inverter). Not only the voltage level (amplitude) can be transformed with a converter; frequency and phase may also be altered arbitrarily.

Depending on the requirements and prerequisites of the system, there are numerous different topologies for each specific converter category [19], [20]. Nevertheless, there are some factors that are common to all applications; the aim to minimise the losses during conversion and the building blocks of switches (semiconductor devices) and energy storage elements (inductors and capacitors). To enhance the first factor, additionally circuit elements may be added to the basic topologies to minimise overvoltages or the rate of rise of the voltage/current. In the first part of this section, the fundamentals of such elements, referred to as snubbers, are studied. In the subsequent section, the converter of special interest in this thesis, the *series resonant converter,* is investigated. For a more detailed understanding of different converter topologies and snubber circuits, refer to [19] – [22].

2.1 Snubber circuits

Snubber circuits are used to reduce the stresses on semiconductor devices e.g. by minimising overvoltages during turn-off caused by stray inductances, limiting the rate of rise of the current during turn-on or enhance the switching trajectories to reduce the switching losses. There are multiple types of snubber circuits depending on the embedding circuit and type of semiconductor, as well as the purpose of the snubber. Consequently, diodes demand different snubbers than thyristors, turn-on snubbers differ from turn-off snubbers for transistors and additionally snubbers are needed in bridge applications [20].

For the series resonant converter, as will be discussed later, the purely capacitive snubber is sufficient enough and is therefore, along with the RCD-snubber, the only snubber studied here.

Hard switching

The step down converter is a fundamental bridge configuration and is shown in Figure 2.1. The current source acts like an inductive load and the current is carried by the power transistor (IGBT in this case) during on-state, and by the freewheeling diode during off-state.
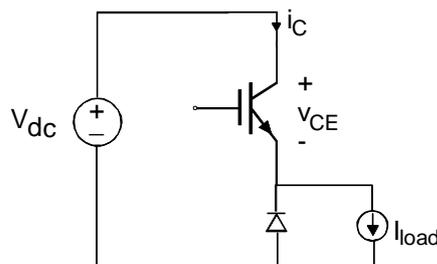
Figure 2.1 The step down converter.

In Figure 2.2, the collector current and collector-emitter voltage transients during switching of the step down converter are illustrated. The simulation values (in [21]) for the load current and the dc link voltage are $I_{\text{load}} = 0.8I_C$ and $V_{\text{dc}} = 0.6V_{\text{CES}}$, where I_C is the rated maximum collector current and V_{CES} is the rated maximum collector-emitter voltage. Note that the voltage and current are expressed in per unit of the normalisation values I_C and V_{CES}.

During turn-on, the semiconductor is exposed to a high current peak as a consequence of the reverse recovery of the freewheeling diode (section 3.1). At the same time the collector-emitter voltage is still high, thus, causing high switching losses. During turn-off, the losses can be even higher due to the long collector current tail (section 3.4). The semiconductor is, under these conditions with simultaneously high current and voltage, said to be operating under *hard switching.*
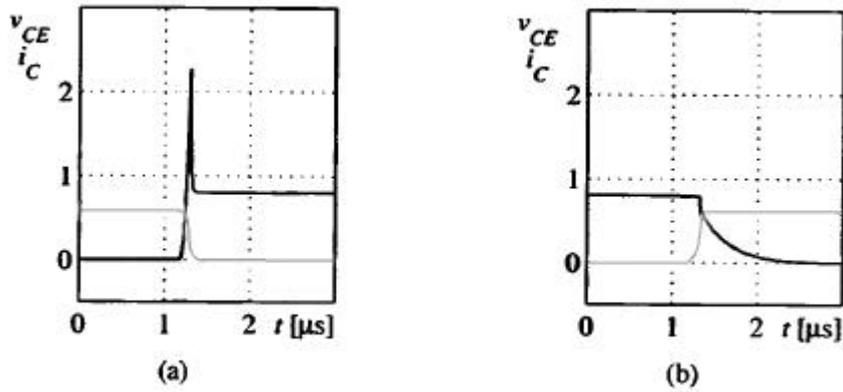
Figure 2.2 Normalised transistor current (black) and voltage (grey) during a) turn-on and b) turn-off of the power transistor in the step down converter [21].

The capacitive snubber

Extensive losses can cause critical junction temperatures or force the transistor to operate outside the Safe Operating Area and subsequently cause device failure. To avoid this, a snubber circuit is added to the converter, like in Figure 2.3.
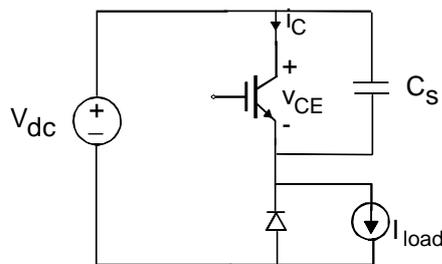
Figure 2.3 The step down converter with a capacitive snubber.

The purpose of the capacitor, C_s, added in parallel with the transistor, is to offer an alternative way for the load current at turn-off and simultaneously raise the collector-emitter voltage as in Figure 2.4b. This is not possible at hard switching, when the only alternative path for the current is through the freewheeling diode, which has to be forward biased to conduct, resulting in that approximately the entire dc link voltage, V_{dc}, is applied across the transistor during the fall time of the current.
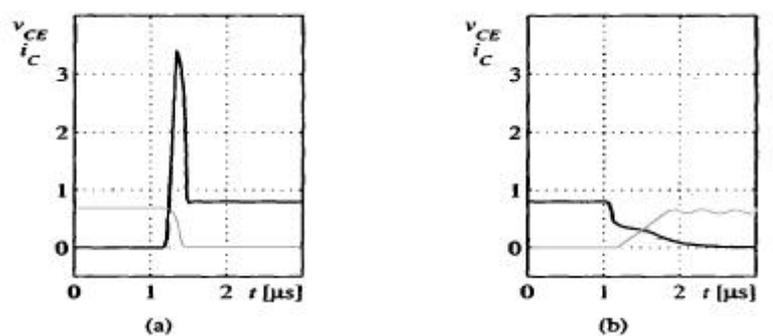
Figure 2.4 Normalised transistor current (black) and voltage (grey) during a) turn-on and b) turn-off of the power transistor in the step down converter with a capacitive snubber. Note the collector current peak at turn-on, and the simultaneously change of the collector current and collector-emitter voltage at turn-off [21].

Switching with snubber circuit embedded is usually referred to as *soft switching,* or like in this case, zero voltage switching (ZVS), owing to the collector-emitter voltage level at the start of the turn-off switching sequence. This actually lowers the turn-off losses, and furthermore, can enhance the electromagnetic compatibility (EMC) by

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reducing the derivative of the collector-emitter voltage. However, apparent from Figure 2.4a, the drawback of lower turn-off losses is the higher collector current peak at turn-on, adding stress to the transistor.

At the instant of turn-on, the capacitor is fully charged and since the freewheeling diode is still conducting, the capacitor voltage equals the full dc link voltage. The diode becomes reversed biased at the peak of the reverse recovery current and at this moment the capacitor can be discharged through the transistor, causing the peak of the collector current during turn-on, Figure 2.4a.
The value of the capacitor should be chosen in a way where the capacitor voltage reaches its off-state level at the same time as the current reaches zero [22], as in Figure 2.4b. If a lower capacitor value is applied, the capacitor voltage reaches the full dc link voltage before the current has reached zero, and if a higher value is chosen the discharge current at turn-on is increased. The mathematical expression for the optimal capacitor value can be found in Appendix A.1.

The charge-discharge RCD snubber
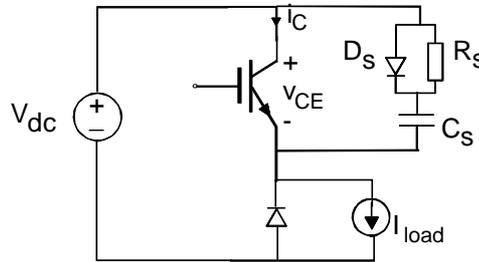
To decrease the current stress of the transistor at turn-on, the discharge current has to be limited. This is done by a charge-discharge RCD snubber [21], further on only referred to as RCD snubber, shown in Figure 2.5.

Figure 2.5 The step down converter with a RCD snubber.

The diode is connected in parallel with the resistor to bypass the current at turn-off when the capacitive snubber is efficient, and the resistor only would cause higher losses. However, at turn-on, the capacitor is discharged through the resistor and the discharge current carried by the transistor is limited. During turn-on at hard switching, the transistor carries both the load current and the reverse recovery current, and at soft switching with a snubber, the transistor carries the sum of the load current and the discharge current when the freewheeling diode has recovered. Consequently, to not increase the stresses on the transistor, caused by the snubber compared to those caused by the freewheeling diode, the resistor value should be chosen in a manner to limit the discharge current to be lower than the reverse recovery current, I_{rr}. This gives a resistor value of

$$R_S > \frac{V_{dc}}{I_{rr}}$$

However, the resistor value should not be chosen too high, since that would slow down the voltage decline and the capacitor should be fully discharged before the next turn-on to be efficient.

2.2 The series resonant converter

The series resonant converter constitute one part of a group called load resonant converters [20]. As the name implies, the converter consist of a resonant part composed by inductors, capacitors and resistors and where usually the latter is part of the load. The purpose of this circuit is to offer soft switching (ZVS or ZCS), according to the resonant behaviour of the converter, resulting in lower switching losses, which in turn may facilitate a higher switching frequency.

A series resonant DC to DC full-bridge converter is shown in Figure 2.6, where the resonant LC tank is connected to the load via a rectifier. Without the rectifier, the circuit is referred to as a series resonant DC to AC converter.
A transformer may be included before the rectifier to provide an output voltage of desired magnitude as well as electrical isolation between in- and output.
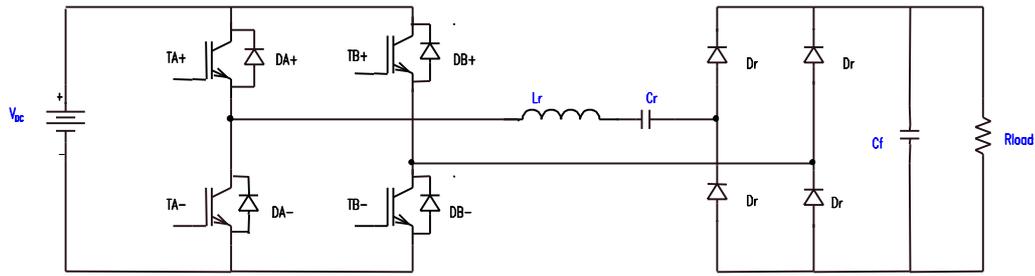
Figure 2.6 A series resonant DC-DC full bridge converter.

To simplify the analysis of the series resonant converter, only a half-bridge, Figure 2.7, is studied. The operation of the switches and the output waveforms are identical, with the addition of the operation of one switch in the half-bridge converter (e.g. T_+) corresponding to the operation of two switches, in antiparallel (T_{A+} and T_{B-}), in the full-bridge converter. The transistors in the full-bridge are in Figure 2.7a replaced by ideal switches, the resonant tank consists of L_r and C_r and the capacitance of the output capacitor, C_f, is usually large to make the output ripple low.
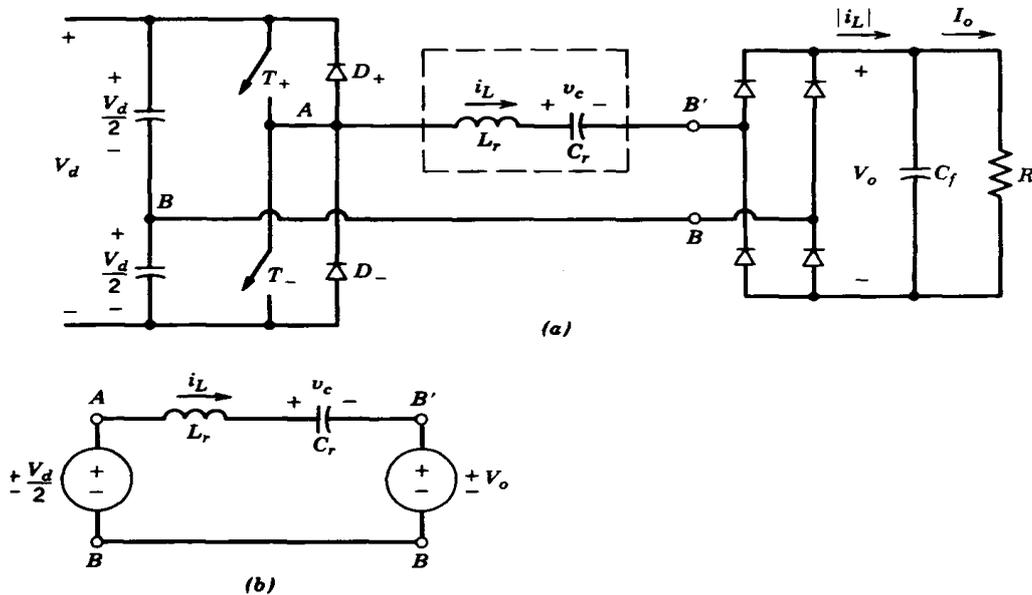
Figure 2.7 Series resonant converter: a) half-bridge b) equivalent circuit[20].

The output waveform and the internal state of the converter is depending on the direction of the flow of the current and which device that is conducting. When i_L is positive, it flows through the transistor, T_+, if it is on and through the diode, D_-, otherwise and the output voltage, V_o, is reflected across the rectifier so that $V_{B'B}=V_o$. When the current reverses, it commutates to the opposite transistor and diode (T_- and D_+) and $V_{B'B} = -V_o$.

This sequence of operation can be described by an equivalent circuit illustrated in Figure 2.7b, and the different states during one period are:

$$for\ i_L > 0$$

$$T_+\ conducting:\quad v_{AB} = +\tfrac{1}{2}V_d \quad v_{AB'} = +\tfrac{1}{2}V_d - V_o$$

$$D_-\ conducting:\quad v_{AB} = -\tfrac{1}{2}V_d \quad v_{AB'} = -\tfrac{1}{2}V_d - V_o$$

$$for\ i_L < 0$$

$$T_-\ conducting:\quad v_{AB} = -\tfrac{1}{2}V_d \quad v_{AB'} = -\tfrac{1}{2}V_d + V_o$$

$$D_+\ conducting:\quad v_{AB} = +\tfrac{1}{2}V_d \quad v_{AB'} = +\tfrac{1}{2}V_d + V_o$$

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The derivation of the output waveforms for the basic undamped series-resonant circuit is given in Appendix A.2. The resonant converter has a resonance frequency equal to

$$\omega_0 = 2\pi f_0 = \frac{1}{\sqrt{L_r C_r}}$$

and the converter can be operated in different modes depending on whether the switching frequency is lower or higher than the resonance frequency. In this study, only continuos-conduction mode, with $\omega_s > \omega_0$, is considered.

During this mode of operation, the switches turn-on at both zero voltage and zero current but are forced to turn off at a finite current. Starting at $\omega_0 t_0$ in Figure 2.8, the transistor T_+ starts conducting the reversing positive current and when T_+ is gated off, at $\omega_0 t_1$, T_- is gated on. However, the current is still positive and therefore commutates to the diode, D_-, but declines quickly towards zero because of the great negative voltage applied over the LC tank (- $V_d/2 - V_o$). When the current becomes negative, it is carried by T_- and an identical half-cycle as the first one is started.

As mentioned earlier, during this mode of operation, the switches turn on at zero current and also (nearly) zero voltage (because the parallel freewheeling diode is conducting, hence, is forward biased, prior to turn-on). This means the reverse recovery characteristicof the freewheeling diode is not of importance since the current has reached zero at turn-off of the diode. Another advantage of the simultaneously ZVS and ZCS, is that lossless turn-off capacitors in parallel with the transistors can be used as turn-off snubbers.
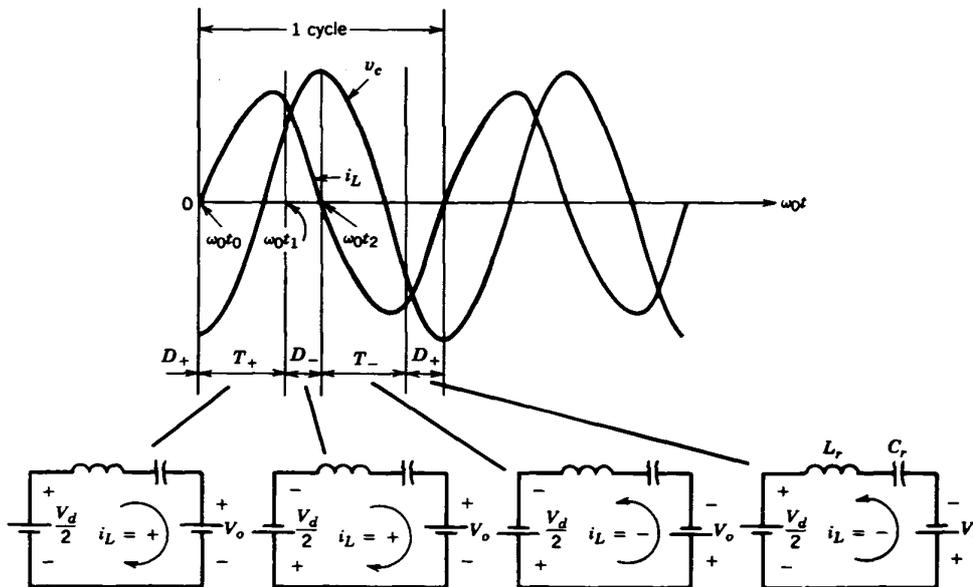
Figure 2.8 Series resonant converter, continuos conduction mode ($\omega_s > \omega_0$)[.20].

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3 Power semiconductors

Power semiconductors are substantially different from ordinary logic-level semiconductors considering structure and characteristics. In this chapter the most important and basic features of the power diode, bipolar junction transistor (BJT), metal oxide semiconductor field effect transistor (MOSFET) and the insulated gate bipolar transistor (IGBT) are studied. The reader is assumed to have some basic knowledge of semiconductor physics and be familiar with common terms like the *pn*-junction, recombination, lifetime, drift and diffusion.

The following subsections are a summary of the more comprehensive texts about semiconductors found in [20] and [22].

3.1 Power diodes

Basic structure and i-v characteristics

The basic structure of the power diode is the simplest form of all semiconductors and the fundamental building block for all semiconductor devices. The cross-section of a power diode is illustrated in Figure 3.1a and it is realised by epitaxial growth of a lightly doped n^- layer on top a heavily doped n^+ layer. The thickness of the n^- layer, also referred to as the drift region, is dependent on the desired breakdown voltage. To form the *pn*-junction, a heavily doped p^+ region is diffused into the drift region.
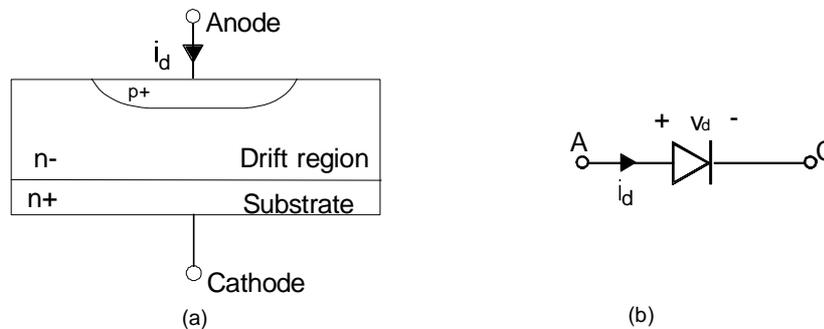
Figure 3.1 a) Cross section of power diode and b) circuit symbol.

The feature that distinguishes the power diode from the signal level diode is the drift region, which is specific to all power semiconductors, and enables the depletion layer to grow into the drift region at reverse blocking voltages. Devices with high breakdown voltages, hence, thick drift regions, would logically have a high resistivity on account of its thick, lightly doped layer. However, the conductivity modulation (discussed later) of the drift region reduces this problem in all bipolar devices (i.e. devices utilising minority carrier injection).

The typical *i-v*-characteristic of a power diode is shown in Figure 3.2. It resembles the characteristic of a signal level diode with the difference of an ohmic curvature, instead of an exponential, in forward bias. This is due to the ohmic resistance of the drift region appearing at the high current levels applied to power diodes. At reverse bias only a low leakage current is allowed to flow until the breakdown voltage, BV_{BD}, is reached and avalanche breakdown occurs with device failure as a possible consequence.
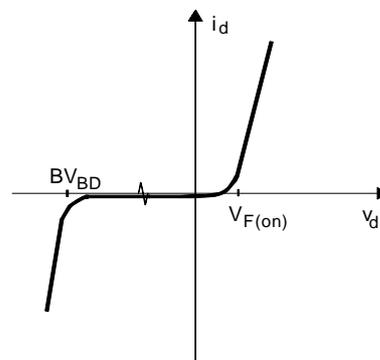
Figure 3.2 The *i-v* characteristic of the power diode.

Non-punch-through and punch-through diodes

There are two different ways of designing the breakdown voltage rating of a diode. The first one is to make the drift region wide enough to maintain the entire depletion region, which is called *non-punch-through* diodes. The second approach is to have a more lightly doped drift region, where the depletion region extends all the way to the n^+ substrate, however, not much further into the layer because of the heavy doping in the substrate. Practically, this results in a *punch-through* diode with half the thickness of the drift region compared to a non-punch-through diode with the same rated breakdown voltage.

On-state losses and conductivity modulation

The total losses of semiconductors can principally be divided into on-state losses (or conduction losses) and switching losses, ignoring off-state losses during reverse bias. For the power diode, at least for medium switching frequencies, the on-state losses are predominant and mostly dissipated in the drift region. For signal level diodes, the voltage across the diode under forward bias can be said to be constant and approximately equal to 0.7 V. If the current flowing through the diode is defined as *I*, the dissipated power would be given by *P=0.7*I*. Yet, this would lead to an underestimation of the losses in the power diode on account of the ohmic resistance in the drift region.
Calculating this resistance on basis of geometry and equilibrium carrier densities, not considering the effect of the carrier injection into the drift region, also referred to as the *conductivity modulation,* would also lead to false results.
When the *pn*-junction is forward biased, holes are injected from the anode into the drift region. At low-level injection these holes are in minority compared to the thermal equilibrium value of the electron concentration of the lightly doped n^- drift region. However, at high-level injection the number of injected holes widely overcomes the quantity of electrons of the drift region, thus, creating a space charge of holes. This space charge attracts electrons from the n^+ substrate, which start to drift towards the injected holes while recombining along the way. This phenomenon is called *double injection* and results in a much lower ohmic resistance of the drift region than at thermal equilibrium.

Switching characteristics

Losses during the switching period depend both upon the switching times as well as the curvature of the voltage and current during that time. Furthermore, these factors are affected by both the intrinsic properties of the device as well as the interaction with the surrounding circuit. An example of this is the time rate of change, *di/dt,* which often is controlled by circuit inductances or by the turn-off of a solid-state device where the diode serves as a freewheeling diode.
In Figure 3.3 the switching period can be divided into five different time intervals, where t_{ri} and t_{fr} represent the turn-on transient and t_{fi} and t_{rr} the turn-off transient.

Turn-on transient
During $t_{ri,}$ the space charge within the depletion region, upheld by the high reverse bias, is removed and at the end of t_{ri}, the depletion layer has reached its thermal equilibrium level. At the start of the second phase, t_{fr}, the *pn*-junction is now forward biased and injection of minority carriers commences and the excess-carrier distribution grows towards the steady-state value supported by the current I_0. The great voltage overshoot, built up during $t_{ri,}$ is due to the ohmic resistance in the drift region, where the conductivity modulation not yet is fully developed, in addition with the voltage contributed by stray inductances in the wafer and bonding wires. When the current has reached its maximum value, I_0, *di/dt* approaches zero, hence, the voltage caused by stray inductances reduces along with the voltage drop over the drift region, which is shorted out by the vast amount of excess carriers. Nevertheless, the peak voltage during this period may reach several tens of volts and can affect the performance of the circuit.

Turn-off transient
The turn-off sequence is basically the reverse of the turn-on sequence. Starting at $t_{fi,}$ the excess charge is removed from the drift region and this carrier sweep out is continued by the negative diode current during t_{rr1}, in addition with the recombination process. When all the excess charge at the ends of the drift region is swept out, the junctions can become reversed biased (t_{rr2}) and the depletion regions expand into the drift region from both

junctions. The excess carriers are now too few to sustain the current required by the inductive circuit and the negative diode current decays towards the off-state leakage level.

The interval during which the diode current is negative is called *reverse recovery*. This is an important characteristic and is always stated in data sheets in terms of the recovery time, t_{rr}, the negative peak of the diode current, I_{rr}, and the reverse recovery charge, Q_{rr}.
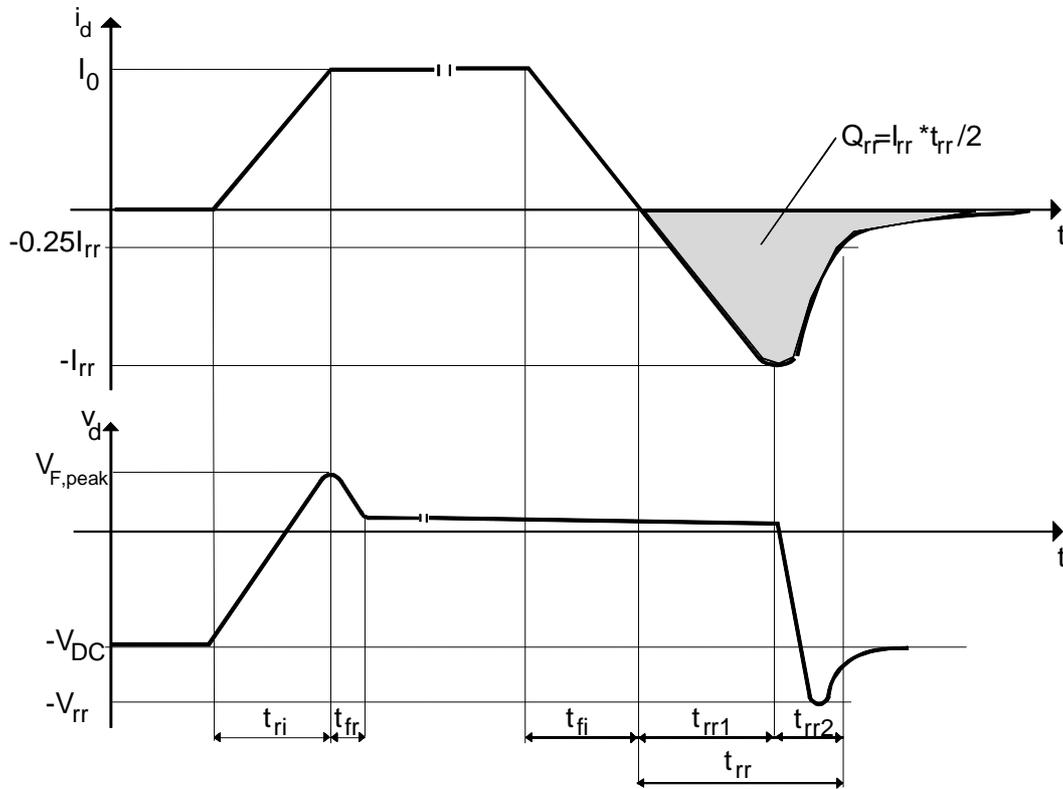
Figure 3.3 Switching trajectories for the power diode.

Important features of bipolar devices

The design of all power semiconductor devices is a trade-off between properties like breakdown voltage, on-state losses and switching losses and this has to be considered when choosing devices for a specific purpose.

Compared to majority carrier devices like MOSFETs and JFETs, the on-state voltage drop for bipolar devices can be made low and virtually independent of the current. This is accomplished by making the lifetime sufficiently long for the diffusion length, L, to be comparable with the drift region length, W_d. A drawback of lower on-state losses is the amount of stored charge in the drift region, owing to the enhanced carrier injection, resulting in longer switching times as was evident in previous subsection. Finally, the demand for higher breakdown voltages requires thicker drift regions since the voltage drop across the drift region is proportional to the square of its length, W_d.

Schottky diodes

A diode with basically the same *i-v* characteristics as the one previously discussed is the Schottky diode.

The structural difference is the p^+ layer replaced by a metal film on top the n^- layer. Electrons have different potential energy in different materials and the electrons in the metal film have lower absolute potential energy than electrons in the semiconductor. This creates a flow of electrons from the semiconductor into the metal, resulting in a negatively charged metal and a depletion layer in the semiconductor adjacent to the interface. The basic difference, compared to *pn*-junction diodes, is the lack of holes (i.e. minority carriers) in the process. The carrier flow in the Schottky diode is entirely constituted by electrons.

The advantage of this type of diode is the low on-state voltage, which can be as low as 0.3 V, making it appropriate for some power applications where relatively low breakdown voltage (100-200V) is acceptable.

3.2 Bipolar Junction Transistors (BJTs)

Basic structure and i-v characteristics

Like other power semiconductors, the capability of sustaining high current levels and high blocking voltages demands a different internal structure of the device compared to signal level devices. The structure of a *npn* BJT, the type most widely used, is found in Figure 3.4 along with the circuit symbol. For the *pnp* transistor, the opposite type of doping and reference direction of currents and voltages are used.
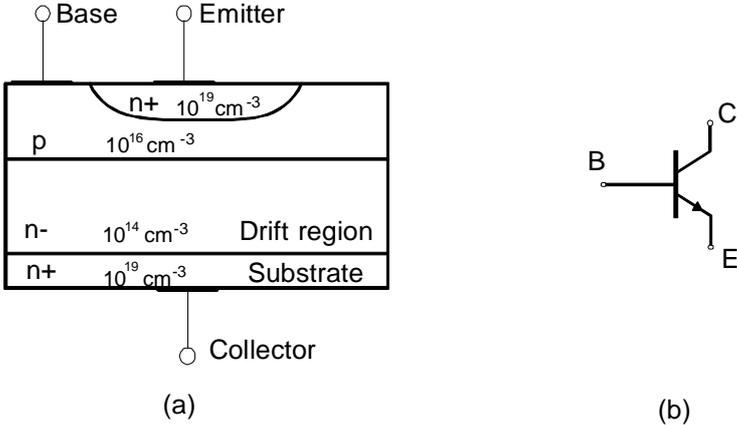
Figure 3.4 a) Vertical structure of *npn* BJT with typical doping densities and b) circuit symbol

The vertical structure, with a large cross-sectional area, gives the advantage of lower on-state resistance as well as a low thermal resistance, which minimise the power dissipation in the transistor. In addition, a narrow base results in good amplification capabilities, although, a too narrow base compromises the breakdown voltage capability. In reality, the numerous bases and emitters on a chip is designed like narrow, interleaved fingers to avoid current crowding (explained later) and parasitic ohmic resistance.

The current gain, $\beta = I_C / I_B$, for a common BJT is quite low, typically 5-10, and is not enough for most power applications. To enhance its performance, a monolithic (i.e. grown on the same wafer) Darlington connection is used, see Figure 3.5.
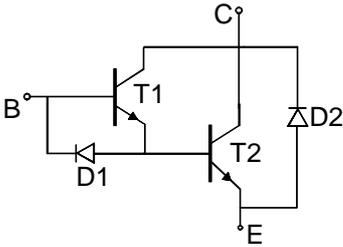
Figure 3.5 Darlington connection where $\beta = \beta_{T1} \beta_{T2} + \beta_{T1} + \beta_{T2}$. D1 is added to aid turn-off and D2 for full bridge applications.

The *i-v* characteristic of a BJT is illustrated in Figure 3.6. The characteristic is similar to the one of the logic level transistor, except for the quasi-saturation region, which depends on the lightly doped collector drift region in the BJT.
One feature of the characteristic of the BJT is the maximum sustainable collector-emitter voltage at high collector currents, BV_{SUS}. With the base open, even higher voltage can be sustained, BV_{CEO}. This voltage is often considered as the transistor's stand-off capability since the transistor mostly experiences high voltages only at zero base current when the BJT operates in cut-off. Less practical sense has BV_{CBO}, the collector-base voltage at open emitter circuit.
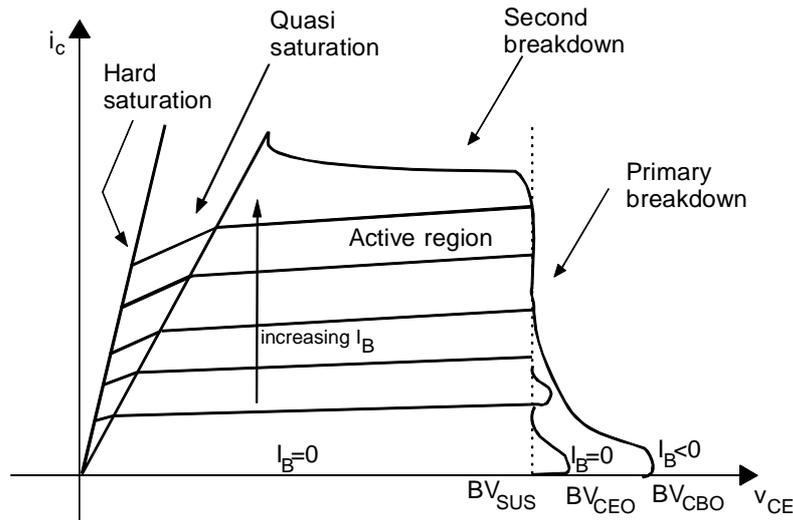
Figure 3.6 The *i-v* characteristics of a BJT.

Gain mechanism

During operation in the *active region*, the collector drift region has little influence on the operation and the analyses of carrier transport and distributions can be simplified by neglecting the drift region.

In the active region, electrons are injected from the emitter into the base, and holes from the base into the emitter because the base-emitter (B-E) junction is forward biased. The collector-base (C-B) junction is reversed biased, hence, thermally generated holes are swept out from the depletion region, adjacent to the junction, into the base and electrons are swept out from the base into the collector. This establishes a minority carrier distribution with a high gradient, like in Figure 3.7b, which supports a considerable diffusion current.
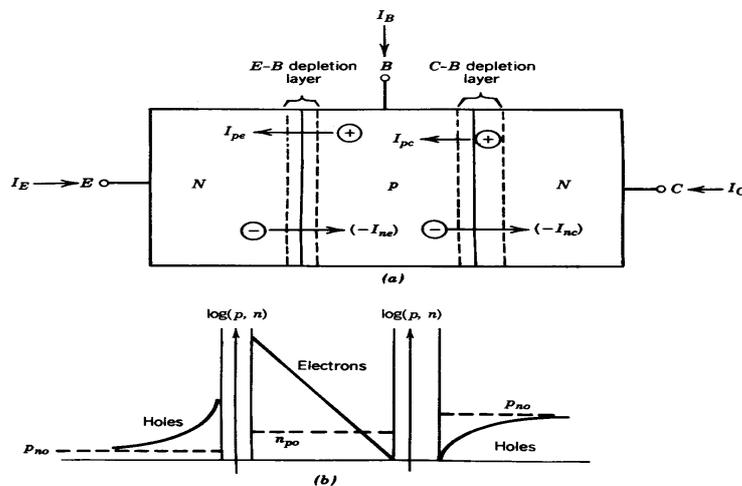
Figure 3.7 a) Carrier transport in a simplified model of the BJT and b) stored charge distribution in the normal active region [20].

The base current, entering the base from the B-E junction, is not equal to the current leaving the emitter on the *n*-type side of the B-E junction, because of the alternative way for electrons to exit the base via the collector. There are three reasons for this:

● The diffusion length of the electrons is longer than the width of the base, hence, few electrons recombine before they reach the collector.

● The diffusion current through the base carries most of the electrons to the edge of the space charge region where the strong electrical field, caused by the reverse biased C-E junction, quickly sweeps them into the collector.

● The relatively large area of the collector yields a high possibility for the electrons to reach the collector.

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In summary, this implies that the collector current is considerably higher than the base current, and therefore, is approximately equal to the emitter current. The much lower base current causing a high collector current gives rise to the gain mechanism of the BJT.

The main factors for a high gain, β, are; heavy doping of the emitter, long minority-carrier lifetime and a narrow base, however, these factors also affects other properties of the transistor and a compromise is often necessary.

Moreover, there are two specific factors causing a drop in β at high current levels - conductivity modulation and current crowding.

The decrease caused by the conductivity modulation occurs at levels of the minority carrier doping density equal to the majority carrier doping density. This is due to the fact that the base current increases to supply excess holes at the same rate as excess electrons, in order to support the neutrality of space charge. The increase in base current occurs without a corresponding increase in collector current, hence, β drops simultaneously.

At *current crowding,* a non-uniform current density in the emitter occurs, owing to the lateral voltage drop caused by the lateral base current, like in Figure 3.8. The lateral voltage drop increases with the length of the (lateral) current path and subtracts from the externally applied B-E voltage. Consequently, the B-E junction voltage, and therefore also the current density, is highest at the periphery of the emitter. This leads to a lower limit of the current, causing the decrease in β, than would have been the case with an evenly distributed current density. This problem can be minimised by designing a large total emitter area, constituted by thousands of small emitter cells with a small lateral width, thus, avoiding a non-uniformly distributed current density.
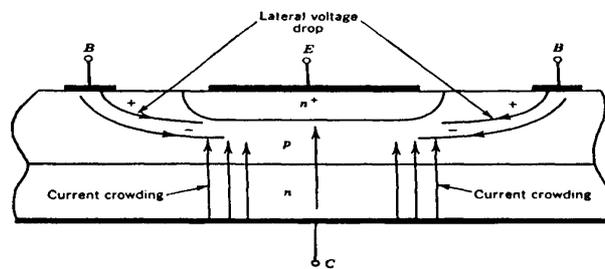
Figure 3.8 Emitter current crowding in forward bias [20].

Quasi saturation

If the base current is allowed to increase, the consequence is an increased collector current and a lower collector-emitter voltage because of the higher load voltage. Also the base-collector (reverse-) voltage decreases when the ohmic voltage drop in the drift region increases with increasing collector current ($v_{BE} + v_{BC} = v_{CE}$). Finally, the B-C junction becomes forward biased and the quasi-saturation region is entered. In this region, the effects of the collector drift region cannot be neglected anymore and has to be included in the BJT model.

When the B-C junction is forward biased, holes are injected into the collector from the base. To sustain space charge neutrality also electrons must be supplied, which is principally done via the injection of electrons from the emitter and the subsequent drift across the base. As the stored excess charge increases, the drift region is shorted out and the voltage drop reduces. Furthermore, as the virtual base expands into the collector, β reduces in addition with the collector current.

Switching characteristics

To investigate the switching characteristics, the BJT is assumed to be embedded in a diode-clamped circuit, as in Figure 3.9. Furthermore, it is assumed that the freewheeling diode is ideal and the load inductive with a constant load current, I_0. The load current, in addition with the lifetime of the minority carriers, determines the amount of stored charge required for the BJT to operate in hard saturation.
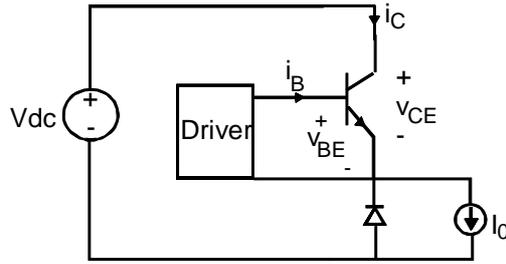
Figure 3.9 Inductively loaded BJT switching circuit with a diode clamp.

Turn-on

During turn-on of the BJT, four different time intervals can be distinguished in Figure 3.10.

The first interval, $t_{d(on)}$, is called the turn-on delay time according to the charging time of the B-E space charge capacitance, where the depletion region of the B-E junction first must be removed before the junction can be forward biased and carrier injection can commence. During the current rise time, t_{ri}, the collector current starts increasing owing to the carrier injection. However, the freewheeling diode is still conducting, therefore, the collector-emitter voltage is still unchanged and the BJT is in the active region.

The voltage fall time can be divided into two intervals, t_{fv1} and t_{fv2}. At t_{fv1}, the entire load current has commutated to the BJT, the diode is reversed biased and the collector-emitter voltage starts to fall. At the beginning of the second interval, t_{fv2}, the BJT enters quasi-saturation and the voltage fall time reduces as a consequence of the decreased current gain. After t_{fv2}, the BJT stays in hard saturation.
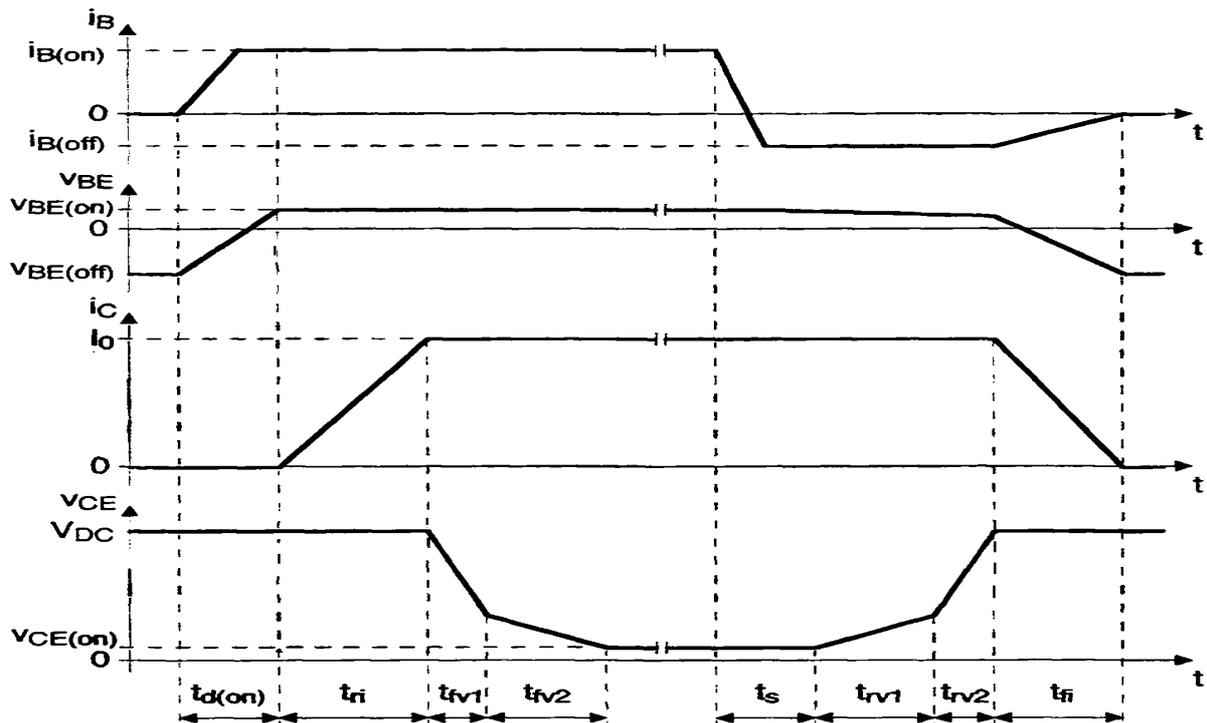
Figure 3.10 Switching period of BJT [22].

Turn-off

Turning off the BJT engages the issue of stored charge removal. The recombination process alone is a rather slow process, hence, a negative base current for carrier sweep out is required. The application of the negative base current can be performed with either a step function or a ramp function with a controlled di_B/dt. In spite of the importance of a fast charge removal, it is shown that the latter function is the most favourable one and the analysis commences with the gradually changing base current.

<u>Storage time</u>, t_s: Only the base current is changed and removes the stored charge, necessary for keeping the transistor in hard saturation.

<u>Voltage rise time</u>, t_{rv}: Divided into two intervals similar to the reverse of the turn-on process. The collector-emitter voltage rises but the freewheeling diode is reversed biased and cannot carry any of the load current.

<u>Current fall time</u>, t_{fi}: The collector-emitter voltage has reached the off-state value, thus, forward biasing the freewheeling diode. The collector current falls to zero as the remaining charge is removed. The B-E space charge capacitance acquires a negative charge as v_{BE} goes negative.

If an abrupt function of the base current is applied, the intervals t_s and t_{rv} are shorter and more stored charge is removed from the *base region*. Still, the majority of charge is stored in the drift region and is substantially removed by the collector current, not the base current. Consequently, the step function reverse biases the B-E junction, hence, disables the gain mechanism of the BJT, at an earlier stage compared to case with the ramp function. After the emitter current is turned off, the only way of removing remaining charge is by recombination and by carrier sweep out of the collector current, now equal to the negative base current (not multiplied by β as before). These slower processes cause a "current tail", which may contribute to higher switching losses.

Second breakdown

A common reason for device failure for bipolar semiconductors is termed second breakdown. This occurs at high current levels where the collector-emitter voltage suddenly decreases, followed by a large increase of the collector current. This leads to high power dissipation, often appearing locally in the transistor, and if this state not is terminated quickly, breakdown of the device occurs.

The cause of the breakdown is not impact ionisation and avalanche breakdown (as in primary breakdown), but a phenomenon referred to as *thermal runaway*. Bipolar devices all have a negative temperature coefficient of resistivity (the resistivity decreases with increasing temperature), furthermore, as the temperature rises the thermal generation of electron-hole pairs increases, contributing to even higher current levels. Consequently, if the power dissipated in the transistor is higher than what can be removed, the temperature increases, which in turn increases the dissipated power further and a loop of positive feedback is initiated.

Safe Operating Area (SOA)

A way of visualising the rated current and voltage limits is the Safe Operating Area, like in Figure 3.11.
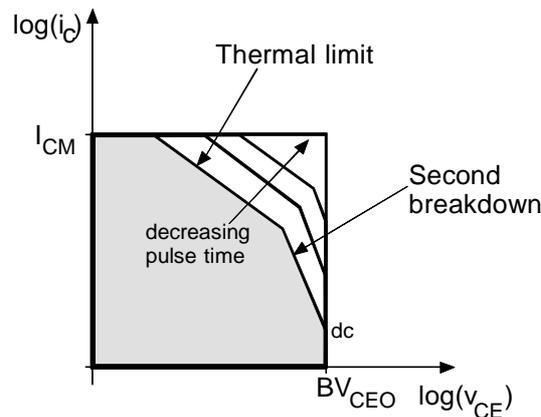

Figure 3.11. Safe Operating Area for the BJT.

I_{CM} is the highest collector current allowed, even for pulsed applications, and is limited by the bond wires and wafer metalisation. The thermal limit is given by the thermal resistivity and the maximum allowed junction temperature.

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3.3 Metal Oxide Semiconductor Field Effect Transistors (MOSFETs)

The MOSFET was introduced 20 years ago, as a compliment to the BJT, in applications with high switching frequencies. The on-state voltage is higher but the switching times considerably shorter for the MOSFET compared to the BJT. The internal processes of the MOSFET are significantly different from those in the BJT and are discussed in this section.

Basic structure

The vertically diffused MOSFET (VDMOS) is the most common MOSFET and consists of four different layers like in Figure 3.12a. In reality the transistor is constituted by thousands of cells, like the one in the figure, connected in parallel.
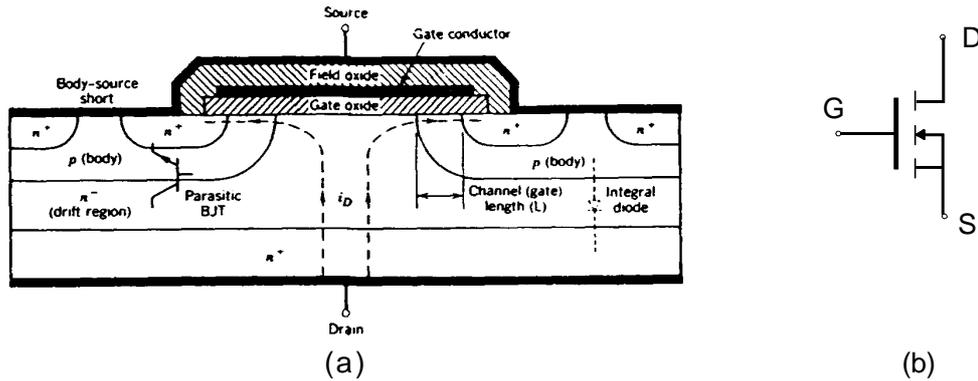
Figure 3.12 a) Vertical structure of *n*-channel MOSFET. The thickness of the layers is not according to scale [20] b) circuit symbol.

If the source and drain regions are of *n*-type doping, the MOSFET is said to be an *n*-channel MOSFET, and with a *p*-type doping, a *p*-channel MOSFET. With a voltage applied between the source and drain, there is always one reverse biased *pn*-junction, independent of the polarity of the voltage. Although this means there can be no minority carrier injection, an applied gate-source voltage affects carriers in the body region and creates a lateral channel, connecting the source to the drain. The channel is formed in the body region, which has an opposite doping compared to the other layers, hence, the channel is formed by an inversion layer (electrons in an *n*-channel MOSFET).

The gate is surrounded by a layer of silicon dioxide, which serves as an insulator, and the gate metalisation covers the drift region for two reasons. First, it enhances the conductivity of the drift region by establishing an accumulation layer under the gate oxie during on-state. Second, it acts like a field plate during blocking state, expanding the radius of the depletion layer, hence, minimising the maximum electrical field and thereby increases the breakdown voltage.

The doping structure of the MOSFET also includes a parasitic *npn* BJT (Figure 3.12a), which must not be triggered during operation. Owing to the disability of controlling the base of the parasitic BJT (body region of MOSFET), its operation cannot be turned off and the body of the MOSFET is therefore shortened to the source by the source metalisation to avoid turn-on. The short-circuit of the parasitic BJT results in a parasitic freewheeling diode which can be used in bridge applications.

i-v characteristics

Like the BJT, the MOSFET is also a three-terminal device, Figure 3.12b, where the gate serves as the input, the drain as output and the source is usually common to both in- and output. The gate-source voltage controls the output current, as is illustrated in the output characteristics in Figure 3.13a, where the drain current, i_D, is plotted versus the drain-source voltage, v_{DS}, for different values of the gate-source voltage, v_{GS}.

During turn-on, the MOSFET traverses the characteristics from cut-off through the active region and finally into the ohmic region, and back again during turn-off.

In cut-off, v_{GS} is less than the threshold voltage, $v_{GS\ (th)}$, and the transistor must withstand the applied power supply voltage. To avoid avalanche breakdown, the applied voltage must be less than the breakdown voltage, BV_{DSS}.

When the gate-source voltage exceeds the threshold voltage, the MOSFET enters the active region. The drain current becomes independent of the drain-source voltage and is controlled only by the gate-source voltage. The current is sometimes said to be "saturated" in the active region, not to be confused by the saturation region of the BJT.
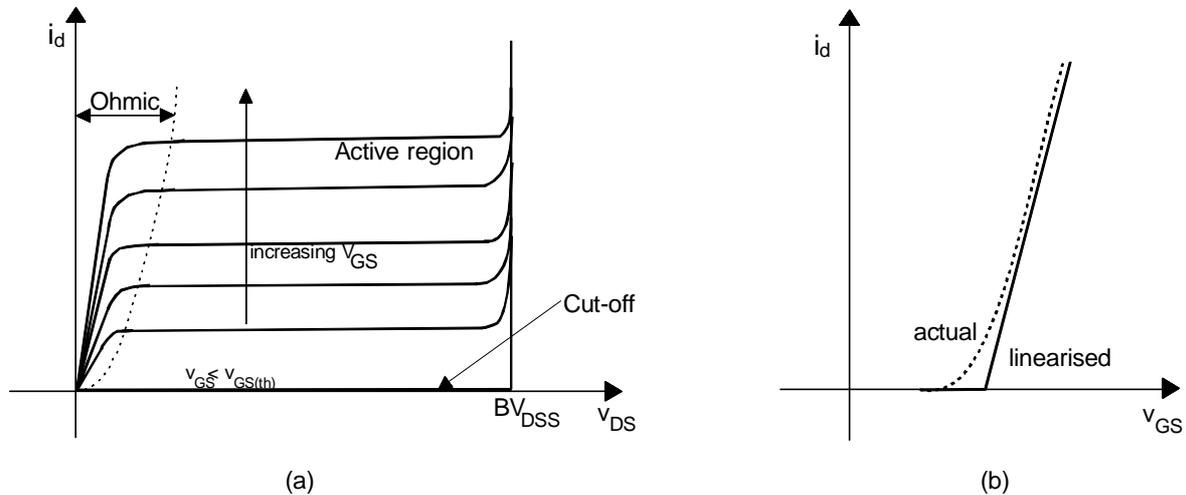

Figure 3.13 a) *i-v* characteristics and b) transfer function of the MOSFET.

In Figure 3.13a, the boundary between the active and ohmic region is determined by $v_{DS} = v_{GS} - v_{GS\,(th)}$. When a high gate-source voltage is applied, the drain current does not saturate and the conduction losses can be kept relatively low by minimising the on state voltage, $v_{DS\,(on)}$ (i.e. the ohmic drop of the drift region).

Inversion layer and field effect

The area of and underneath the gate actually forms a capacitor, with the gate metalisation and the body region as the electrodes and the silicon oxide as the dielectric. When a positive voltage is supplied across the gate-source terminals, an equally large charge is formed in the gate (positive charge) as in the body (negative charge), adjacent to the gate oxide. For low voltages, the positive charge on the gate side repells the holes near the interface, creating a depletion layer with negative charge of ionised acceptors in the (*p*)body region (Figure 3.14a). As the gate-source voltage increases, free electrons are attracted to this layer by the electric field, and more holes are depleted further into the body where they are neutralised by electrons from the n^+ source (Figure 3.14b). The free electrons are substantially produced by thermal generation of electron-hole pairs.

If the gate-source voltage is made as high as the threshold voltage, $v_{GS\,(th)}$, the density of free electrons is equal to the density of free holes in the bulk of the body and the electrons form an *inversion layer* (Figure 3.14c). This inversion layer acts like a channel connecting the source to the drain and allows a current to flow. The ability to modulate the conductivity of the body region beneath the gate oxide is called the *field effect* (hence MOS*FET*).

The thickness of the depletion layer grows with increasing gate-source voltage. Yet, once the inversion layer is established, it "screens" the depletion layer from the electrical field and ceases the growth. The increasing bias will instead increase the density of free electrons and the conductivity of the channel.

The drain current levels off when entering the active region from the ohmic region in Figure 3.13a, and this can be attributed to a vertical voltage drop over the channel owing to the resistance of the channel. As the drain current through the channel increases, the voltage drop over the channel increases simultaneously. If a constant gate-source voltage is assumed, the oxide voltage will then decrease ($v_{oxd}=v_{GS}-v_{channel}$), producing a non-uniformly distributed inversion layer. The decreasing inversion layer at the drain end of the channel results in an increasing resistivity and higher drain-source voltage drop, which causes the curve in the *i-v* characteristics to level off.
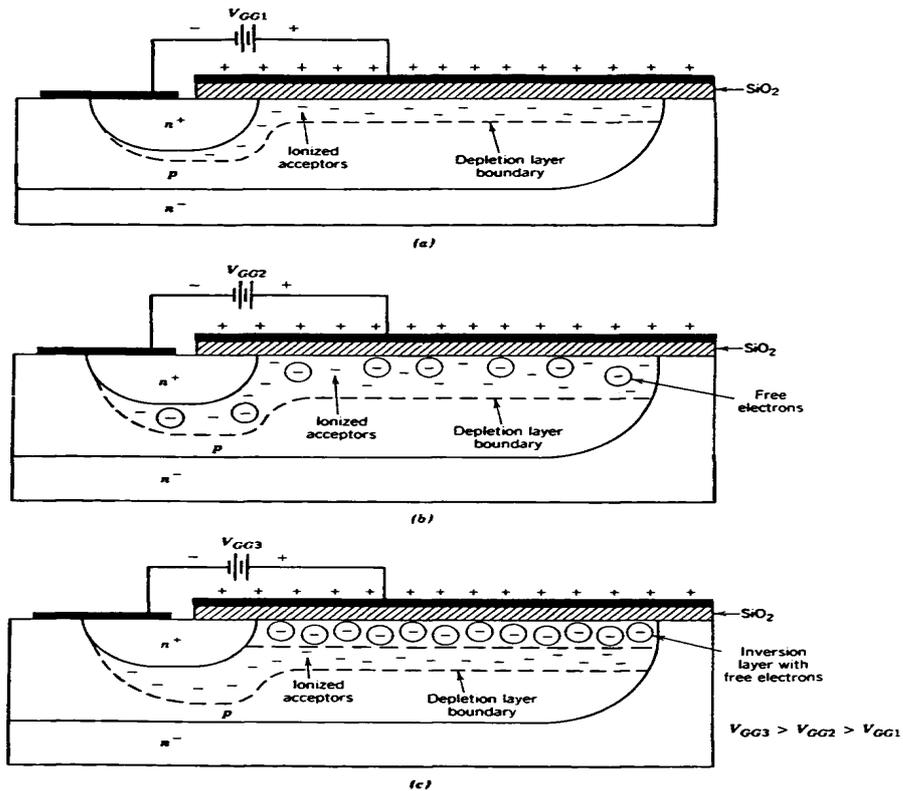
Figure 3.14 Formation of the a) depletion layer and b) c) inversion layer, as the gate-source voltage is increased [20].

Switching characteristics

The significantly shorter switching times for the MOSFET, compared to the BJT, are due to the reduction of stored charge that has to be removed or supplied. The only charge that must be transported is stored in the stray and depletion layer capacitances, which are included in the equivalent circuit in Figure 3.15a.

The drain current, during operation in the active region, is modelled by a current source, $i_D = g_m(v_{GS} - v_{GS\ (th)})$, where g_m is the transconductance. In the ohmic region, the voltage drop over the drift region is modelled by a resistance, $r_{DS(on)}$, and is used for calculating the conduction losses.

Because of the dependence of the depletion region thickness, neither the gate-drain capacitance, C_{gd}, nor the gate-source capacitance, C_{gs}, is constant. The variation of C_{gs} is however small and C_{gs} is considered to be constant, where as C_{gd} may vary by a factor 10 to 100 as the drain-source voltage changes (Figure 3.15c).
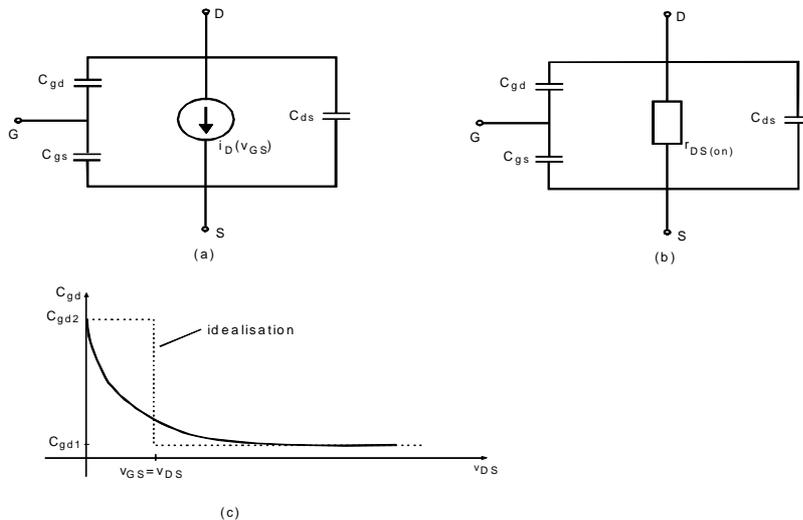
Figure 3.15 Equivalent circuits of MOSFET for transient analysis a) in cut-off and active region b) in ohmic region and c) the variation of gate-drain capacitance with drain-source voltage.

Like at the analysis of the BJT, the same inductively clamped step-down converter is assumed (Figure 3.9), with the addition of a gate resistance between the MOSFET and the gate drive. The switching transients are shown in Figure 3.16, with the turn-on first followed by the turn-off.
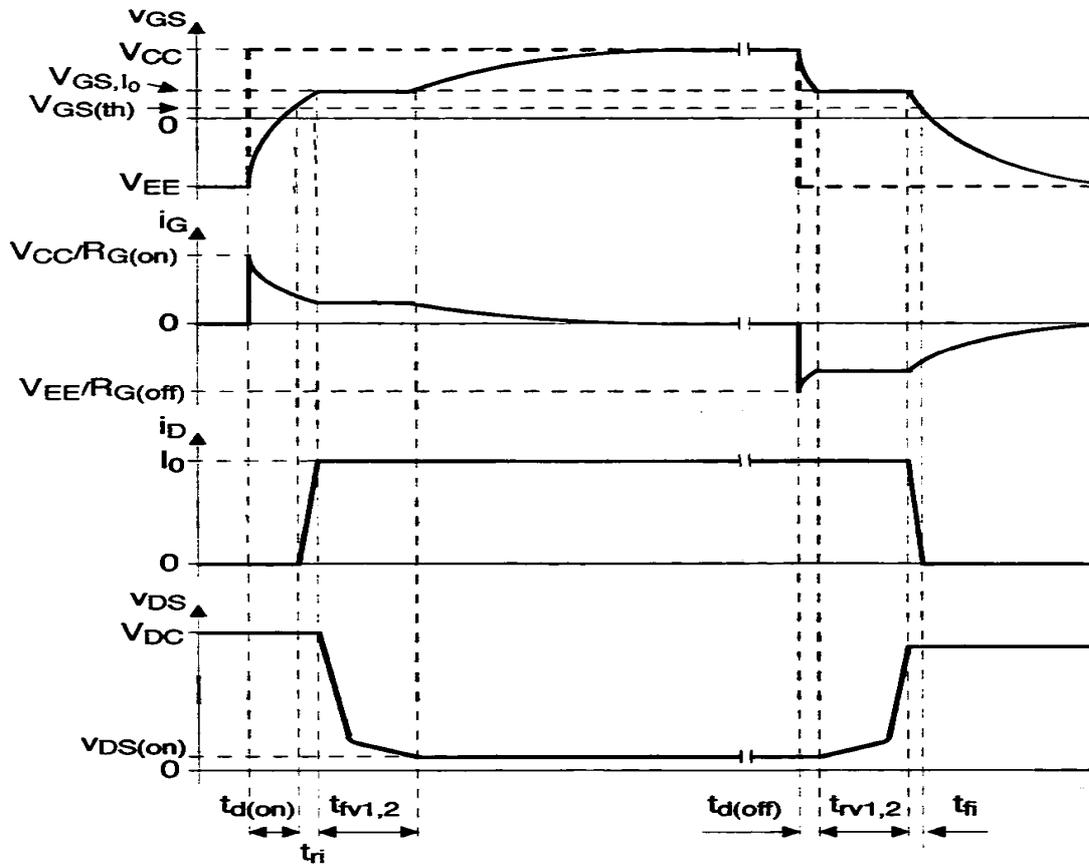
Figure 3.16 Switching transients for the MOSFET [22].

Turn-on

Turn-on delay time, $t_{d(on)}$: The gate drive is assumed to be a step function and the gate-source voltage increases from zero to the threshold voltage. Only the gate-source and the gate-drain voltage, not the drain-source voltage, are affected, hence, the gate-drain and gate-source capacitances appear in parallel to the gate and the gate resistor, R_G. The time constant is then equal to $R_G \cdot (C_{gs} + C_{gd1})$, but, as $t_{d(on)}$ is significantly shorter, the gate-source voltage appears to be linear during this interval.

Current rise time, t_{ri}: When the threshold voltage, $v_{GS\,(th)}$, is reached, the current transfers to the MOSFET and when the complete load current is carried by the MOSFET, the freewheeling diode is reverse biased and the drain-source voltage begins to fall.

Voltage fall time, t_{fv}: The gate-source voltage is clamped to the voltage corresponding to I_0 in the transfer characteristics (Figure 3.13b). In order to decrease the drain-source voltage, the entire gate current flows through the gate-drain capacitance to recharge it. The interval can be separated in two. During the first, the depletion region is reduced and C_{gd} holds its lowest value, C_{gd1}. During the second interval, the ohmic region is reached and C_{gd} holds its highest value, $C_{gd2.}$

Finally, when the on-state voltage, $v_{DS\,(on)}$, is reached, the gate-source voltage clamp is released and the voltage starts to rise towards the gate drive limit with a time constant equal to $R_G \cdot (C_{gs} + C_{gd2})$.

Turn-off

The sequence during turn-off is essentially the reverse of the turn-on process.

Turn-off delay time, $t_{d(off)}$: The gate-source voltage falls to the voltage level determined by the drain current, I_0, in the transfer function.

Voltage rise time, t_{rv}: The drain current is clamped to I_0 and the entire gate current flows through the gate-drain capacitance, recharging it. The rise time of the drain-source voltage depends on whether the transistor operates in the ohmic region ($v_{DS} < v_{GS}$ during t_{rv1}), or the active region ($v_{DS} > v_{GS}$ during t_{rv2}). The gate-drain capacitance changes gradually during these two consecutive intervals, from the maximum value, C_{gd2}, to the minimum value,

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C_{gd1}. Once the collector-emitter voltage has reached its final off-state value, the freewheeling diode becomes forward biased and the load current commutates from the transistor to the diode.

Current fall time, t_{fi}: The declination of the drain current is determined by the declination of the gate-source voltage and as the drain current reaches zero the gate-source voltage have reduced to the threshold voltage. The gate current rises with a time constant proportional to the gate resistance and the sum of the gate-drain and gate-source capacitances.

Unlike the BJT, the switching losses for the MOSFET are almost temperature independent, owing to the nearly constant values of the capacitances. However, the conduction losses may vary, according to the variation of the drift region resistance with the junction temperature.

Conduction losses and breakdown voltages

The major losses of a MOSFET are constituted by conduction losses, opposed to the BJT where the switching times and losses are considerably higher. On one hand, the lack of conductivity modulation in the MOSFET causes higher on-state losses, on the other hand, the switching times are kept short. The drift region, with its low doping density and long length (in current direction), is the cause of the major part of the conduction losses, especially at high breakdown voltages where the drift region must be made thick enough to sustain the applied voltage and allow the expansion of the depletion region.

Even though the parasitic BJT is shorted, it can be triggered by high derivatives of the drain-source voltage at turn-on. This condition is referred to as *latch-up* and can be avoided by following the value of the gate resistor specified by the manufacturer.

Safe operating Area (SOA)

The SOA for a MOSFET is for most switching applications virtually rectangular, limited by the maximum drain current, I_{DM}, the breakdown voltage, BV_{DSS}, and the maximum allowed junction temperature, T_j. Often a limit of 20-30 V is set for the maximum gate-source voltage, even though it may sustain up to 100V, depending on the thickness of the gate oxide.

3.4 Insulated Gate Bipolar Transistors (IGBTs)

The IGBT was developed to take advantage of the short switching times and low switching losses of the MOSFET and the high breakdown voltage and low conduction losses of the BJT. The IGBT is also referred to as GEMFET or COMFET owing to its structural resemblance to the MOSFET, as can be seen in Figure 3.17a.

The difference from the MOSFET is the additional, heavily doped p^+ layer at the drain end of the IGBT, which forms a *pn*-junction (junction J_1) and facilitates the minority carrier injection into the drain region.
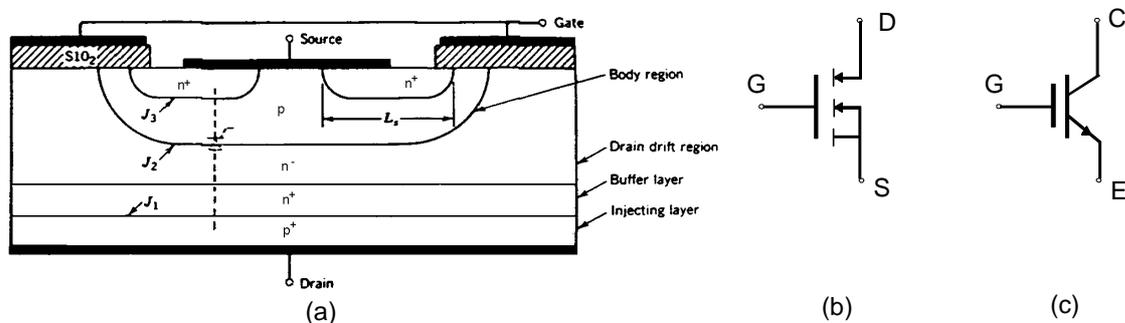

Figure 3.17 a) Vertical cross section of the IGBT [20] and b) c) circuit symbols

The IGBT illustrated in Figure 3.17a, is of a punch-through type, PT-IGBT, because of the way the depletion region reaches entirely through the drift region at high blocking voltages. If the IGBT lacks the n^+ buffer layer, it

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is referred to as a non-punch-through (NPT-) IGBT, and the width of the drift region must be approximately twice as thick as for a PT-IGBT for the same blocking voltage.

The parasitic thyristor is due to the injecting layer and to avoid turn-on, the geometry of the junctions J_2 and J_3 is in reality a bit more complex than in Figure 3.17a.

Two different circuit symbols are shown in Figure 3.17 b and c, since there still is some disagreement about the standard symbol, however, the symbol in Figure 3.17 c is the most common seen and is basically viewed as a BJT with a MOSFET gate input.

The *i-v* characteristics of an *n*-channel IGBT are very similar to the one for the MOSFET (Figure 3.13a). In the forward direction, the junction labelled J_2 in Figure 3.17a, blocks the forward voltage and the junction J_1 the reverse voltage. However, in PT-IGBTs, the doping densities of the surrounding layers are sufficiently high to lower the reverse blocking capability to only a few tens of volts, which in most power applications can be considered as a negligible capability.

On-state operation

As in a MOSFET, a channel is created underneath the gate when the applied gate voltage exceeds the threshold voltage. The electrons flowing through this inversion layer attract holes from the drain and the holes flow towards the body region by both drift and diffusion, where they recombine with electrons from the source. The junction J_2 acts like a collector of a *pnp* BJT, collecting the diffusing holes, and the IGBT can therefore be described by a Darlington circuit, Figure 3.18a. The ohmic drift region is modelled by a resistance, R_{drift}, and most of the drain current is carried by the MOSFET. A more detailed model is used in Figure 3.18b where also the parasitic thyristor is included.
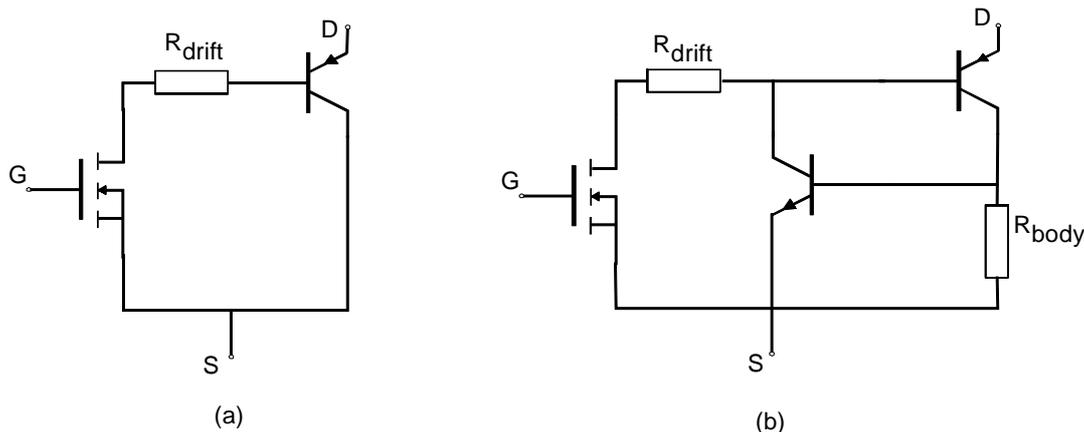
Figure 3.18 a) Darlington circuit of IGBT b) including parasitic thyristor.

Switching characteristics

The same circuit conditions (step-down converter with freewheeling diode) as for the MOSFET and the BJT are assumed for the IGBT and the same equivalent circuit can be used (with C_{gs}, C_{gd} and C_{ds}). Most of the transient operation, illustrated in Figure 3.19, is identical to that of the MOSFET.

Turn-on transient
Similar to the MOSFET transient with a difference in interval t_{fv2}, where the gate-drain capacitance increases to its higher value and the MOSFET has reached its ohmic region. However, the BJT part of the IGBT has not reached hard saturation yet and the conductivity modulation is therefore not fully developed. This conductivity modulation lag causes a slower voltage drop of the drain-source voltage and the increased switching losses is referred to as forward recovery.

Turn-off transient
The sequence differs from that of the MOSFET in interval t_{fi}, where the drain current experiences a long "tail" current. During the first interval, t_{fi1}, the drain current drops rapidly in agreement with the MOSFET transient. In the next interval, the MOSFET channel is turned off and the only way for the stored charge in the drift region to

reduce is by recombination. Short lifetime of the excess carriers gives shorter tailing time, however, will also lead to higher conduction losses during on-state.

In PT devices the buffer layer serves as a sink for the holes where the recombination is a faster process owing to the design of shorter lifetime in the buffer layer. In the case of NPT-IGBTs, the switching losses are minimised by keeping the amplitude of the current during the tailing time as low as possible. This is achieved if the MOSFET part of the current is designed to carry the major part of the drain current, which in newer devices is approximately 90%.
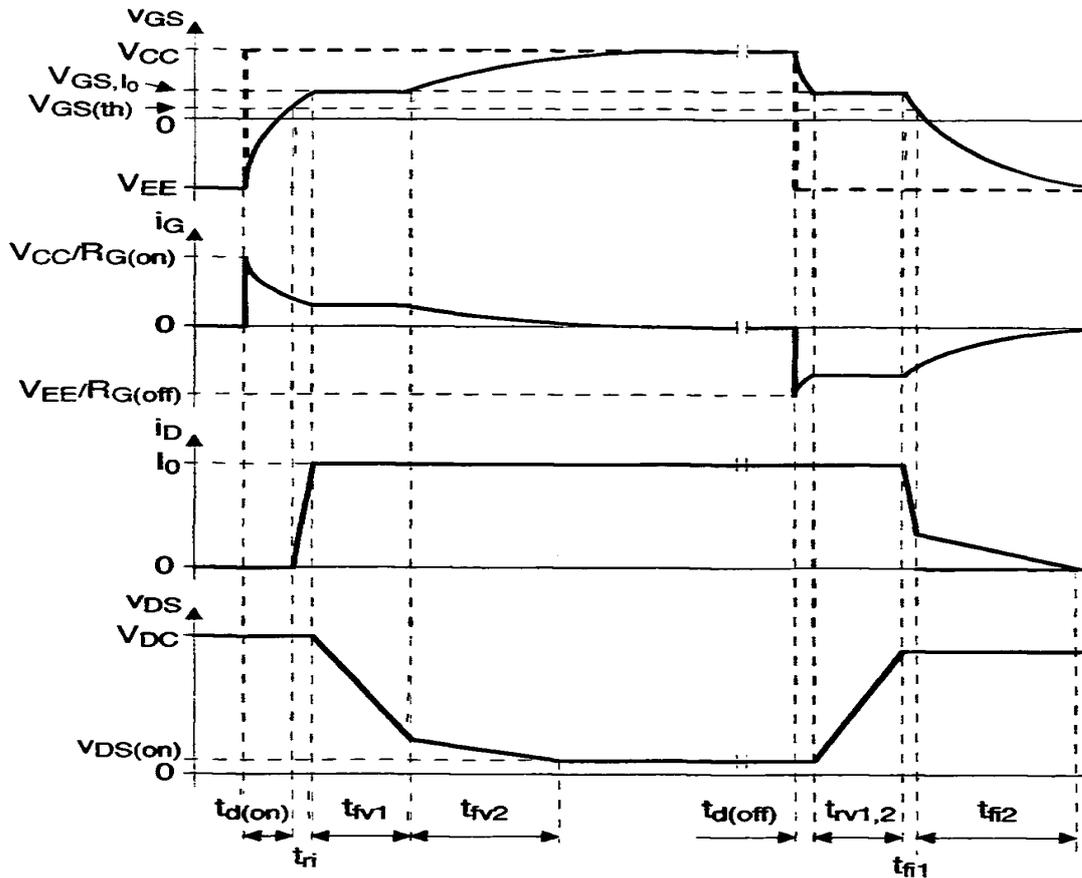
Figure 3.19 Switching transient of the IGBT [22].

Latchup

The state where the parasitic thyristor is turned on is named latchup. This state is crucial and must be avoided or turned off quickly. The problem is that the thyristor is not possible to turn off from the gate, it has to be turned off by forcing the drain current to commutate.

Latchup is separated into static and dynamic latchup. The current limit for static latchup is usually higher than for dynamic latchup. This is according to the rapid expansion of the depletion region at turn-off of the MOSFET part. This enhances the base transport factor of the BJT, which means that holes are more likely to reach the collector without recombining. Consequently, for a specified on-state current, a higher hole current and ohmic drop, hence, lower current limit, will occur during dynamic latchup than static latchup. To avoid latchup, an optimised gate resistance, always specified by manufacturers, should be applied, which keeps the MOSFET channel open until a sufficient amount of excess carriers have recombined.

Safe operating Area

The most important limits in the SOA are the maximum drain current, I_{DM}, to avoid latchup, the maximum gate voltage $v_{GS\ (max)}$ and the breakdown voltage of the drift-body junction, BV_{CBO}. The gate voltage limit is set to make the IGBT withstand currents ten times higher than the rated current under approximately 10 μs (short circuit conditions).

The IGBT is usually designed to have a maximum junction temperature of 150° C and to have conduction losses independent of the temperature. This is possible because the internal MOSFET has a positive coefficient of temperature and the internal BJT a negative. However, for applications with parallel IGBTs, the IGBTs are designed to have a slightly positive coefficient of temperature.

The Reverse Bias Safe Operating Area, RBSOA differs from other semiconductors because latchup must be avoided and the reapplied rate of change of the drain-source voltage limited. Hence, the cut off corner in Figure 3.20b.

Figure 3.20 a) FBSOA and b) RBSOA

4 IGBT models

Although the area of developing power semiconductor models for circuit simulators has won more interest from research groups and software vendors in recent years, there still is a gap between the development of the actual semiconductors and the development of commercially available simulator models of the devices.

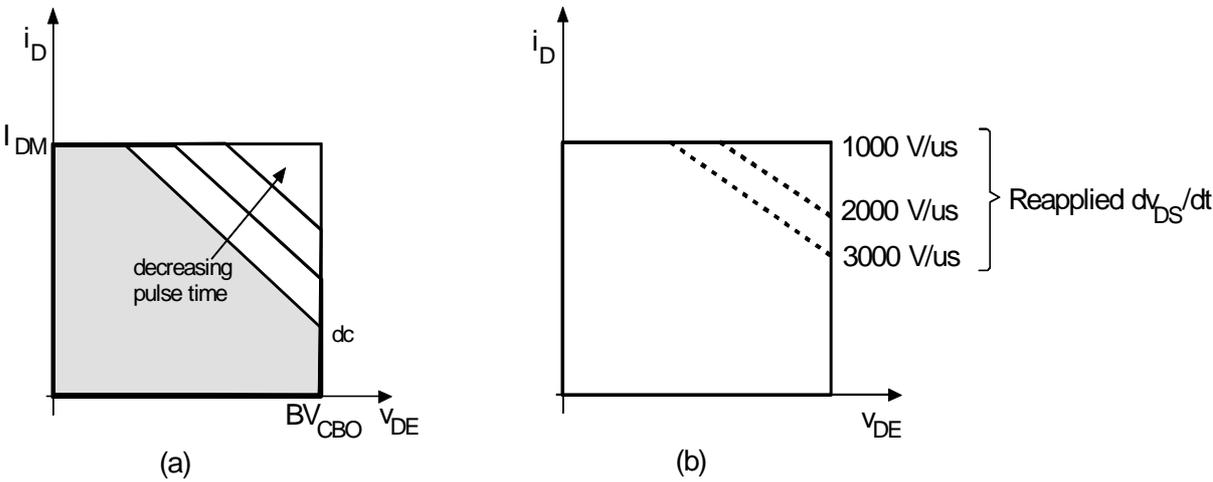When modelling IGBTs, there is always a trade-off between accuracy and simplicity of the model. High accuracy is often accomplished only at the cost of computing speed, the portability between different circuit simulators or complex parameter extraction.

There are certainly a variety of different approaches when modelling IGBTs; hence, each model has its own features, trying to emulate the reality. It is therefore essential for circuit designers to focus on the purpose of the simulations and based on this, together with available resources, make the appropriate choice of model. Additionally, regardless of model, the parameter extraction is of greatest importance and the number of parameters and the extraction procedure are also to be considered before choosing model.

4.1 IGBT model categories

As mentioned earlier the different design aspects of a model strongly depends upon the purpose of the model. Most models are manufactured for investigating device behaviour in circuit simulations but there are also some for understanding the internal physics and mechanisms and for structure optimisation.

Both static and dynamic characteristics must be well described, however, depending on the designer's philosophy this can be done viewing the device from the outside, as a "black-box", or from the inside, trying to emulate the internal physics.

Independent of design strategy, an accurate model must be able to model some basic features of the semiconductor. In [1] there are given five "basic physical phenomena" for semiconductor devices, and for the IGBT, all five (Resistivity modulation, Charge storage, MOS-capacitance, Electrothermal behaviour and Breakdown limits) are stated to be "very important" or at least "to be included".

The majority of vertical IGBT models published since 1985 is reviewed and also categorised in [2].

In this chapter, a summary of these categories is given, including reviews of different models with respect to the background of this thesis. Although the literary study included almost 70 articles, only a few reviews are given in each section.

A. Behavioural models

The behavioural models are also called "functional" or "empirical" models because this category does not consider the internal physics of the IGBT. The device is instead viewed as a "black-box" and the external characteristics is described with curve fitting algorithms or look-up tables. The DC-characteristics can often be well modelled, yet, the transient behaviour is more complex and difficult to model on account of the interactions with the other elements in the circuit during switching.

A model constituted by both a linear (dynamic) and a non-linear (static) block, the Hammerstein configuration, is developed in [15] and [16]. The performance is stated to be as good as the physics-based model [17] and it is implemented in the SABER circuit simulator.

B. Semimathematical models

The second group of models consists of parts based on physics as well as existing circuit devices. A common configuration is the Darlington-circuit where a MOSFET serves as a driver device and the *pnp* as the main transistor. Other parts are used to account for some specific IGBT effects, like base conductivity modulation, Non-Quasi-Static effects and non-linear capacitances.

These models are generally not as accurate as mathematical models since none of the existing built-in BJTs are comparable with the internal, wide-base BJT of the IGBT. Nevertheless, the advantages of this category are the simplicity and the possibility of implementation in any circuit simulator.

A method called "the lumped-charge approach" is used by [12] and [13]. The purpose of the latter model is to provide an accurate model with easy parameter extraction (both from experimental set-ups and data sheets) and also to be available in the public domain. Although the parameter extraction is easier compared to Hefner [3-8], it is not described in detail and the model is only validated for PT-IGBTs and for low voltage applications. Also [12] utilises much of the parameter extraction developed by Hefner and it is stated that the new model yields

more accurate results compared to the existing PSPICE model [14], at least for blocking voltages ranging from kilovolts and up.

C. Mathematical models

Based on semiconductor physics, this group of models tries to solve the device equations in an analytical way. The complexity of he model is dependent on how well the model tries to emulate the internal physics and how many features of the IGBT that is considered. The diffusion equation is essential to model as well as the carrier distribution, which can be modelled by a 1-D or 2-D model.

Not all models may be suitable for both circuit simulators and for IGBT structure optimisation. However there are some approximate solutions to make the model less complex and more portable; e.g. substitutions and neglecting of terms in equations and truncation of the result in (Laplace-) transformations.
One of the first accurate 1-D models was developed by Hefner [3-8] and many subsequent publications are based on his work e.g. the built-in PSPICE IGBT model [10], specifically based upon [5], [7]-[9]. The Hefner model is also the basis in [11] though extended to include 2-D effects during forward conduction, which influences the on-state characteristics, with lower conduction losses as a consequence.

D. Seminumerical models

The last category is referred to as "seminumerical" owing to the discretisation of the wide base into a finite number of elements. Another method used is to express the derivatives in the diffusion and transport equations by finite differences while other device parts are described analytically as in the first category.
Models of the seminumerical category yield most accurate results at the cost of computing speed and difficulty to implement into normal circuit simulators. This is evident in [18] where the low doped region in the bipolar transistor is realised by a hybrid model and the MOSFET part is described by a standard MOSFET model, all implemented into the SABER environment with subroutines with model equations written in FORTRAN77.

4.2 The MicroSim[a] PSPICE[a] model

As a result of the completed literary study, numerous models have been investigated with many different purposes and accomplishments. No specific model appears as the evident choice since simplicity is always compromised by accuracy. The way of implementation and choice of circuit simulator are important in deciding which model to choose and this turned out to be one of the final decisive factors. The advantages of adapting a commercially available simulator model is obvious, considering the limited time for the evaluation in this thesis, but also for aspects of e.g. convergence and computer efficiency.

In compliance with above stated factors, the choice of model falls upon the MicroSim[®] PSPICE[®] (ver. 8.0) IGBT model (further on only referred to as the PSPICE model). The basis of this decision is mainly due to two factors:

- The Hefner model [3]-[8] is the basis of the chosen PSPICE model, and since the Hefner model is implemented in several circuit simulators with sufficient accuracy, this would favour the PSPICE model.

- The fact that PSPICE is already available at ALSTOM and the model implemented and included in the symbol libraries. This entails several advantages, not only the reduction in costs and efforts, adherent to the procurement and introduction of a new product, but also the possibility of using the existing knowledge and documentation of the software.

There are also found some shortages of the PSPICE model. One is the poor accuracy at high power applications (3300V-1200A) investigated in [12], and another, that not all references could be retrieved ([9]) and the full implementation therefore not verified. Notwithstanding these drawbacks, the PSPICE model appears to be the most reasonable choice.

The PSPICE IGBT model is described by an equivalent circuit, shown in Figure 4.1. Five dc current components and six charge components describe the different fundamental physical effects of the IGBT, with the exception of a complete electrothermal behaviour. The detailed derivation of the full set of equations is not explained here; for a more comprehensive study of the underlying semiconductor physics, refer to [3]-[10].
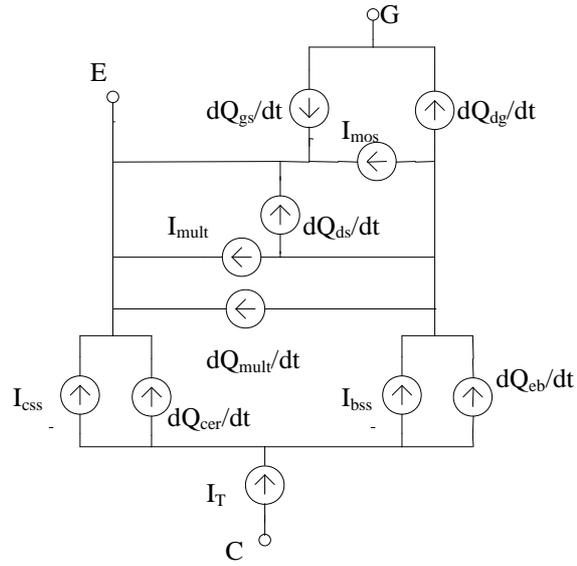
Figure 4.1 Equivalent circuit of the MicroSim® PSPICE® IGBT model.

5 Parameter extraction

5.1 Parameter extraction procedure

The parameter extraction procedure for NPT-IGBTs, developed by Hefner in [7], is adopted here, for the parameters required by the PSPICE model. The extraction procedure involves measurements of both steady-state and dynamic characteristics as well as calculations on collected data. These calculations are required to separate the characteristics of the internal MOSFET and bipolar transistor.

The required parameters, and the measurement used to extract them, are shown in table 5.1. The final parameter set, used in PSPICE, is slightly modified as explained later.

Table 5.1 The extracted parameters.

Parameter	Unit	Parameter name	Measurement used for extraction (measurement #)
A	m^2	Area (active) of the device	Visual inspection of decapsulated device
t_{HL}	s	Base life time	Turn-off current tail decay time vs. anode current (1)
I_{sne}	A	Emitter electron saturation current	Relative size of turn-off current tail decay time vs. anode current and anode voltage (2)
W_b	m	Metallurgical base width	(2)
N_b	cm^{-3}	Base doping concentration	(2)
K_{psat}	A/V^2	MOSFET channel saturation region transconductance	Saturation current vs. gate voltage (3)
V_T	V	Threshold voltage	(3)
K_{plin}	A/V^2	MOSFET channel linear region transconductance	On-state voltage vs. gate voltage at constant anode current (4)
C_{gs}	nF	Gate-source capacitance	Gate charge (5)
C_{oxd}	NF	Gate-drain overlap oxide capacitance	(5)
A_{gd}	m^2	Gate-drain overlap area	Gate-drain charge (5)

In the next subsection the different measurements are explained in detail and in the following subsection the implementation is described.

Measurements

1:Tail Decay Rate

The clamped inductive load circuit (Figure 5.1a) is used to measure the turn-off current decay rate. After the gate voltage is turned off and the anode voltage (V_A) has reached the clamp voltage (V_{clamp}), the current starts to decline. At first, the decay rate is high but then the current tails off slowly.
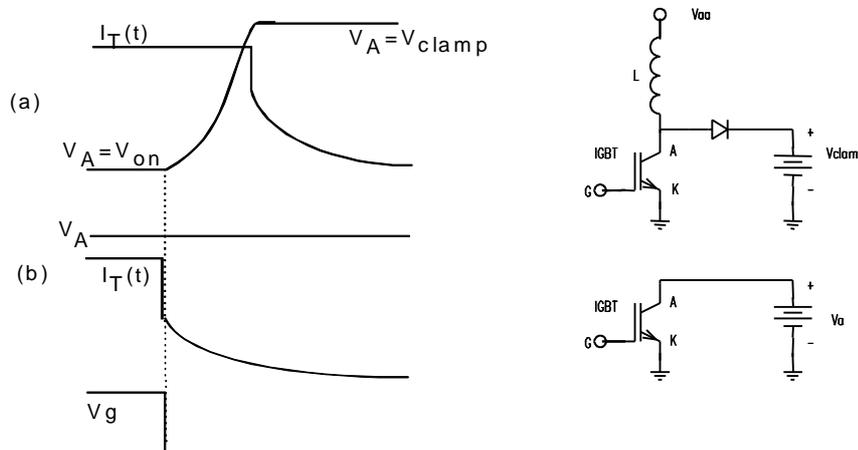
Figure 5.1 The turn-off switching waveform and circuit configuration for a) The clamped large inductive load circuit b) The constant anode supply voltage.

According to [3], the decay time constant of the *slowly* decaying tail current, for a constant anode voltage, is given by:

$$\frac{d \ln I_T}{dt} = \frac{d I_T / dt}{I_T} \approx -\frac{1}{t_{HL}}\left(1 + \frac{I_T}{I_k^t}\right)$$ (5.1)

where

$$I_k^t \equiv \frac{q^2 A^2 D_p n_i^2}{I_{sne} t_{HL}}$$ (5.2)

To extract the lifetime, a least-squares fit is done to the measured data of the inverse current decay time constant versus current, like in Figure 5.2. In accordance with eq. 5.1, the zero current intercept gives the value of $1/t_{HL}$. However the slope of the fitted curve, $1/(\tau_{HL} I_k^\tau)$, is not used to extract I_{sne} because of insufficient variation with current (I_{sne} is extracted in measurement #2).
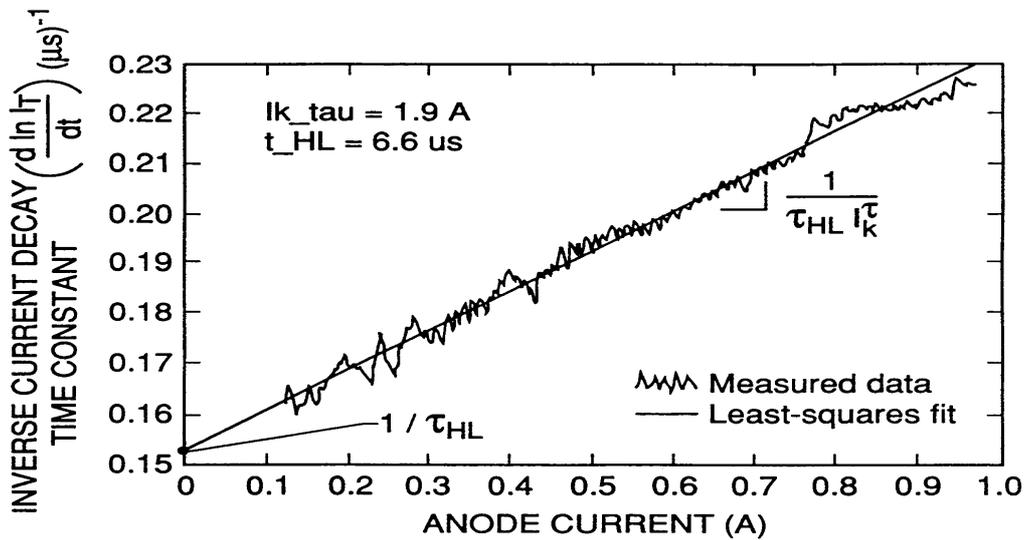
Figure 5.2 Current tail decay rate with $1/\tau_{HL}$ equal to the extrapolated zero current intercept [7].

2: Tail size versus anode current for different anode voltages

For these measurements the constant anode supply voltage circuit in Figure 5.1b, is used.
After the initial rapid current fall during turn-off, there is redistribution time for the excess carriers before the slower current tail begins. To be able to describe the tail decay time by a simple model, the current tail is extrapolated back to the MOSFET part of the curve, using the current tail of a higher initial current waveform, as in Figure 5.3b.
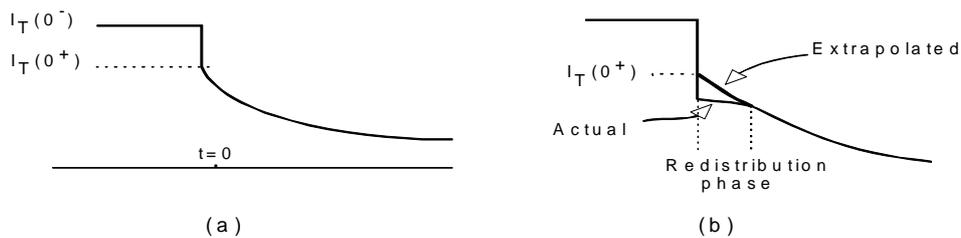
Figure 5.3 Constant anode voltage turn-off with a) current waveform indicating current levels before and after the rapid fall of the MOSFET current, and b) the redistribution phase and the extrapolation of $I_T(0^+)$.

The relative size of the extrapolated current tail is then given by [3]:

$$b_{tr,V} \equiv \frac{I_T(0^+)}{I_T(0^-) - I_T(0^+)}\bigg|_{V_A = const} = b_{tr,V}^{max}\left(1 + \frac{I_T(0^+)}{I_k}\right)^{-1} \tag{5.3}$$

where

$$b_{tr,V}^{max} = \left((W/L)^2 \frac{\coth(W/L)}{2\tanh(W/2L)} - 1\right)^{-1} \tag{5.4}$$

and

$$I_{sne} \equiv \frac{\tanh^2(W/2L)}{(W/L)^4}\left(\frac{(4qn_iAD_p)^2}{L^2(1+1/b)}\right) \cdot \frac{1}{b_{tr,V}^{max}I_k} \tag{5.5}$$

Using eq. 5.3 for different values of anode voltages, $1/\beta_{tr,V}$ can be plotted versus the initial tail current, $I_T(0^+)$, like in Figure 5.4. A least-squares fit is used to fit a slope to the measured data, and for each set of data, $\beta_{tr,V}^{max}$ is obtained from the zero current intercept and the slope, $\beta_{tr,V}^{max}I_k$, is used with eq. 5.5, in addition with prior extracted parameters A and t_{HL}, to obtain I_{sne}.
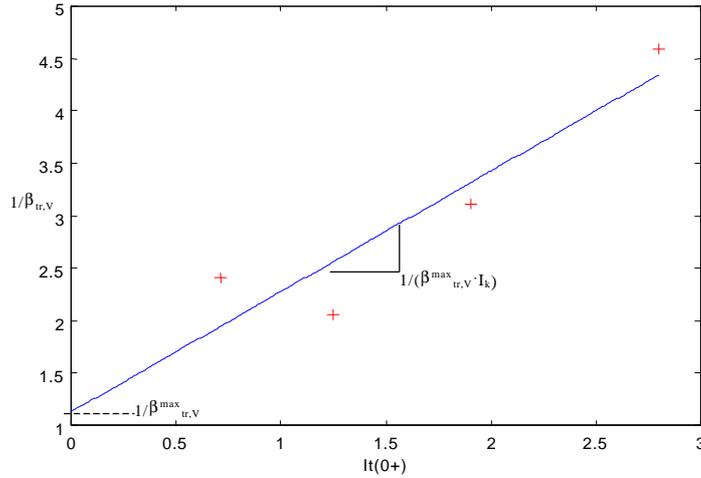
Figure 5.4 $1/\beta_{tr,V}$ versus $I_T(0^+)$ for 125 V anode voltage, indicating $\beta_{tr,V}^{max}$ at zero current intercept.

$\beta_{tr,V}^{max}$ is then used with eq. 5.4 to extract W_b and N_b. This is done by solving W (iteratively) for each $\beta_{tr,V}^{max}$ (i.e. each anode voltage) and then by plotting W versus the square root of V_A. Then, in addition with the formula, given in [3];

$$W \approx W_B - \sqrt{2e_{si}V_A/qN_B}, \tag{5.6}$$

W_b is given by the zero voltage intercept, and N_b is given by the slope of the curve.

3: Saturation current versus gate voltage

To separate the MOSFET saturation current from the IGBT anode saturation current, the current gain of the internal bipolar transistor, $(1+\beta_{ss})$, can be used, since according to [3]:

$$I_{MOS}^{sat} = I_T^{sat} / (1 + \boldsymbol{b}_{ss})$$ (5.7)

The derivation of β_{ss} is given in Appendix B.1.
The output characteristics of the IGBT, eq. 5.7 and the relationship given in [7];

$$\sqrt{I_{MOS}^{sat}} = \sqrt{K_{psat}/2}(V_{gs} - V_T)$$ (5.8)

yields K_{psat} and V_T from a linear plot with the square rote of the MOSFET saturation current versus the gate voltage.

4: On-state voltage versus gate voltage

The on-state voltage for a constant anode current is indicated for different gate voltages in Figure 5.5. The on-state voltage, V_{on}, in the linear region, is in [7] given to be proportional to K_{plin} according to:

$$V_{on} = const. + \frac{I_T}{(1 + \boldsymbol{b}_{ss})K_{plin}}\left(\frac{1}{V_{gs} - V_T}\right)$$ (5.9)

Hence, K_{plin} can be extracted from the slope of the curve if V_{on} is plotted versus $1/(V_{gs}-V_T)$.
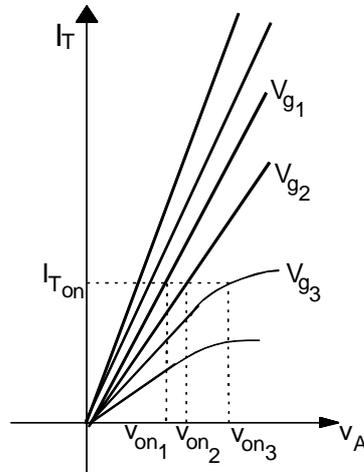
Figure 5.5 On-state voltage at a given collector current for different gate voltages.

5: Gate and gate-drain charge

The typical turn-on waveforms for the gate and anode voltage are shown in Figure 5.6. The gate circuit is designed to give a nearly constant gate current and the load to give a low anode current in order to keep the stored charge approximately equal to zero, which implies that the gate charge characteristics are similar to the ones of the structurally equivalent power MOSFET [7].
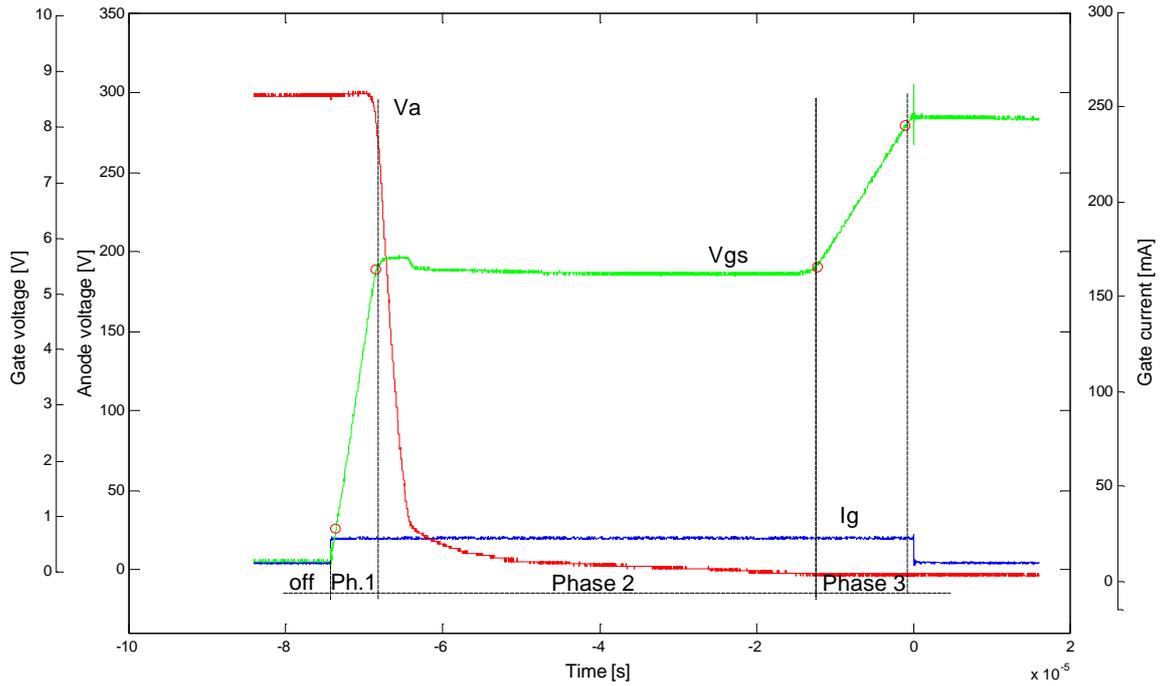
Figure 5.6 The gate and gate-drain characteristics for a low anode current and nearly constant gate current pulse.

During the first and the third phase, the gate-source voltage rises with a constant slope as the gate current charges the gate-source capacitance. The quote of the gate current and the rate of rise of the gate-source voltage is therefore used to determine the gate-source capacitance, C_{gs}, and the gate drain overlap oxide capacitance, C_{oxd}, like in Figure 5.7.
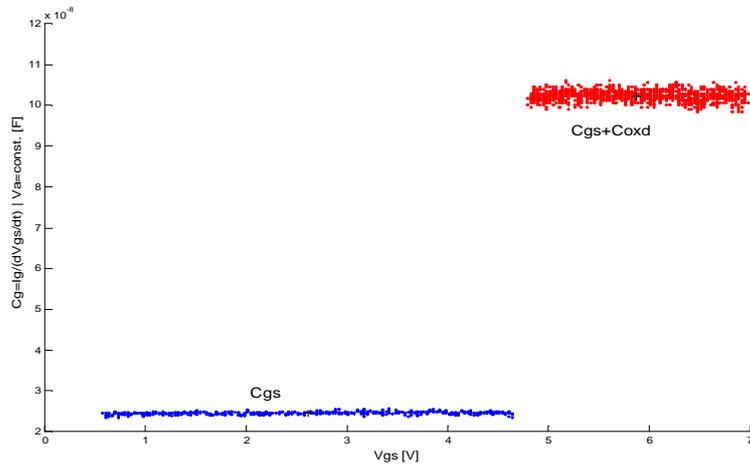
Figure 5.7 The input capacitance versus gate voltage during the first and third phase of Figure 5.6.

During the second phase, the anode voltage drops as the gate voltage stays constant and the gate current charges the voltage dependent gate-drain feedback capacitance. Like in Figure 5.8, the gate-drain depletion capacitance can be plotted versus the difference of the anode and gate voltage, using

$$C_{gd} = \frac{-I_g}{dV_A/dt}\bigg|_{V_{gs}=const.} \tag{5.10}$$

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For high values of the anode voltage, the gate-drain depletion capacitance is approximated by

$$C_{gdj} \approx \frac{A_{gd}\,\mathbf{e}_{si}}{\sqrt{2\mathbf{e}_{si}(V_A - V_{gs})/qN_B}} \qquad (5.11)$$

and with the value of the gate-drain depletion capacitance from the dashed line in Figure 5.8, the parameter A_{gd} is extracted.
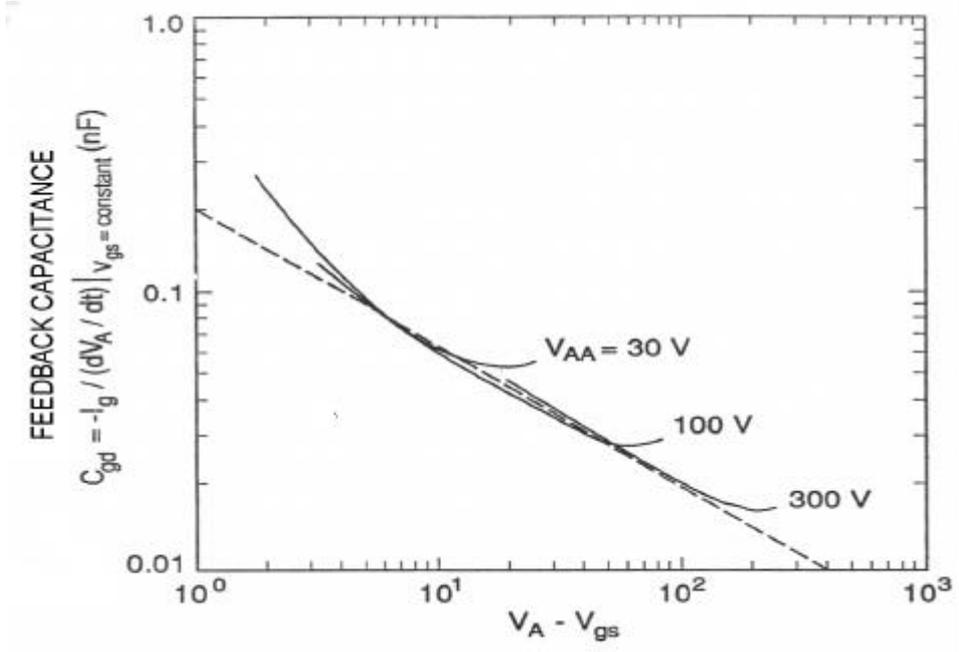
Figure 5.8   The gate-drain feedback capacitance versus anode-gate voltage for three different supply voltages. The dashed line is fitted to the waveforms of higher voltages due to the approximation in eq. 5.11[7].

5.2 Implementation of parameter extraction procedure

To perform the measurements in the previous subsection, circuits for the clamped large inductive load (measurement #1) and the constant anode supply voltage (measurements #2-4) are implemented. Additionally, two different gate drive circuits are designed; the first for supplying ± 15 V for "ordinary" gate drive conditions, and the second providing a low (≈20 mA) but constant gate current in measurement #5. In [7], the latter gate drive circuit is designed with a 100 V pulse and a gate resistor of 5 kΩ, however, owing to the lack of a 100V pulse generator, the gate drive is implemented as a current generator.
The different instruments used for the measurements are given in Appendix B.2.
The results of the measurements are logged on a computer by a serial bus and the software LeCroy Scope Explorer® ver. 2.1.

The clamped inductive load circuit and the constant anode supply circuit

The circuit configurations for these circuits are shown in Figure 5.1. Both configurations are implemented in the same circuit with the possibility to "switch" between the different circuit configurations.
To minimise the parasitic components, most components are mounted on a lamina of copper where additional wires are thin sheets of copper. The anode current is measured with a shunt resistor of 10 mΩ, placed on the lamina and also directly mounted on the IGBT. The clamp/anode voltage (V_{clamp}/V_a) is implemented with a variable transformer and a rectifier and held constant by a large capacitance (C) in parallel with a power resistor (5 kΩ) for discharging purpose.
The IGBTs are mounted on the top of a cooling flange to minimise the internal heating.

The ±15 V gate drive circuit

The gate drive circuit principally contains one optical transmitter and one receiver to get galvanic isolation from the pulse generator and two high-speed MOSFET drivers to supply sufficient current with low output impedance. It also includes a variable gate resistor in parallel with a diode for lower gate resistance at turn-off. A schematic gate drive circuit is shown in Figure 5.9.
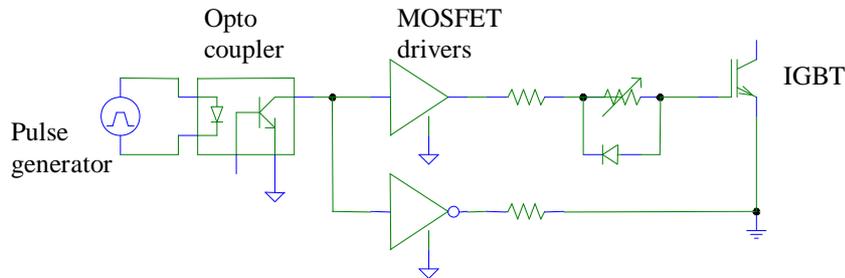
Figure 5.9 Schematic circuit configuration of the gate drive circuit for ± 15 V supply voltage.

The current generator

The constant gate current in measurement #5 is supplied by a current generator, implemented with a *pnp*-transistor and zenerdiode, which keeps a voltage of 3 V over the transistor and a variable resistor. To get a current of 20 mA, the resistance is set to approximately 130 Ω.
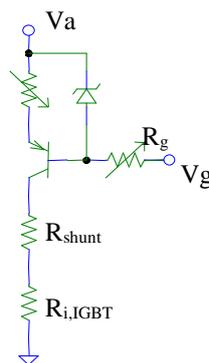
Figure 5.10 Schematic circuit configuration of the current generator.

5.3 Results of the parameter extraction

When the measurements are performed and the results logged on the computer, additionally processing of the data, described in section 5.1, is executed, which is done in MATLAB® ver. 5.3. No detailed description of each algorithm is given here, however, the basic structure of most algorithms can be summarised as follows:

- The collected data is read into MATLAB from the source file.
- The data is plotted and segments of the plotted curve are selected.
- Various curve fitting algorithms are used on the selected segments, depending on the type of IGBT and which parameter to be extracted.
- Different mathematical operators (e.g. logarithmic, derivative etc) are used to produce the desired plot (stated in section 5.1).
- If necessary, additional calculations according to section 5.1 are done to extract the final parameter.

The parameter extraction is performed on three different IGBTs: EUPEC FF300R12KE3 (NPT), SEMIKRON SKM400GB125D (NPT) and TOSHIBA MG300Q2YS40 (PT).

The result is summarised in Table 5.2 below, together with the results given in [7] (similar with the default values in PSPICE).

Table 5.2 The extracted parameters for three different IGBTs and the reference values of [7].

Parameter	Unit	Eupec	Semikron	Toshiba	Hefner [7]
A	m^2	1.7e-4*	2.0e-4	4.1e-4	1.0e-5
t_{HL}	s	8.7e-7	3.4e-6	3.9e-6	0.3 - 8.0e-6
I_{sne}	A	1.2e-11	5.1e-11	2.2e-10	6.0e-14
W_b	m	1.1e-5	2.3e-5	2.4e-5	93e-6
N_b	cm^{-3}	5.9e18	4.1e18	3.7e19	2e14
K_{psat}	A/V^2	4.0	5.5	1.6	0.4
V_T	V	6.1	6.1	4.7	5.0
K_{plin}	A/V^2	3.9	3.6	3.9	0.75
C_{gs}	nF	2.2e-8	2.2e-8	2.5e-8	0.6e-9
C_{oxd}	NF	1.0e-007	1.2e-007	7.8e-008	1.6e-9
A_{gd}	m^2	1.7e-5	2.9e-5	1.0e-5	5e-6

*received from manufacturer

The values of the parameters cannot be compared directly with the values in [7], owing to different IGBTs with different ratings, yet, the results are of interest to get an idea of the plausibility of the extracted parameters.

Most of the results are consistent, both comparing the different IGBTs as well as comparing the IGBTs with the reference values. However, the results of I_{sne} and N_b differ a great deal and, notwithstanding the difficulty of estimating some of the parameter values, the extracted base doping concentration, N_b, cannot be considered to be plausible. All the three parameters W_b, I_{sne} and N_b are extracted from the same measurement (#2) which emphasises the importance of the accuracy of the measurements. The causes and measures of the inaccurate results are discussed in the next section.

5.4 Discussion

The measured waveforms are the first encountered source of inaccuracy during the extraction procedure. Oscillations, basically caused by parasitic components, make the curve fitting process of the traces more difficult and may cause less accurate results. Although parasitic components never can be completely avoided, a different way of implementing the used circuit configurations should be investigated, in order to minimise these effects.

The most probable source of error is the processing of the collected data and the curve fitting algorithms. The general problem is the difficulty of a satisfying reproduction with a small spread of the results.
One of the reasons would seem to stem from the small number of traces used (4) for the generation of the "secondary" curves (measurement #2). This can cause a large spread of the data and an imprecise least-squares fit, like in Figure 5.11. Considering the algorithms, issues like logarithmic operations on values approaching zero or derivatives of a transient curve may cause problems with a large spread of the results as a consequence.

The number of traces can be increased by increasing the current range of the measurements, however, this may influence the conditions of the measurement (e.g. V_a may not be constant).
Another improvement is the use of normalization and residual functions in MATLAB to improve and estimate the accuracy of the numeric computations.
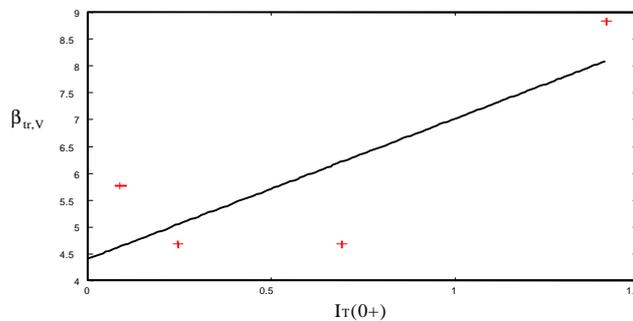
Figure 5.11 Plot of $\beta_{tr,V}$ in measurement #2 with a large spread of the data resulting in a poorly fitted least-squares fit.

6 Simulation

6.1 Simulation in PSPICE

MicroSim® PSPICE® is a software program for circuit simulation. The circuit is designed, using the built-in components, and parameters and initial conditions are set arbitrarily before the simulation is executed. The result is displayed by an additional program where all currents and voltages can be displayed as well as traces with mathematical operators, for example the dissipated energy as the integral of the dissipated power (top plot, Appendix C.2).
The MicroSim® PSPICE® Evaluation version 8.0 is used for the simulations.

6.2 Simulation of the series resonant converter

Before the series resonant converter can be fully implemented and simulated, the extracted parameter set is modified according to the parameter set in PSPICE. Most parameters are identical, however, instead of K_{plin} the parameter K_F (=K_{plin} /K_{psat}) is used and the parameters C_{gs}, C_{oxd} and J_{sne} (I_{sne}) are given in per unit area, as in Table. 6.1.

Table 6.1 The PSPICE parameters and the default values.

PSPICE parameters	Unit	Default
Area	m^2	1.0e-5
t_{HL}	s	7.1e-6
Jsne (I_{sne}/Area)*	A/V^2	6.5e-13
Wb	-	9.0e-5
Nb	V	2,00E+14
Kpsat	m^2	0.38
Vt	F/cm^2	4.7
Kf (K_{plin}/K_{psat}*)*	F/cm^2	1
Cgs	m	1.24e-8
Coxd (C_{oxd}/Agd)*	cm^{-3}	3.5e-8
Agd	A/cm^2	5.0e-6

* refers to extracted parameters .

As stated in section 5, all the extracted parameters are not correct and cannot be used for simulation. To be able to replace these and also to test the different parameters and their influence on the result, a simple test circuit, shown in Figure 6.1, is implemented where the IGBTs are tested under same conditions as in the converter (500V, 200A). The parameters are varied between the PSPICE default values and the extracted values and the result compared with datasheet ratings with respect to the shape of the waveforms and on-state voltage. This gives rather rough results, yet, most parameters are found to have little influence on the result except for N_b and to some extent J_{sne}, which is expected from section 5.

PARAMETERS:		PARAMETERS:		PARAMETERS:	
Period	30u	Wb	1e-5	Area	1.71e-4
PW	16u	Kp	4	Agd	1.7e-5
Vg	15	Tau	8.7e-7	Va	500
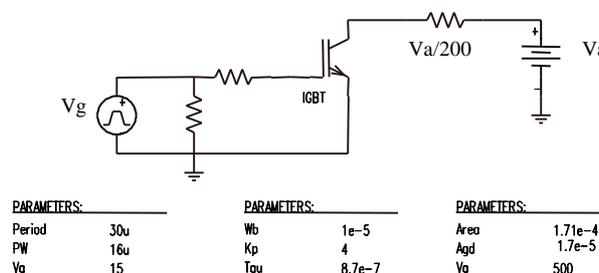
Figure 6.1 Test circuit for the IGBT parameters.

When satisfying parameter sets are achieved for all three IGBTs, the parameters are included in the PSPICE IGBT model and implemented in the converter, starting with a half-bridge to verify circuit behaviour and convergence. The full-converter is also verified, first with ideal switches, and then also with IGBTs and snubbers. The full circuit is given in Appendix C.1.

The simulations are performed at four different load conditions in accordance with the reference measurements [26] and the circuit conditions are given in Table 6.2. The load conditions for the reference measurements are lower than for the rated converter application owing to the requirement of safety margins when varying different parameters like temperature etc.

Table 6.2 The circuit conditions for the simulated series resonant converter.

Iload=100A; Vtank=400V Temp=45 deg						
IGBT	**Sim. nbr**	**Vload [V]**	**Period (T) [us]**	**Switching frequency (1/T) [kHz]**	**Rload [ohm]**	**Cload [uF]**
Eupec, Semikron, Toshiba	1	5	30,9	32,36E+3	0,05	350
	2	40	31,5	31,75E+3	0,4	300
	3	180	33,3	30,03E+3	1,8	175
	4	360	40,2	24,88E+3	3,6	175

The output of the simulations, like the one shown in Appendix C.2, is analysed and the total average losses during five periods are calculated by dividing the total dissipated energy (top plot) with the total time. Furthermore, the total losses can be divided into conduction losses and switching losses, which is visible in the middle-top plot where the peaks are the switching losses. The middle-bottom plot shows the voltage and current of one IGBT(ZA1) and the bottom plot shows the load current and voltages and currents of the LC-tank (L_r and C_r in the circuit in Appendix C.1).

6.3 Results

The results of the simulations for all IGBTs and for two different parameter sets are given in Appendices C.3 and C.4, with the parameter values in C.5. The default parameter set is not used since the calculations of the simulation do not converge and the unmodified extracted parameter set does not give realistic output waveforms. Modification of two of the parameters (N_b and J_{sne}) yields better results, shown in Diagram 6.1 – 6.3, although this procedure is not very realistic since the parameters are optimised in accordance with the known reference values. Nevertheless, this indicates the importance of correct parameter values and a careful extraction procedure.

From the diagrams it is seen that the parameter set, "Optimised2", gives the best results. The discrepancy in the results of the Eupec IGBT is a result of the reference values having a different control strategy (dual control) as well as a load current of only 75 A.
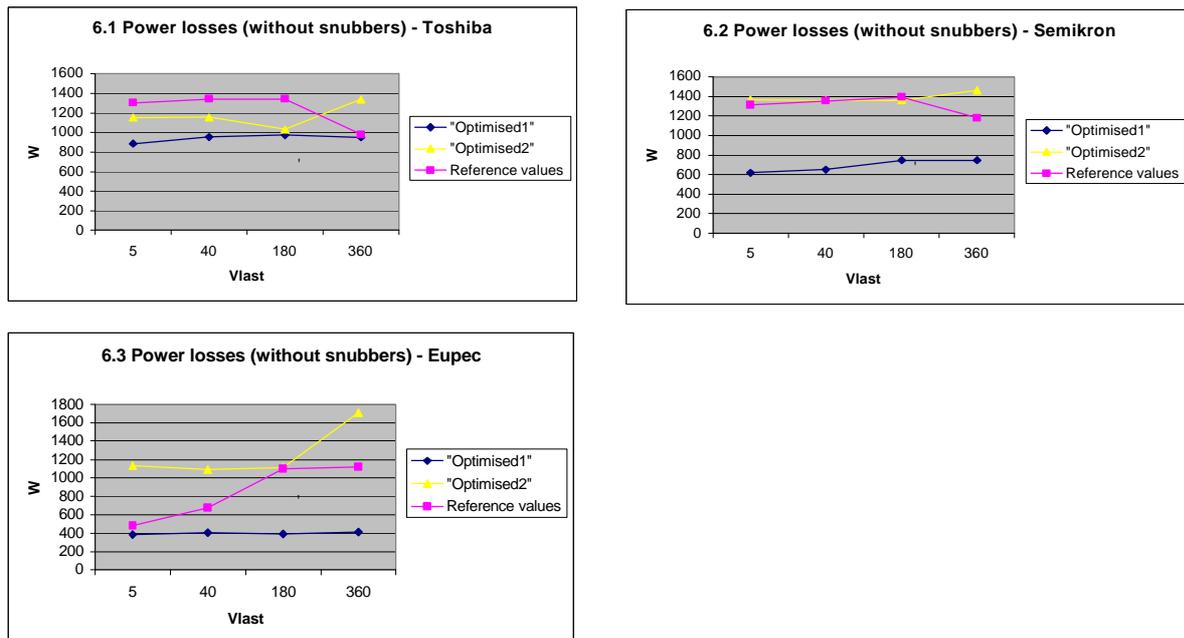
Diagram 6.1 – 6.3 Power losses with two different parameter sets ("Optimised 1" and "Optimised 2").

The parameter extraction procedure is developed for NPT IGBTs, yet, only a minor difference is noticeable between the results of the SEMIKRON (NPT) and TOSHIBA (PT).

The results (Appendices C.3, C.4) also indicate that the model does not emulate the circuit behaviour with snubbers accurately. Instead of decreasing the losses as would be expected, the snubbers actually increase them, owing to increased switching losses at turn-on (90% of the total losses). The reason for this is not easily explained without an in-depth analysis, yet, it is evident that the snubber affects the transient characteristics and transfers the transistor model into a region where the model equations no longer are valid.

During simulation, additional factors and their impact on circuit behaviour are studied. One of these is the influence of the freewheeling diode model. Different parameter sets are studied along with different gate resistors without any major variation of the results. This cannot really be expected since the reverse recovery current of the diode is minimal owing to the soft turn-on of the IGBTs.
As a consequence of the roughly optimised parameter sets, a minor leakage current can be observed, which gives rise to negative power losses, hence, reducing the total power losses. However, a comparison with the absolute value of the dissipated power results in a difference of only 1%, which can be considered to be negligible.

6.4 Discussion

One of the fundamental features, which would support the accuracy of the PSPICE model, is the similarity to the Hefner model [3]-[8]. The Hefner model is implemented in SABER® in [23] and stated to be accurate "for the range of static and dynamic conditions in which the device is intended to be operated". However these conditions are for low power applications (20A, 600V) and may be a reason why the performance of the PSPICE model is unsatisfying for operation at 100A, 400V.

As mentioned previously, a thoroughly study of the implementation made in [9] has to be undertaken to find the underlying causes of the inaccuracy of the PSPICE model, but on account of the inability to obtain the mentioned reference, this has not been possible. Moreover, the incomplete set of equations given in [10] is not sufficient enough to draw any conclusions, however, constitutes a source of criticism since the units of some of the parameters are not consistent. The parameters referred to is C_{gs}, C_{oxd} and J_{sne}, which are given in per unit area (cm^{-2}), yet, multiplied by an area in units of m^2 in the equations. Whether this is an error of the referenced text or the actual implementation of the equations is left unsaid and only stated as an observation.

7 Conclusions

7.1 Results

The objective of this thesis is to find an appropriate IGBT model for power loss calculation and to verify its performance. This has been done by means of the validation of the MicroSim® PSPICE® IGBT model, resulting from an initial literary study. The validation process involves a parameter extraction procedure and a subsequent circuit simulation including the extracted parameter set, to compare the simulated results with the measured reference values. These results are summarised below.

The results of section 6, indicate one major factor above all; the importance of a careful extraction procedure and the accuracy of the parameters. Sufficient results are obtainable, but only for the unrealistic scenario where the parameters are optimised to fit the simulation results to the measured reference values.
Furthermore, the model, even when including the "correct" parameter set resulting in the most accurate results, is marred by difficulties of producing accurate results for the entire range of loading conditions.
Additionally, the performance of the model, trying to emulate the circuit behaviour at soft switching (capacitive turn-off snubbers), is totally insufficient.
Consequently, the evaluated model is found not to comply with the stated specifications of section 1.

7.2 Future work

None of the IGBT models studied in the literary survey can clearly be stated as the obvious choice. Often, even though the proposed model seems to be accurate, it is not validated and verified by enough measurements or only for low power operating conditions. Nevertheless, there are some models, which can be of interest for future implementation and validation, and these are briefly discussed below.

For PSPICE simulators the models proposed in [12] and [24] are of interest. In [12] a model for both low and high voltage levels (1200A, 3300V) is developed and stated to have better performance than the built-in PSPICE model [14]. The design approach is the lumped charge model and the parameter extraction procedure is based on Hefner [7].
The other model, [24], implemented using the ABM facility (Analog Behavioral Modeling) in PSPICE, is shown to be more accurate than [14], however failed to prove the overall performance.

Lauritsen *et al.* have developed a model in [13], with three objectives: easy parameter extraction, accurate static and dynamic performance and source code available in the public domain. The model was implemented in the SABER circuit simulator and validated for medium power applications. However, the available source code was recently removed owing to bugs and errors of the code.

Previously, the importance of the parameter extraction procedure has been emphasised. However, the sequence developed by Hefner in [7] is not easily realised successfully and as is stated in [25]; "*only a few laboratories throughout the world have the capability to accurately extract the IGBT model parameters*".
In order to simplify the extraction procedure, a software package has been developed by Hefner and Bouché in [25]. The package consist of five different programs, each with an graphical interface, which extract the 20 parameters used by the Hefner model [23], and uses the IEEE 488 bus to control the measurement instruments.
This software should facilitate the extraction process significantly and, together with the Hefner model implemented in SABER, would probably achieve a sufficient result of the stated objective.
Another possibility is to obtain the parameters, or even the complete IGBT model, from the manufacturers. This is preferable since the manufacturers have the necessary knowledge and capability to obtain these results.
Finally, new releases of circuit simulators usually include extensive libraries containing various devices for direct implementation into the design and future releases may offer the simplest way of achieving the appropriate model.

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Appendix A

A.1 Optimal value of snubber capacitor

The value of the capacitor should be chosen in a way where the capacitor voltage reaches its maximum value, V_{DC}, at the same instant as the current is equal to zero, like in Figure 2.4b. If the optimal value for the capacitor is denoted, C_{base}, and the fall/rise time for the load current/capacitor voltage is denoted t_{fi}, then a mathematical expression for C_{base} would be [22]:

$$i_{CS} = I_0 - i_T = I_0 - I_0(1 - \frac{t}{t_{fi}}) = I_0 \frac{t}{t_{fi}} \quad 0 < t < t_{fi} \qquad (A-1)$$

where i_T is the transistor current and I_0 is the full load current.

$$v_{CS}(t) = \frac{1}{C_S} \int i_{CS}\ dt = \frac{I_0 \cdot t^2}{2 \cdot C_S \cdot t_{fi}} \qquad (A-2)$$

$$v_{CS}(t_{fi}) = V_{DC} \quad \Rightarrow \quad C_S = C_{Base} = \frac{I_0 \cdot t_{fi}}{2 \cdot V_{DC}} \quad \Rightarrow \quad v_{CS}(t) = V_{DC} \cdot \left(\frac{t}{t_{fi}}\right)^2 \qquad (A-3)$$

A.2 Undamped series resonant circuit

The undamped series resonant circuit is shown in Figure A.1, where V_d is the input voltage at time t_0 and the initial conditions are I_{L0} and V_{C0}. If the inductor current is denoted i_L and the capacitor voltage v_c, then the circuit equations are [20]:

$$L_r \frac{di_L}{dt} + v_c = V_d \qquad (A-4)$$

and

$$C_r \frac{dv_c}{dt} = i_L \qquad (A-5)$$

with the solution for $t \geq t_0$:

$$i_L(t) = I_{L0} \cos w_0(t-t_0) + \frac{V_d - V_{c0}}{Z_0} \sin w_0(t-t_0) \qquad (A-6)$$

and

$$v_c(t) = V_d - (V_d - V_{c0}) \cos w_0(t-t_0) + Z_0 I_{L0} \sin w_0(t-t_0) \qquad (A-7)$$

where

$$\text{the angular resonance frequency} = w_0 = 2pf_0 = \frac{1}{\sqrt{L_r C_r}} \qquad (A-8)$$

and

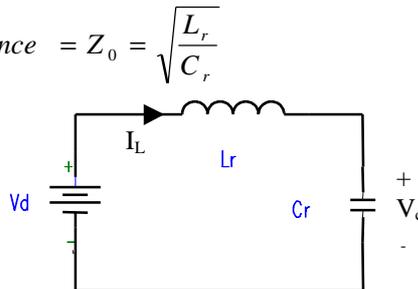$$\text{the characteristic impedance} = Z_0 = \sqrt{\frac{L_r}{C_r}} \qquad (A-9)$$

Figure A.1 The undamped series resonant circuit.

Appendix B

B.1 Derivation of b_{ss}

The electron and hole currents in the base, for an active area A, are given in [3] by:

$$I_n(x) = \frac{P_0^2 I_{sne}}{n_i^2} + \frac{qP_0 AD}{L} \cdot \left(\coth\left(\frac{W}{L}\right) - \frac{\cosh[(W-x)/L]}{\sinh(W/L)} \right) \qquad (B-1)$$

$$I_p(x) = \frac{P_0^2 I_{sne}}{bn_i^2} + \frac{qP_0 AD}{L} \cdot \left(\frac{\coth(W/L)}{b} + \frac{\cosh[(W-x)/L]}{\sinh(W/L)} \right) \qquad (B-2)$$

where, if x = 0 is defined as the emitter edge of the base and x = W the collector edge, the steady-state boundary conditions for the excess carrier distribution are defined as:

$$\phi(0) \equiv P_0, \quad \phi(W) = 0$$

The anode current, evaluated at $x=W$, is then given by [3]:

$$I_T = I_n(W) + I_p(W) = \frac{P_0^2 I_{sne}}{n_i^2} + \frac{qP_0 AD}{L} \cdot \left(\coth\left(\frac{W}{L}\right) - \frac{1}{\sinh(W/L)} \right) +$$

$$+ \frac{P_0^2 I_{sne}}{bn_i^2} + \frac{qP_0 AD}{L} \cdot \left(\frac{\coth(W/L)}{b} + \frac{1}{\sinh(W/L)} \right) =$$

$$= \frac{P_0^2 I_{sne}}{n_i^2}(1 + 1/b) + \frac{P_0 qAD}{L} \cdot \coth(W/L)(1 + 1/b) \qquad (B-3)$$

$$\Rightarrow$$

$$P_0^2 + Q_1 P_0 - Q_2 I_T = 0 \qquad (B-4)$$

where

$$Q_1 = \frac{qAD}{L} \cdot \frac{n_i^2}{I_{sne}} \coth(W/L) \qquad and \qquad Q_2 = \frac{n_i^2}{I_{sne}} \frac{1}{1 + 1/b}$$

Hence, P_0 can be expressed in terms of I_T by solving the quadratic equation in B-4.

The expression for the steady-state common emitter current gain of the bipolar transistor, β_{ss}, given in [3], in addition with the solution and coefficients of B-4, result in an expression for β_{ss} in terms of P_0 (consequently in terms of I_T):

$$b_{ss} = \frac{I_p(W)}{I_n(W)} = \frac{\dfrac{P_0^2 I_{sne}}{bn_i^2} + \dfrac{qP_0 AD}{L} \cdot \left(\dfrac{\coth(W/L)}{b} + \dfrac{1}{\sinh(W/L)} \right)}{\dfrac{P_0^2 I_{sne}}{n_i^2} + \dfrac{qP_0 AD}{L} \cdot \left(\coth\left(\dfrac{W}{L}\right) - \dfrac{1}{\sinh(W/L)} \right)} =$$

$$= \frac{(1/b)P_0 + \dfrac{n_i^2}{I_{sne}} \dfrac{qAD}{L} \cdot \coth(W/L)\left(\dfrac{1}{b} + \dfrac{1}{\coth(W/L)\sinh(W/L)} \right)}{P_0 + \dfrac{n_i^2}{I_{sne}} \dfrac{qAD}{L} \cdot \coth(W/L)\left(1 - \dfrac{1}{\coth(W/L)\sinh(W/L)} \right)} =$$

$$= \frac{(1/b)P_0 + Q_1\left(\dfrac{1}{b} + \dfrac{1}{\cosh(W/L)} \right)}{P_0 + Q_1\left(1 - \dfrac{1}{\cosh(W/L)} \right)} \qquad (B-5)$$

B.2 Measurement instruments

Measurement	Label	Instrument name	Model
IGBT parameter extraction	Vg	10 MHz Pulse Generator	Thurlby Thandard Instruments TGP110
	Vaa	Power supply(5V,0-20V,0-40V;2.5A)	Powerbox 3000
	Vclamp ,Va	Variable transformer	Metrel Ma 4804
	Vcc	Power supply(5V,12V,0-30V;2.5A)	Velleman PS 603
	L	inductor	44uH (2*22uH)
	C	capacitance	2200uF
	Vg	HV Differential probe	SI-9000A
	It	Shunt resistor (10 mΩ)	LEM 25
		Oscilloscope	LeCroy 3904AM

Appendix C

C.1 PSPICE simulation model of the series resonant converter
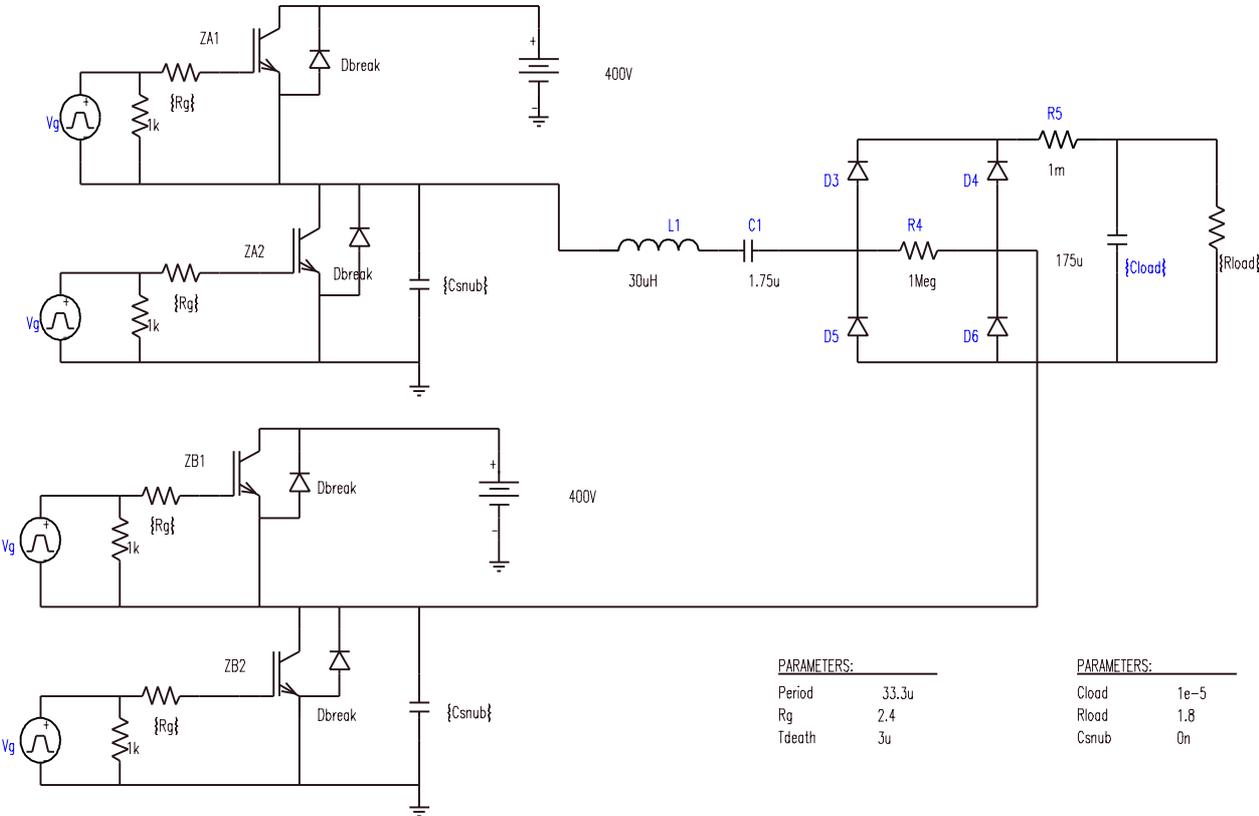
C.2 Simulation output - Eupec
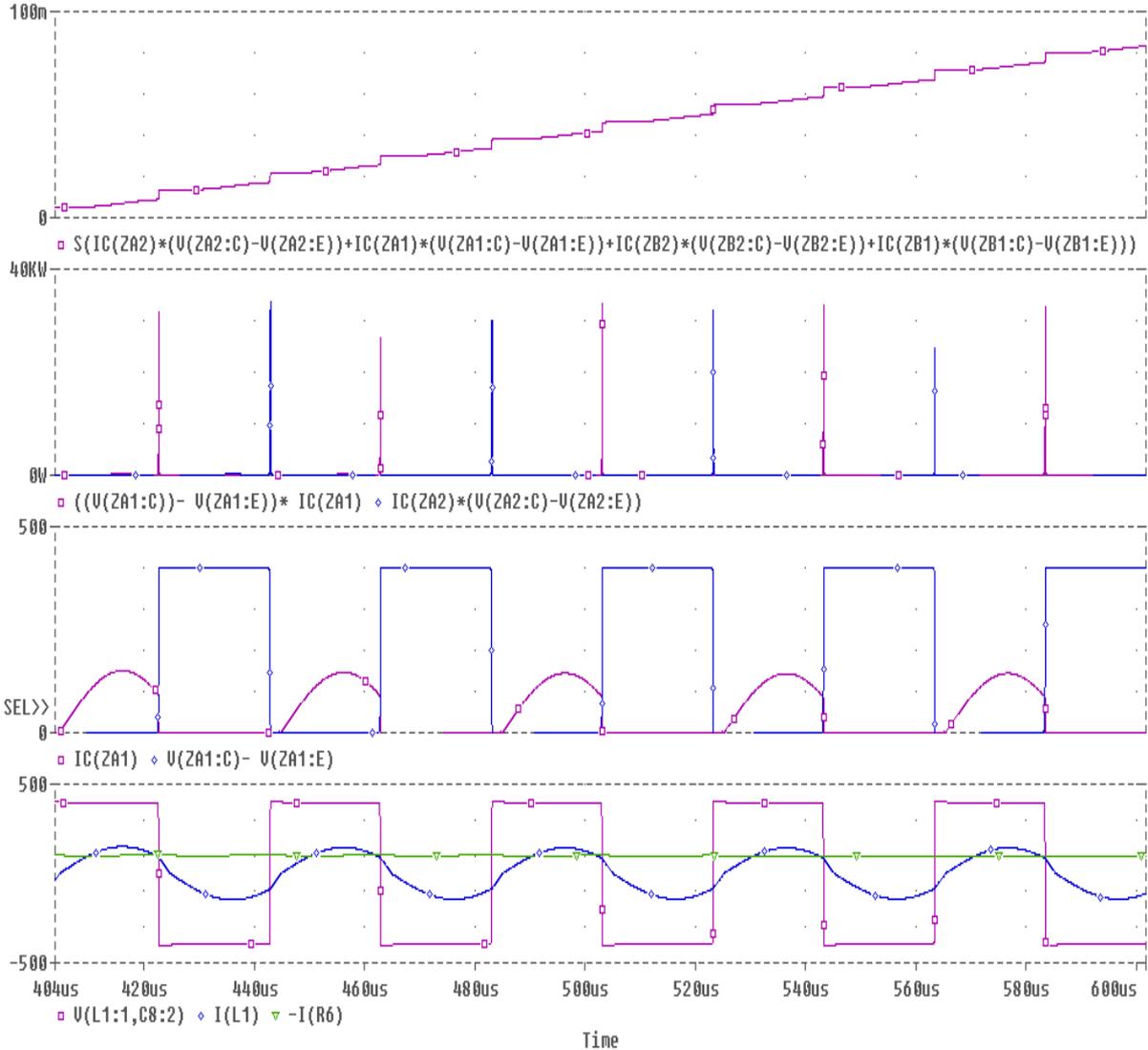
Vload = 5 V Csnubber = 0 nF

Top plot: Total energy losses in all of the four IGBTs.

Middle-top plot: Power losses in ZA1 and ZA2. Each peak corresponds to the instant switching loss.

Middle-bottom plot: Current and voltage of ZA1.

Bottom plot: The LC-tank voltage (square-wave), LC-tank current (sine-wave) and load current (≈ 100A).

C.3 Power losses - Parameter set: "Optimised1"

IGBT	Sim. nbr	Vload [V]	Total power losses [W]		Switching losses* [%//kW]		Ref. values without snubber		Ref. values with snubber	
			no snubber	Snubber (C=390nF)	no snubber	snubber (C=390nF)	[W]**	[P_{meas}/P_{ref}]	[W]	[P_{meas}/P_{ref}]
Eupec	1	5	386	878	62//70	70//10	480	80,42%	-	-
	2	40	405	894	59//73	71//11	675	60,00%	450	198,67%
	3	180	395	891	53//67	83//9,7	1100	35,91%	630	141,43%
	4	360	415	1028	51//35	58//29	1120	37,05%	690	148,99%
Semikron	1	5	617	1063	49//52	-	1310	47,10%	920	115,54%
	2	40	653	1075	48//68	-	1350	48,37%	960	111,98%
	3	180	748	1144	42//61	-	1390	53,81%	1000	114,40%
	4	360	746	1354	35//33	-	1180	63,22%	870	155,63%
Toshiba	1	5	885	1563	66//69	-	1300	68,08%	650	240,46%
	2	40	955	1527	66//67	-	1340	71,27%	660	231,36%
	3	180	971	1598	55//47	-	1340	72,46%	700	228,29%
	4	360	950	1831	56//31	-	980	96,94%	650	281,69%

*fraction of total (energy-)losses // maximum peak of power for all IGBTs during simulation. Not measured for all snubbers since results are unrealistic.

**For Eupec:Dual Control, 75A; others Freq.Mod., 100A

C.4 Power losses - Parameter set: "Optimised2"

IGBT	Sim. nbr	Vload [V]	Total power losses [W]		Switching losses* [%//kW]		Ref. values without snubber		Ref. values with snubber	
			no snubber	snubber (C=390nF)	no snubber	snubber (C=390nF)	[W]**	[P_{meas}/P_{ref}]	[W]	[P_{meas}/P_{ref}]
Eupec	1	5	1132	2617	48//73	x	480	235,83%	-	-
	2	40	1096	2528	92//72	x	675	162,37%	450	561,78%
	3	180	1115	2549	90//66	x	1100	101,36%	630	404,60%
	4	360	1713	2551	93//26	x	1120	152,95%	690	369,71%
Semikron	1	5	1364	2318	67//56	x	1310	104,12%	920	251,96%
	2	40	1360	2278	70//70	x	1350	100,74%	960	237,29%
	3	180	1358	2288	68//62	x	1390	97,70%	1000	228,80%
	4	360	1460	2341	72/28	x	1180	123,73%	870	269,08%
Toshiba	1	5	1149	2095	68//71	x	1300	88,38%	650	322,31%
	2	40	1153	2080	65//72	x	1340	86,04%	660	315,15%
	3	180	1029	2126	59//50	x	1340	76,79%	700	303,71%
	4	360	1337	2356	68//27	x	980	136,43%	650	362,46%

*fraction of total (energy-)losses // maximum peak of power for all IGBTs during simulation. Not measured for snubbers since results are unrealistic.

**For Eupec:Dual Control, 75A; others Freq.Mod., 100A

C.5 Parameter sets for the PSPICE simulation

IGBT	Parameter set	Area [m^2]	Tau [s]	Kpsat [A/V^2]	Kf [ ] (Kplin/ Kpsat)	Vt [V]	Agd [m^2]	Cgs [F/cm^2] (Cgs)	Coxd [F/cm^2] (Coxdj/Agd)	Wb [m]	Nb [cm^-3]	Jsne [A/cm^2] (Isne/Area)
Default		1.0e-5	7.1e-6	0.38	1	4.7	5.0e-6	1.24e-8	3.5e-8	9.0e-5	2,00E+14	6.5e-13
Eupec	Extracted	1.71e-4	8.743e-7	4.0276	0.968	6.05	1.692e-5	2.165e-8	607.2e-9	1.081e-5	5.906e18	7.205e-12
	Optimised1	"	"	"	"	"	"	"	"	"	1,00E+13	2.2e-9
	Optimised2	"	"	"	"	"	"	"	"	"	1,00E+13	2.7e-10
Semikron	Extracted	1.96e-4	3.416e-6	5.4970	0.657	6.12	2.940e-5	2.171e-8	398.5e-9	2.271e-5	4.105e18	2.582e-11
	Optimised1	"	"	"	"	"	"	"	"	"	1,00E+13	2.58e-10
	Optimised2	"	"	"	"	"	"	"	"	"	1,00E+13	5.58e-11
Toshiba	Extracted	4.11e-4	3.896e-6	1.5597	2.48	4.71	0.9863e-5	2.456e-8	787.7e-9	2.415e-5	3.737e19	5.440e-11
	Optimised1	"	"	"	"	"	"	"	"	"	9,00E+12	4.44e-10
	Optimised2	"	"	"	"	"	"	"	"	"	1,00E+13	2.44e-10