Exam in Power Electronics, EIEN25
2020-06-04, 08:00-13:00

Means of assistance:		Calculator
Grades:	20-30 p:	3
	31-40 p:	4
	41-50 p:	5

In total 5 exercises

Reminder! Clear handwriting and figure drawing for the scanning with CamScanner.

Send the scanned solutions to:

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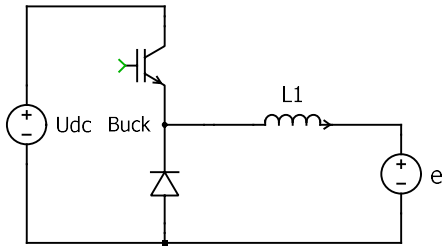
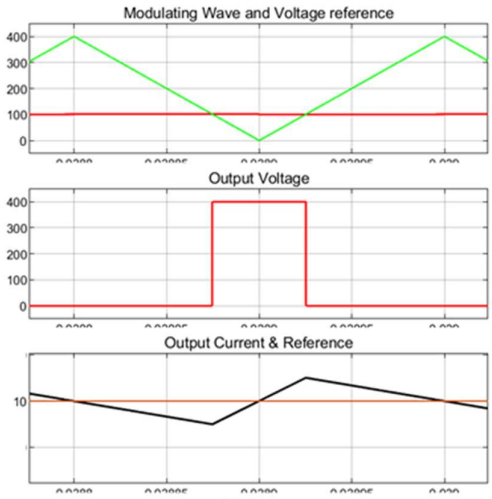
1 1Q converter, losses and temperature

A buck converter[1] supplies a load according to the figure. The semiconductor are mounted on a heat sink[2]. The converter is modulated with a 5 kHz carrier wave, Udc=400V, e=100V, L=1.5 mH. The current to the load has an average value of 10 A. The following data is extracted from data-sheets:



IGBT:

- Threshold voltage = 1.0 V
- Differential resistance = 5.0 mohm.
- Turn-on loss E_{on} = 1.5 mJ assuming a DC link voltage and current of 400 V DC and 50 A
- Turn-off loss E_{off} = 0.6 mJ assuming a DC link voltage and current of 400 V DC and 50 A



Diode:

- Threshold voltage = 0.8 V
- Differential resistance = 7 mohm.
- Reverse recovery Charge Q_f = 1 µC @ 400 V DC link & 50 A

[1] Microsemi APTGTQ100SK65T1G

[2] ATS-X50400G-C1-R0

Thermal:

- Thermal resistance of the heat sink $R_{th,ha}$ = 2.6 K/W
- Thermal resistance of the IGBT R_{th,jc_T} = 0.6 K/W
- Thermal resistance of the Diode R_{th,jc_D} = 0.7 K/W
- Ambient temperature = 35 C

Disregard the thermal resistance case-to-heatsink.

a) Calculate the current ripple. (3p)

$$\Delta i = \frac{Udc - e}{L} \cdot \Delta t = \frac{400 - 100}{1.5e^{-3}} \cdot \frac{1}{5000} \cdot \frac{1}{4} = 10$$

b) Calculate the losses of the transistor and the diode. (4p)

$$i_{T,ave} = \frac{10}{4} = 2.5\ A$$

$$i_{T,RMS} = \sqrt{\frac{1}{4} \cdot \frac{(5^2 + 15^2 + 5 \cdot 15)}{3}} = 5.2\ A$$

$$i_{D,ave} = \frac{10 \cdot 3}{4} = 7.5\ A$$

$$i_{D,RMS} = \sqrt{\frac{3}{4} \cdot \frac{(5^2 + 15^2 + 5 \cdot 15)}{3}} = 9.0\ A$$

$$P_T = 1.0 \cdot 2.5 + 5e^{-3} \cdot 5.2^2 + \left(1.5e^{-3} \cdot \frac{5}{50} + 0.6e^{-3} \cdot \frac{15}{50}\right) \cdot 5000 = 4.3\ W$$

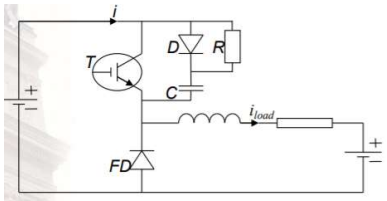
$$P_D = 0.8 \cdot 7.5 + 7e^{-3} \cdot 9.0^2 + 400 \cdot 1e^{-6} \cdot \frac{15}{50} \cdot 5000 = 7.2\ W$$

c) Calculate the junction temperatures of the transistor and the diode. (3p)

$$T_h = 35 + (4.3 + 7.2) \cdot 2.6 = 64.9\ C$$
$$T_T = 64.9 + 4.3 \cdot 0.6 = 67.5\ C$$
$$T_{TD} = 64.9 + 7.2 \cdot 0.7 = 69.9\ C$$

2 Snubbers and semiconductors

a) Draw an IGBT equipped step-down chopper (buck converter) with an RCD snubber. Give a detailed description of how the RCD charge-discharge snubber operates at turn on and at turn-off. Explain why the snubbers are needed. (2 p.)



At turn off of transistor T, the capacitor C limits the over voltage on T due to leakage inductances in the DC link. The current i commutates over to the capacitor C via diode D. The capacitor C charges until the potential of the

transistor emitter reduces till when the diode FD becomes forward biased and thereafter the load current i_{load} flows through diode FD and the current i=0.

At turn on of the transistor T, the Capcitor C is discharged via R to limite the discharge current through T. The capacitor C is discharged via the transistor T and resistor R. The diode FD becomes reverse biased and the current i commutates to the transistor T.

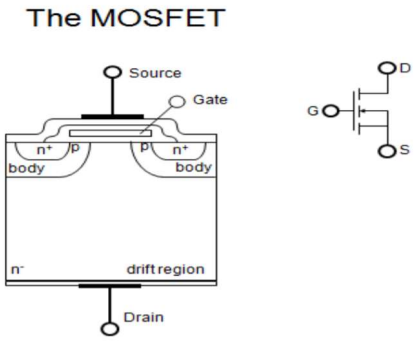
b) The DC link voltage on the supply side is 400V and the load voltage is 100 V. Calculate the snubber capacitor for the commutation time 0.005 ms. The load current is 15 A, assumed constant during the commutation. Calculate the snubber resistor so the discharge time (3 time constants) of the snubber capacitor is less than the IGBT on state time. The switch frequency is 5 kHz (3 p.)

$$i_C = C \cdot \frac{du_C}{dt} \rightarrow C = \frac{i_C}{\frac{du_C}{dt}} = \frac{15}{\frac{400}{5e^{-6}}} = 0.1875\ \mu F$$

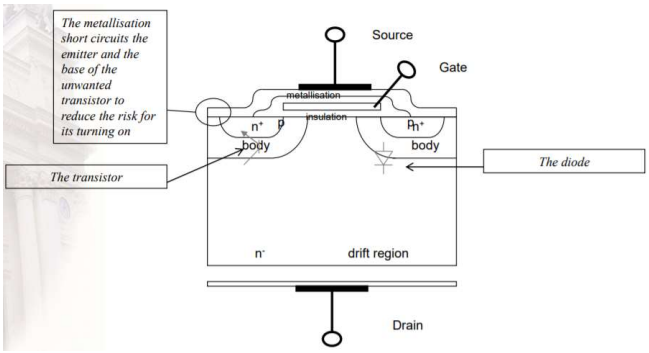
$$t_{T,ON} = \frac{1}{5000 \cdot 4} = 50\ \mu s$$

$$\tau = \frac{50e^{-6}}{3} = R \cdot C \rightarrow R = \frac{50e^{-6}}{3 \cdot C} = 89\ \Omega$$

c) Draw a figure with the diffusion layers in a (n-channel) MOSFET (2 p.)



d) Where in the (n-channel) MOSFET diffusion layers structure can an unwanted NPN-transistor be found, and where can the anti-parallel diode be found? (2 p.) What in the MOSFET layout reduces the risk that this unwanted transistor is turned on?

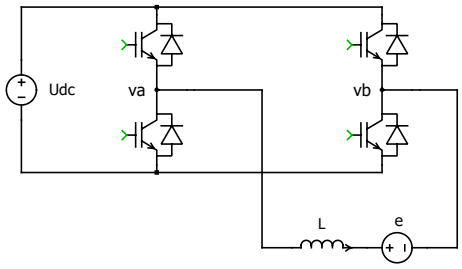


e) Which layer is always present in a power semiconductor? How is it doped? (1 p.)

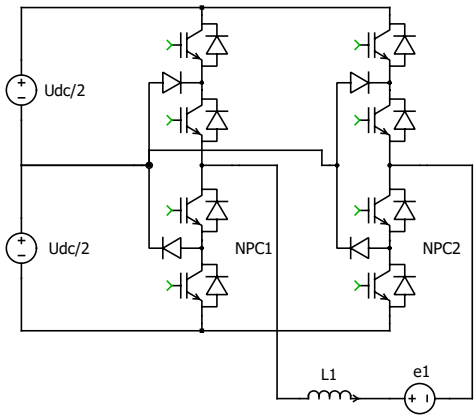
The depletion region that is doped n-. It is an insulating region within a conductive, doped semiconductor material where the mobile charge carriers have been diffused away or have been forced away by an electric field. The only elements left in the depletion region are ionized donor or acceptor impurities. The depletion region is so named because it is formed from a conducting region by removal of all free charge carriers, leaving none to carry a current

3 4Q converter

A 4Q converter can be implemented either with a 2-level or a 3-level structure (illustrated to the right). In either case, the converter is used for current control of a DC-load. The converter is modulated with a 5 kHz carrier wave, U_{dc}=400V, e=100V, L=2 mH.



A load current reference step is made from 0 A to 30 A. Then after four carrier wave periods the current reference is again set to 0 A.



a) Illustrate the potential references together with the carrier wave, the output potentials, and the load voltage for the 2-level case for a few periods before the positive step (0-> 30A) to a few periods after the negative step (30->0 A) (2 p)

The positive current step:

$$T_s = \frac{1}{5000} \cdot \frac{1}{2} = 1e^{-4}$$

$$u^* = \frac{L}{T_s} \cdot (i^* - i) + e = \frac{2e^{-3}}{1e^{-4}} \cdot (30 - 0) + 100 = 700 = 100 + (300 + 300)$$

$$= 400 \;\&\; 400\ V, i.e.\ two\ sampling\ periods\ needed\ which\ means\ one\ carrier\ wave\ period$$

$$u^* = \frac{L}{T_s} \cdot (i^* - i) + e = \frac{2e^{-3}}{1e^{-4}} \cdot (0 - 30) + 100 = -500 = 100 - (500 + 100)$$

$$= -400\ and\ 0\ V, i.e.\ one\ sampling\ period\ with$$

$$-400\ V\ and\ one\ with\ 0\ V\ needed$$

b) Illustrate the load current for the same period, accounting for the correct current derivatives. (2p)

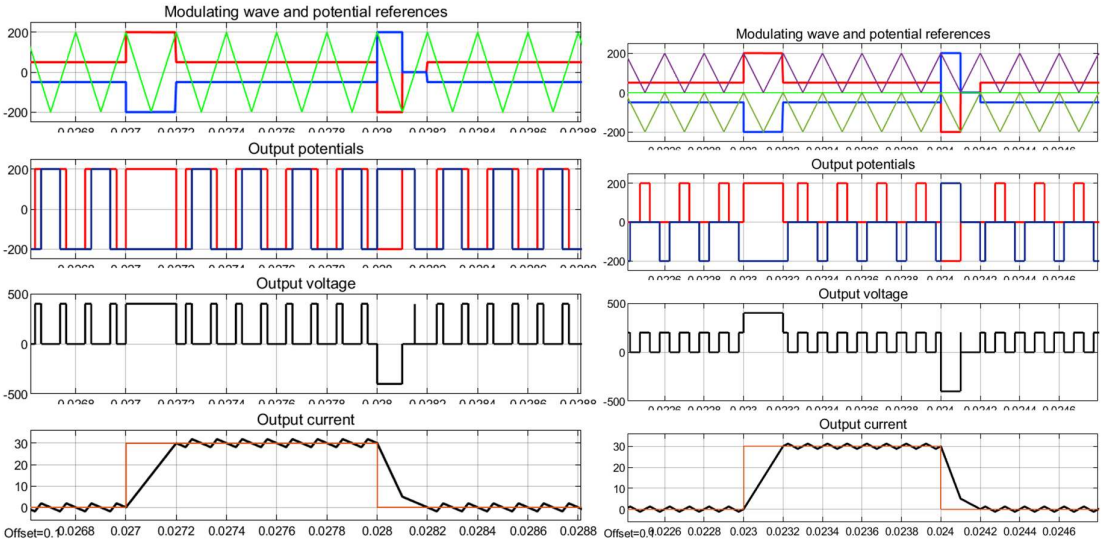
The current derivatives can be expressed as:

$$\frac{di}{dt} = \begin{cases} \dfrac{U_{dc} - e}{L} = \dfrac{400 - 100}{2e^{-3}} = 150kA/s \\ \dfrac{0 - e}{L} = \dfrac{0 - 100}{2e^{-3}} = -50kA/s \\ \dfrac{-U_{dc} - e}{L} = \dfrac{-400 - 100}{2e^{-3}} = -250kA/s \end{cases} \quad for\ the\ 2-level\ converter, and$$

$$\frac{di}{dt} = \begin{cases} \dfrac{U_{dc} - e}{L} = \dfrac{400 - 100}{2e^{-3}} = 150kA/s \\ \dfrac{U_{dc}/2 - e}{L} = \dfrac{400 - 100}{2e^{-3}} = 50kA/s \\ \dfrac{0 - e}{L} = \dfrac{400 - 100}{2e^{-3}} = -50kA/s \\ \dfrac{-U_{dc/2} - e}{L} = \dfrac{400 - 100}{2e^{-3}} = -150kA/s \\ -\dfrac{U_{dc} - e}{L} = \dfrac{400 - 100}{2e^{-3}} = -250kA/s \end{cases}$$

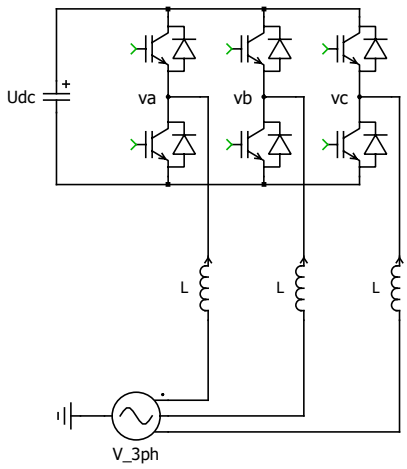
c) Like in a), but for the 3-level converter (3p)

d) Like in b), but for the 3-level converter. (3p)



4 3-phase converter, active filter

A 2-level 3-phase converter is used as an active filter in the power grid. The grid voltage is a 400 V (phase-to-phase RMS) symmetric 3-phase system. The rated power is 100 kW and the phase inductances are L=1 mH each.



a) What is the lowest DC link voltage (U_{dc}) that the converter can have with a 15% margin to the highest stationary terminal voltage (grid voltage + max voltage drop over the phase inductances)? Make it clear what modulation method you assume! (3p)

Since this is an Active Filter, the worst case is when the phase current lags the gri2p pd voltage with 90 degrees, and the inductor voltage thus is in phase with the grid voltage.

The maximum phase current, from the rated data is:

$$i_{phase\_rms} = \frac{100000}{\sqrt{3} \cdot 400} = 144\ A$$

If the AF is able to supply 144 A phase current, then the Inductor voltage drop will be

$$|u_L| = \omega \cdot L \cdot i_{phase_{rms}} = 100 \cdot \pi \cdot 1e^{-3} \cdot 144 = 45\ V$$

The highest terminal voltage the converter will have to supply, expressed as a PEAK Phase-to-Phase-voltage and including 15 % margin will be:

$$\widehat{U}_{p-p} = 1.15 \cdot \left(400 + 45 \cdot \sqrt{3}\right) \cdot \sqrt{2} = 777\ V$$

This is the highest instantaneous value of Phase-to-Phase voltage that can occur and thus also the minimum required DC link voltage IF symmetric modulation is used.

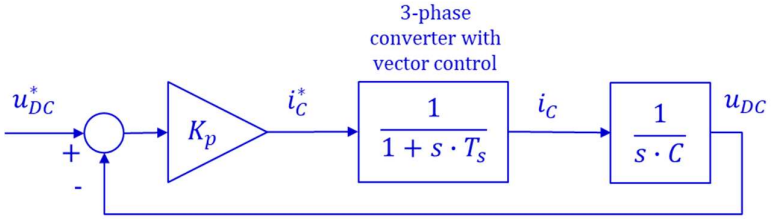
b) Derive a DC link voltage controller and draw the control system as a block diagram from the DC link voltage reference all the way to the 3-phase modulator, including current sensing etc, assuming that the active filter does ONLY control the DC link voltage. (4p)

The charging/discharging of the Capacitor voltage is controlled by the AF that has a limited response time here modelled as a time constant T_s = the current controller sampling time.

The power fed to the DC link capacitor is assumed to be (almost) equal to the power taken from the grid, i.e.:

$$i_C \cdot U_{dc} = -i_q \cdot e_{grid} \rightarrow i_q^* = -\frac{U_{dc}}{e_{grid}} \cdot i_C^*$$

A closed loop control system for the DC capacitor voltage can then be drawn as



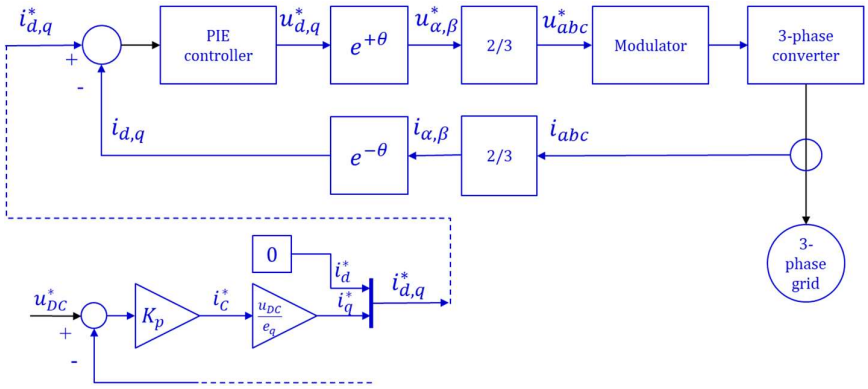
And the gain Kp calculated as:

$$\frac{u_{DC}}{u_{DC}^*} = \frac{K_p \cdot \frac{1}{1+s\cdot T_s} \cdot \frac{1}{s\cdot C}}{1 + K_p \cdot \frac{1}{1+s\cdot T_s} \cdot \frac{1}{s\cdot C}}$$

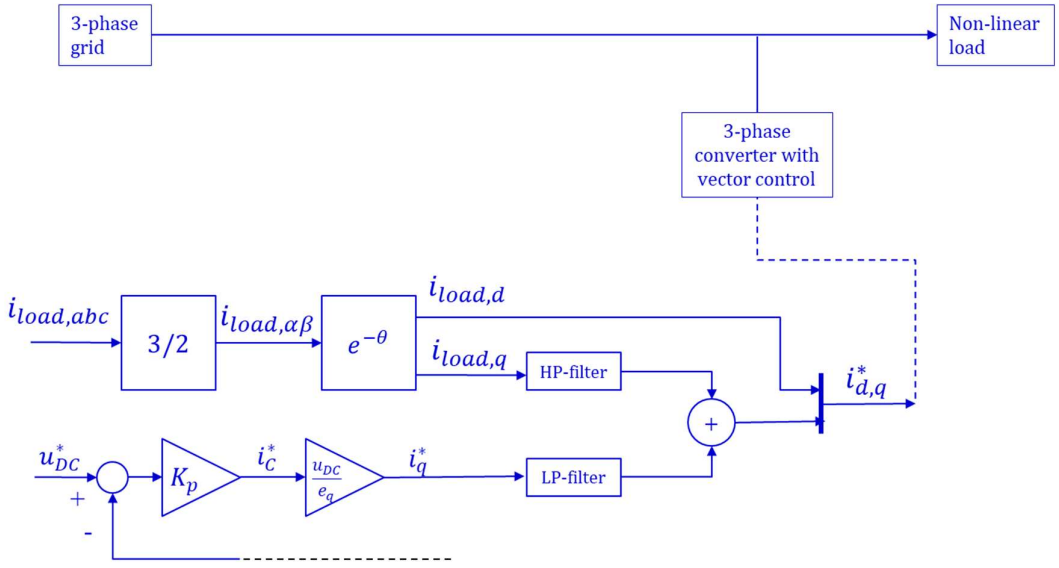
$$= \frac{\frac{K_p}{C\cdot T_s}}{s^2 + s\cdot\frac{1}{T_s} + \frac{K_p}{C\cdot T_s}}$$

$$s^2 + s\cdot\frac{1}{T_s} + \frac{K_p}{C\cdot T_s} = 0 \rightarrow K_p = \frac{C}{4\cdot T_s}$$

Where the Udc-controller feeds the 3-phase converter vector control system like this:



c) Now add the control functions needed for compensation of reactive power, asymmetric load currents and harmonics. Draw a block diagram of the control system of the active filter, assuming a non-linear load to be filtered (not illustrated in the figure). The block diagram should include measurement of the currents drawn by the non-linear load, the transformations needed, the filters needed and the DC link voltage controller from question b), current controllers etc all the way up to the modulator. (3p)



5 3-phase converter, PMSM drive

A 200kW Permanently Magnetized Synchronous Machine is used in a drive train supplied from a 2-level converter with 800V DC link voltage . The inductances along the rotor reference frame axis are different $Lsx \neq Lsy$. The base speed is 3000 rpm and the max speed is 9000 rpm.

a) What is the rated torque of the machine? (2p)

$$T_m = \frac{P_n}{\omega_{base,mech}} = \frac{200000}{3000 \cdot \frac{\pi}{30}} = 637\ Nm$$

b) What is the RMS Phase-to-phase voltage at rated power? (2p)

The base speed is the lowest speed that still require the highest voltage the converter can supply,

$$U_{pp,rms} = \frac{U_{dc}}{\sqrt{2}} = \frac{800}{\sqrt{2}} = 566\ V\ rms$$

c) What is the rated phase current of the machine? (2p)

Assuming unity power factor:

$$P = \sqrt{3} \cdot U_{pp,rms} \cdot I_{phase} \rightarrow I_{phase} = \frac{P}{\sqrt{3} \cdot U_{pp,rms}} = \frac{200000}{\sqrt{3} \cdot 566} = 204\ A$$

d) Write the torque expression in rotor coordinates and describe your interpretation of the terms in the expression, and how they relate to the rotor geometry, rotor permanent magnetization and stator current locus. (2p)

$$T = \psi_{pm} \cdot i_q + (L_d - L_q) \cdot i_d \cdot i_q$$

Depending on the difference between the two inductances, the reluctance torque ($(L_d - L_q) \cdot i_d \cdot i_q$) contributes to the Lorenz torque ($\psi_{pm} \cdot i_q$) depending on the sign of i_d.

e) Explain, in a qualitative sense, what is the best locus for the stator current vector to minimize the amount of current needed for torque production. (2p)

For the terminal voltage and the current to be roughly in phase, i_d must be negative and thus $L_q > L_d$ which is normally the case with PM machines.

---------- Good Luck ! ----------

6 Some formulas:

Power Invariant vector definition:

$$\vec{s} = s_\alpha + j s_\beta = \sqrt{\frac{2}{3}}\left[s_a + s_b e^{j\frac{2\pi}{3}} + s_c e^{j\frac{4\pi}{3}} \right] = \sqrt{\frac{3}{2}} s_a + j \frac{1}{\sqrt{2}} (s_b - s_c)$$