

Power Electronics

Laboratory Preparations #2

Four Quadrant DC-DC Converter

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The four quadrant DC-DC converter - description of the building blocks

The four quadrant DC-DC converter investigated in the laboratory, consists of a diode rectifier (AC-DC), DC link capacitors and two transistor half bridges, see Figure 4. Note that one of the half bridges is based on MOSFET technology and one on IGBT technology. In Figure 4, also snubbers are contained. Furthermore, a circuit used to limit the DC link capacitor inrush current is shown. This circuit is connected in series with the DC link capacitor.

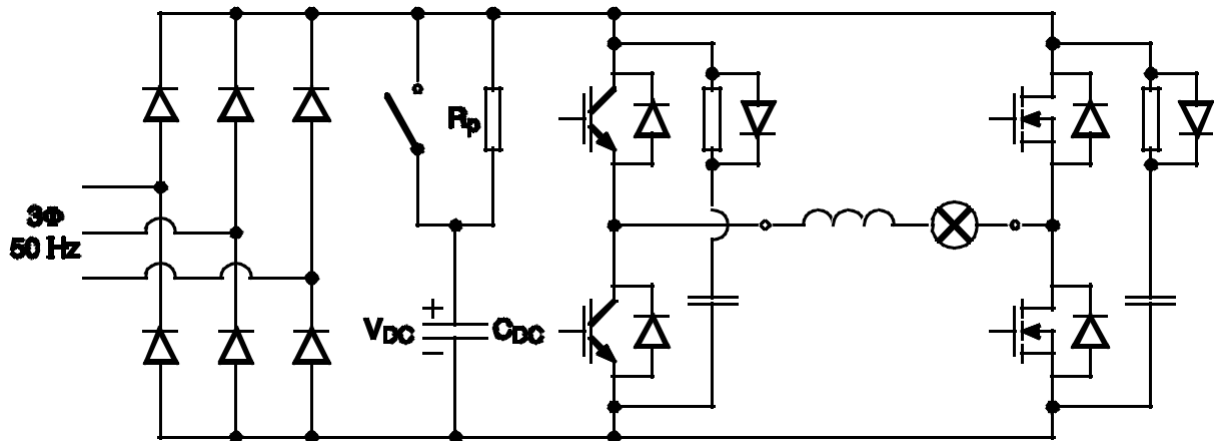


Figure 1 The power electronic main circuit of the converter investigated.

The power electronic main circuit in Figure 4 is connected to the power grid via two transformers. A three phase full transformer is directly connected to the power grid, for two purposes. First, for personal safety (galvanic isolation) and second, for step down transformation to guarantee that the converter DC link voltage is not set too high. This is needed because the DC link voltage is varied with the second transformer, which is a three phase adjustable transformer. A suitable DC link voltage, approximately 200 V, is set with the adjustable transformer.

The converter output voltage reference value is set by an external potentiometer. The pulse width modulated (PWM) output voltage is measured with a differential probe. The measured output voltage together with the load current, which is measured with a current probe, is shown on a two-channel oscilloscope.

All the laboratory set-ups are equipped with a four-channel oscilloscope, which is used for the measurements. For a good practice, it is recommended that only one of the probe ground connections is used, both in order to minimize electronic noise and for personal safety.

A description of the building blocks forming the converter control electronics follows:

Triangle wave generator

The triangle wave generator consists of a Schmitt trigger and an integrator, see Figure 2.

As was studied earlier in the simulation exercise #2, the input-output characteristics of the integrator stage when its output is connected to the input of the Schmitt trigger, is shown in Figure 3 below:

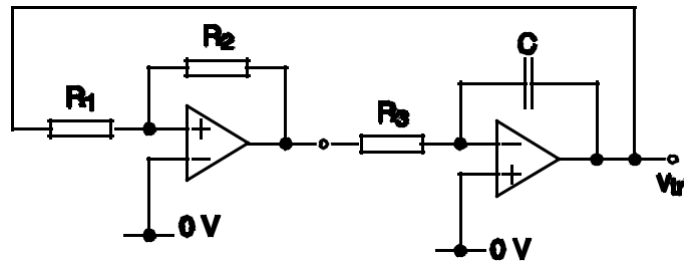


Figure 2 The triangle wave generator.

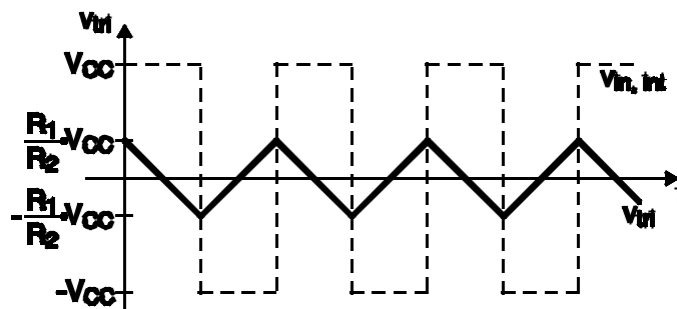


Figure 3 Input and output signal of the integrator.

DC link voltage measurement

In order for the modulator to give the right duty-cycle independent of the DC link voltage, the amplitude of the triangle wave carrier must correspond to half the DC link voltage in control units. Therefore, the DC link voltage has to be measured. This is done with a differential amplifier with a gain 0.05. The output signal from this differential amplifier is fed both to a 12 V zener diode and a circuit labelled AD 633.

AD 633 is a four quadrant (!) analog multiplier, which is used to multiply the output of the triangle wave generator with the output of the differential amplifier. In this way, a triangle wave with amplitude proportional to the DC link voltage is created. The 12 V zener diode at the differential amplifier output starts to conduct when the voltage across it exceeds 12 V, which corresponds to a DC link voltage of 240 V. This in turn triggers the thyristor TY1 thereby biasing the light emitting diode (LED) LD1. When LD1 is conducting, the potential at the anode of TY1 decreases to 2.5-3 V.

The differential amplifier output signal (i.e. the DC link voltage measurement) is also fed to an operational amplifier, U5D, of type LF 347. There, the signal is compared with an adjustable voltage (R18). If the DC link voltage, expressed in control units, is lower than the pre set level then Q1 is off and Q2 is on (conducting). When Q2 is conducting, the LED LD2 is biased and the anode potential of TY1 decreases to 2.5-3 V.

As will be discussed later on, biasing of either LD1 or LD2 corresponds to fault indications. The decreased potential associated with this is also used to signal the drive circuits to inhibit the switching. The difference between triggering of TY1 compared to Q2, is that if Q2 is triggered the fault indication can be reset automatically during operation if the fault condition is resolved. If on the other hand TY1 is triggered, this cannot be reset automatically. This fault indication is reset by closing the breaker S1 which short circuits TY1, causing its anode current to decrease below the hold level.

The reason for dividing the fault indications this way is that TY1 is triggered for DC link over voltage which is regarded as a severe fault condition. Q2 on the other hand is triggered by under voltage, which must be automatically reset, partly due to that this fault is not severe and partly due to the fact that under voltage will be detected during start up.

A power resistor, R_P , in parallel with an electro-mechanical relay, is placed in series with the DC link capacitors, C_{DC} , in order to limit the inrush current. Otherwise, the high voltage derivative exposed to the DC link capacitors results in a high inrush current when the rectifier is connected to the power grid. By connecting a resistor in series with the DC link capacitors this problem is solved. When the DC link voltage has reached a certain level the resistor is short circuited in order not to expose the resistor for an excessive power dissipation.

The triangular wave adapted to the DC link voltage is used for converter pulse width modulation (PWM). Since this is a four quadrant DC-DC converter (i.e. two half bridges), two pulse width modulated signals should be created, one for each half bridge. Two reference values are therefore needed. They are created from one voltage reference value, set by the external potentiometer. One of the reference values for the half bridge is positive while the other is negative. This is achieved by using inverting amplifier with a gain equal to -1 .

The DC-link-voltage-adjusted triangle wave is compared with the reference values in comparators of type LM 311. Note that LM 311 has an internal inverter, according to Figure 4. The comparator output voltage approximately equals $+V_{CC}$ when the triangle wave voltage is lower than the reference value in question. On the contrary, the comparator output voltage equals $-V_{CC}$ when the triangle wave voltage exceeds the reference level in question.

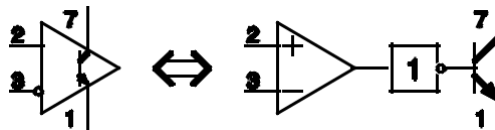


Figure 4 LM311 circuit symbol (left) and its equivalent (right). Note the inverter of the equivalent.

The comparator outputs, PWM1 and PWM2, are pulse width modulated signals. Both of these signals are fed from the modulator printed circuit board (PCB) to one drive circuit PCB each. PWM1 is fed to a ferrite-isolated drive circuit PCB consisting of two drive circuits, one for the upper transistor and one for the lower transistor. In the laboratory set up, the ferrite-isolated drive circuits are used to control the gates of the half bridge consisting of IGBTs. In the same manner PWM2 is fed to an opto-isolated drive circuit PCB, controlling the gates of the MOSFET equipped half bridge.

Usually, the same type of transistors is used throughout the entire converter, i.e. MOSFET and IGBT-technology are not mixed up as in the laboratory set up. Furthermore, the same type of drive circuits is normally used for all the main circuit transistors. However, from a laboratory point of view it is interesting to compare different technologies used in the same circuit.

The drive circuits

Both the ferrite and the opto-isolated drive circuit PCBs have a voltage divider located at their input. These voltage dividers gives two voltage levels, -10 V and $+10$ V, which the PWM signals fed from the modulator, are compared with. Thus, one pulse width modulated signal is compared with two voltage levels in comparators of type LM 311.

This distinction is made since the two transistors of a half bridge, needs one gate control signal each. The reason for selecting ± 10 V is that some immunity to electrical noise is desired. If the drive circuit signal paths are followed it is realized that if the PWM signal is between ± 10 V, both

signal is fed back to the thyristor TY3, via an opto-coupler. When TY3 is triggered the LED LD1 becomes biased, and the strobe inputs of the comparators are forced low resulting in turn-off of all the power transistors of the converter.

This signal path is however fairly long, implying that short circuit detection is not handled fast enough. The base of the push-pull stage complementary transistor pair is also connected to the anode of $T_{y_{sc}}$ and further down to the reference (i.e. ground) level of the drive circuit. This means that the drive circuit detecting short circuit turns off the corresponding power transistor fast.

The diode D_{sc2} is intended to block when the power transistor is in the blocking state to make sure that the drive circuit is not exposed to the power transistor blocking voltage (several hundred volts). This means that D_{sc2} must sustain a voltage at least as high as the DC link voltage. The reason why the current through it should be low when conducting, is that the transition from conducting to blocking should be as fast as possible. In other words it is desired that the reverse recovery time of D_{sc2} is kept short.

The capacitor C_{sc} is needed to capture any voltage pulse resulting from diode D_{sc2} or power MOSFET turn-off, which otherwise would show up across the zener diode and possibly trigger the short circuit protection scheme. C_{sc} is discharged against the reference potential via D_{sc1} .

Ferrite isolated drive circuit

This drive circuit appears to be more complicated than the opto-isolated. This is due to the fact that the ferrite isolated drive circuit not only should transfer the control signal but also the energy needed for power transistor turn-on. For the opto-isolated drive circuit, galvanic isolated DC power supply is needed for each drive circuit, since the opto-couplers can only transfer signals and not energy.

In the circuit scheme of the ferrite isolated drive PCB, the PWM signal is inverted twice following the blanking time circuit. This could have been solved in a simpler way by using a non-inverting buffer circuit instead. The idea of the inverters is, besides the fact that the blanking time circuit must be ended with a logic gate, only to turn the PWM signals right.

After the inverters the PWM signals are mixed with a clock signal of high frequency (3 MHz). The signal mixing is carried out with aid of logic AND and NAND gates. At high control signal level out from the blanking time circuit, the pulses out from the AND and NAND gates have opposite phase. At low control signal out from the blanking time circuit, the AND and NAND gate output signals are instead constant. The output from these gates are fed to one push-pull stage each and further to one ferrite transformer. In series with the transformer primary winding a capacitor is inserted, to prevent from DC magnetising the transformer, which leads to magnetic saturation.

Both diodes connected to the transformer secondary forms a rectifier. Since a transformer can only transfer AC signals, this means that when the output signal of the blanking time circuit is high, the rectifier output will be non-zero. When the blanking time circuit output level is low, the transformer output, and thus the rectifier output, equals zero. At turn-on of the upper IGBT, the gate current will flow through D7 and R17, which is the gate resistor at turn-on. At the IGBT turn-off, the gate current instead flows through Q11 and R18, which consequently is the turn-off gate resistor.

The short circuit protection scheme operates in a way similar to the previously discussed. The zener diode connected across the drive circuit gate-emitter terminals is there to prevent this voltage from exceeding the breakdown voltage during the switching transients. This breakdown voltage is usually around 50 V, but a common recommended maximum level is 20 V. Similar zener diodes are also placed on the opto-isolated drive circuit PCB though not shown in the circuit scheme.

Preparations

Prepare for the laboratory work by doing exercises 1-3 below.

1. Study the circuit schemes and make sure that you understand how the building blocks operate. Draw a block diagram for the converter. The block diagram should consist of triangle wave generator, comparators, blanking time circuits and drive circuits.
2. Estimate the rated power of the converter. In datasheets of power semiconductor devices, it is often stated that they are tested at rated current and for instance 70% of the rated voltage. These tests are carried out in laboratory conditions. In practical applications it can be hard to obtain as good circumstances as in the laboratory because of stray inductance etc. Therefore, somewhat more conservative approach is taken.
In your estimation of the converter rated power consider:
 - Maximum DC link voltage to be equal to 60% of the rated maximum voltage, for the device with the lowest rated voltage.
 - Maximum load current to be equal to 80% of the rated value for the power device with the lowest rated current.Note that there are several maximum current specifications for example max., cont. etc. Note that they are temperature dependent. The temperature we consider is 125 °C. Make sure you use the right one.
3. Estimate the converter losses for the worst case load condition with the converter rating you have determined above. Use the losses calculated to select a suitable thermal resistance for a suitable heat sink. Hint: Assume that the converter operates at rated current with a duty-cycle equal to 0.95. The data of the semiconductors are found in the appendix. The workflow is given below:
 - The losses of the three-phase rectifier bridge are found from Fig. 3b of the datasheet.
 - The conduction losses of the IGBT are found from Fig. 11 (125 °C) of the datasheet together with equation (6.8) in the textbook.
 - The switching losses of the IGBT are found in Fig. 2 or Fig. 3 in the data sheet. Use equations (6.11) and (6.12) to scale the losses.
 - The on-state losses of the IGBT freewheeling diode are found from Fig. 17 of the datasheet and equation (6.13) of the textbook.
 - The turn-off losses of the IGBT freewheeling diode are found from Fig. 18 of the datasheet and equation (6.18) of the textbook.
 - The on-state resistance of the MOSFET is found from Fig. 5 (125 °C) of the datasheet. The on-state voltage and losses are calculated according to equations (6.5) and (6.8) of the textbook.
 - To calculate the switching losses of the MOSFET use the current rise- and fall-times (t_r and t_f) under Characteristics on the first page of the datasheet.

- The on-state losses of the MOSFET freewheeling diode are found from Fig. 11 of the datasheet and equation (6.13) of the textbook.
- The turn-off losses of the MOSFET freewheeling diode are not specified in the datasheet. Use Q_{rr} of the MOSFET (Fig. 12) and the snappiness factor $S=1/3$ for the IGBT diode to calculate Q_f (equation (6.16)) for the MOSFET. Then use equation (6.17) to estimate the losses.
- Summarize your results in a table format for ease of reading and visualization.
- For thermal management calculations use the workflow specified on pages 242-244 of the textbook. The thermal resistances for the power semiconductor devices are found on the first page of each datasheet. Assume an ambient temperature of 40 °C.

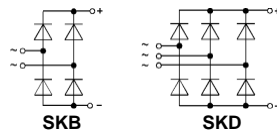
The report should contain

- A block diagram for the converter circuit.
- A detailed description of the four quadrant DC-DC converter, both the power electronic main circuit and the control electronics. The following items must be thoroughly explained:
 1. Between which frequencies can the triangular wave be varied?
 2. Why each drive circuit is equipped with two gate resistors?
 3. Explain the operation of the blanking time circuit. Determine the minimum and maximum blanking time obtainable. How long are the set blanking times? According to the datasheets, what do you think is a suitable value?
 4. Explain the operation of the short circuit protection scheme for the opto-isolated drive circuit.
 5. Estimate nominal DC link voltage and load current for the laboratory converter.
 6. Calculate the converter losses and determine a suitable heat sink (i.e. thermal resistance).

Datasheets and schematics for the laboratory exercise

Power Bridge Rectifiers

SKB 50
SKD 50



Features

- Isolated metal case with screw terminals
- Blocking voltage to 1600 V
- High surge current
- SKB = single phase bridge rectifier
- SKD = three phase bridge rectifier
- Easy chassis mounting

Typical Applications

- Single and three phase rectifiers for power supplies
- Input rectifiers for variable frequency drives
- Rectifiers for DC motor field supplies
- Battery charger rectifiers

V _{RSM} V _{RRM} V	I _D (T _{case} = . . .)			
	50 A (64 °C)		50 A (92 °C)	
	Types	R _{min} Ω	Types	R _{min} Ω
200	SKB 50/02 A3	0,1	SKD 50/02 A3	0,1
400	SKB 50/04 A3	0,3	SKD 50/04 A3	0,2
800	SKB 50/08 A3	0,4	SKD 50/08 A3	0,4
1200	SKB 50/12 A3	0,6	SKD 50/12 A3	0,6
1400	SKB 50/14 A3	0,7	SKD 50/14 A3	0,7
1600	SKB 50/16 A3	0,8	SKD 50/16 A3	0,8

Symbol	Conditions	SKB 50	SKD 50	Units
I _D	T _{amb} = 45 °C; isolated ¹⁾ chassis ²⁾ P1A/120	10 20 34	10 22 40	A A A
I _{DCL}	T _{amb} = 35 °C; P1A/120 F T _{amb} = 45 °C; isolated ¹⁾ chassis ²⁾ P1A/120 T _{amb} = 35 °C; P1A/120 F	47 8 16 29 40	60 10 22 40 60	A A A A A
I _{FSM}	T _{vj} = 25 °C, 10 ms T _{vj} = 150 °C, 10 ms		750 600	A A
i _{2t}	T _{vj} = 25 °C, 8,3...10 ms T _{vj} = 150 °C, 8,3...10 ms		2800 1800	A ² s A ² s
V _F V _(TO) r _T	T _{vj} = 25 °C; I _F = 150 A T _{vj} = 150 °C T _{vj} = 150 °C		1,6 0,85 8	V V mΩ
I _{RD} t _{rr} f _g	T _{vj} = 25 °C; V _{RD} = V _{RRM} T _{vj} = 150 °C; V _{RD} = V _{RRM} T _{vj} = 25 °C		1 10 typ. 10 2000	mA mA μs Hz
R _{thjc} R _{thch} R _{thja}	total total T _{amb} = 35 °C; P1A/120 F isolated ¹⁾ chassis ²⁾ P1A/120	0,65 0,06 0,9 5,7 2,5 1,3	0,45 0,06 0,7 5,5 2,3 1,1	°C/W °C/W °C/W °C/W °C/W °C/W
T _{vj} T _{stg}			- 40...+ 150 - 55...+ 150	°C °C
V _{isol} RC	a.c. 50...60 Hz; r.m.s., 1 s / 1 min P _R =1W		3000 / 2500 50 0,1 50	V~ Ω μF A
F _u M1 M2	to heatsink SI units US units to terminals SI units US units		5± 15% 44± 15% 3± 15% 26± 15%	Nm lb. in. Nm lb. in.
w			250	g
Case		G 14	G 15	

1) Freely suspended or mounted on an insulator

2) Mounted on a painted metal sheet of min. 250 x 250 x 1 mm

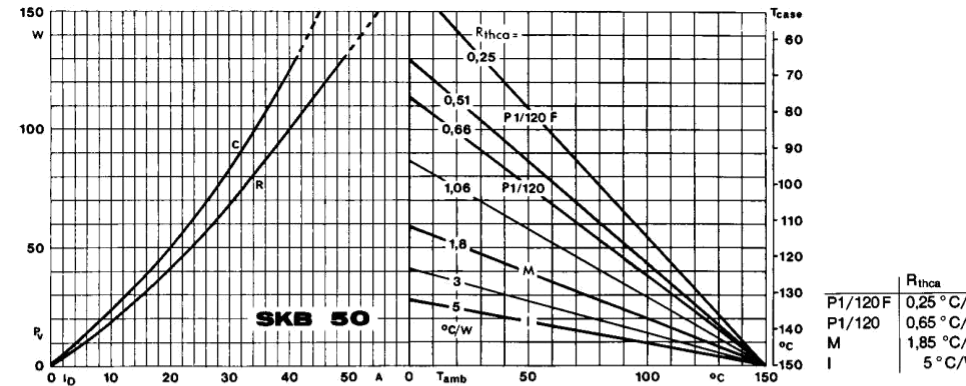


Fig. 3 a Power dissipation vs. output current and case temperature

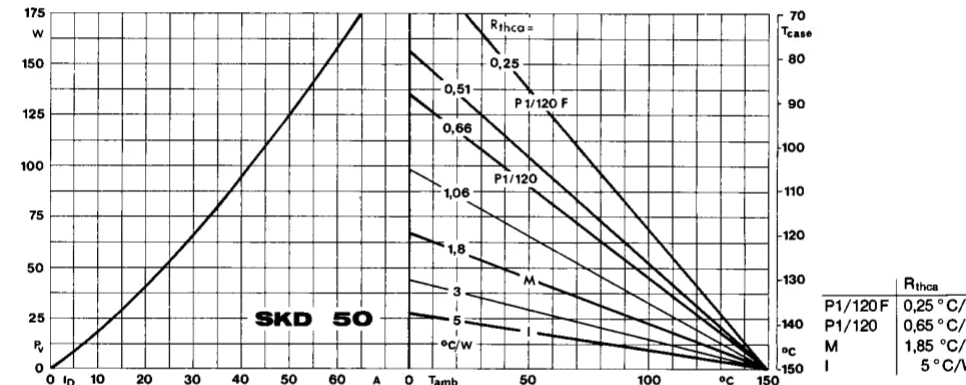


Fig. 3 b Power dissipation vs. output current and case temperature

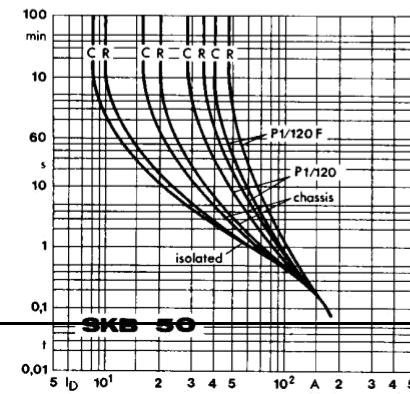


Fig. 6 a Rated overload current vs. time

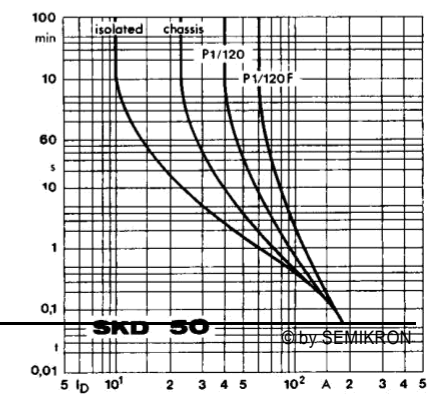


Fig. 6 b Rated overload current vs. time

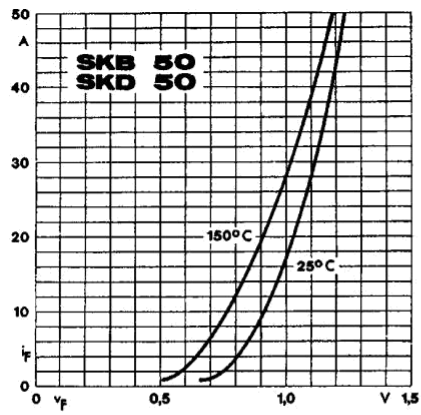
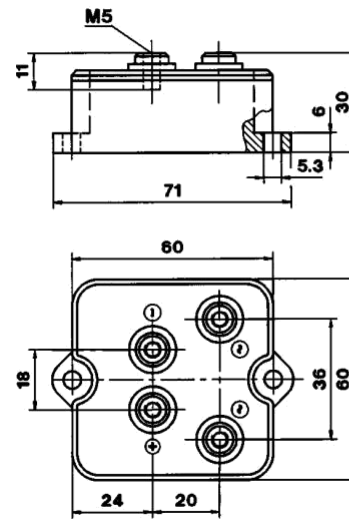


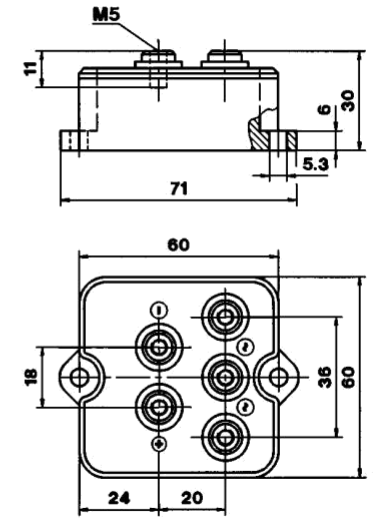
Fig. 9 Forward characteristics of a single diode

SKB 50
Case G 14



Dimensions in mm

SKD 50
Case G 15

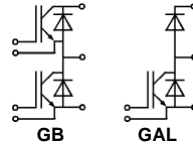


Dimensions in mm

SEMITRANS® M IGBT Modules SKM 50 GB 123 D SKM 50 GAL 123 D



SEMITRANS 2



Features

- MOS input (voltage controlled)
- N channel, Homogeneous Si
- Low inductance case
- Very low tail current with low temperature dependence
- High short circuit capability, self limiting to $6 \cdot I_{nom}$
- Latch-up free
- Fast & soft inverse CAL diodes⁸⁾
- Isolated copper baseplate using DCB Direct Copper Bonding Technology
- Large clearance (10 mm) and creepage distances (20 mm).

Typical Applications: → B 6 - 21

- Three phase inverter drives
- Switching (not for linear use)

- 1) $T_{case} = 25 \text{ °C}$, unless otherwise specified
- 2) $I_F = -I_C, V_R = 600V$,
- $di/dt = 800 \text{ A}/\mu\text{s}$, $V_{GE} = 0 \text{ V}$
- 3) Use $V_{GEoff} = -5 \dots -15 \text{ V}$
- 5) See fig. 2 + 3; $R_{Goff} = 27 \text{ } \Omega$
- 8) CAL = Controlled Axial Lifetime Technology.

Case and mech. data → B 6 - 22 SEMITRANS 2

Absolute Maximum Ratings		Values	Units
Symbol	Conditions ¹⁾	... 123 D	
V_{CES}		1200	V
V_{CGR}	$R_{GE} = 20 \text{ k}\Omega$	1200	V
I_C	$T_{case} = 25/80 \text{ °C}$	50/40	A
I_{CM}	$T_{case} = 25/80 \text{ °C}; t_p = 1 \text{ ms}$	100 / 80	A
V_{GES}		± 20	V
P_{tot}	per IGBT, $T_{case} = 25 \text{ °C}$	310	W
$T_j, (T_{stg})$		- 40 ... +150 (125)	°C
V_{isol}	AC, 1 min.	2 500	V
humidity	DIN 40 040	Class F	
climate	DIN IEC 68 T.1	55/150/56	
Diodes			
$I_F = -I_C$	$T_{case} = 25/80 \text{ °C}$	50/40	A
$I_{FM} = -I_{CM}$	$T_{case} = 25/80 \text{ °C}; t_p = 1 \text{ ms}$	100 / 80	A
I_{FSM}	$t_p = 10 \text{ ms}; \sin.; T_j = 150 \text{ °C}$	550	
I^2t	$t_p = 10 \text{ ms}; T_j = 150 \text{ °C}$	1500	A ² s

Characteristics		min.	typ.	max.	Units
Symbol	Conditions ¹⁾				
$V_{(BR)CES}$	$V_{GE} = 0, I_C = 1 \text{ mA}$	$\geq V_{CES}$	-	-	V
$V_{GE(th)}$	$V_{GE} = V_{CE}, I_C = 2 \text{ mA}$	4,5	5,5	6,5	V
I_{CES}	$V_{GE}=0, T_j = 25 \text{ °C}$	-	0,3	1	mA
I_{GES}	$V_{CE} = V_{CES}, T_j = 125 \text{ °C}$	-	3	-	mA
V_{CESat}	$V_{GE}=20V, V_{CE}=0$	-	-	200	nA
V_{CESat}	$I_C=40A, V_{GE} = 15 \text{ V};$	-	2,5(3,1)	3(3,7)	V
V_{CESat}	$I_C=50A, T_j = 25 (125) \text{ °C}$	-	2,7(3,5)	-	V
g_{fs}	$V_{CE}=20V, I_C=40A$	-	30	-	S
C_{CHC}	per IGBT	-	-	350	pF
C_{ies}	$V_{GE}=0$	-	3300	4000	pF
C_{oes}	$V_{CE}=25V$	-	500	600	pF
C_{res}	$f = 1 \text{ MHz}$	-	220	300	pF
L_{CE}		-	-	30	nH
$t_{d(on)}$	$V_{CC} = 600 \text{ V}$	-	70	-	ns
t_r	$V_{GE}=+15V/-15V$	-	60	-	ns
$t_{d(off)}$	$I_C = 40 \text{ A, ind. load}$	-	400	-	ns
t_r	$R_{Gon} = R_{Goff} = 22 \text{ } \Omega$	-	45	-	ns
$E_{on(5)}$	$T_j = 125 \text{ °C}$	-	7	-	mWs
$E_{off(5)}$		-	4,5	-	mWs
Diodes ⁸⁾					
$V_F = V_{EC}$	$I_F=40A, V_{GE}=0V;$	-	1,85(1,6)	2,2	V
$V_F = V_{EC}$	$I_F=50A, T_j = 25 (125) \text{ °C}$	-	2,0(1,8)	-	V
V_{TO}	$T_j = 125 \text{ °C}$	-	-	1,2	V
r_T	$T_j = 125 \text{ °C}$	-	-	22	mΩ
I_{RRM}	$I_F=40A; T_j = 25 (125) \text{ °C}^{(2)}$	-	23(35)	-	A
Q_{rr}	$I_F=40A; T_j = 25 (125) \text{ °C}^{(2)}$	-	2,3(7)	-	μC
$V_F = V_{EC}$	$I_F=50A, V_{GE}=0V;$	-	-	-	V
$V_F = V_{EC}$	$I_F = 75 \text{ A}, T_j = 25 (125) \text{ °C}$	-	-	-	V
V_{TO}	$T_j = 125 \text{ °C}$	-	-	-	V
r_T	$T_j = 125 \text{ °C}$	-	-	-	mΩ
I_{RRM}	$I_F=50A; T_j = 25 (125) \text{ °C}^{(2)}$	-	-	-	A
Q_{rr}	$I_F=50A; T_j = 25 (125) \text{ °C}^{(2)}$	-	-	-	μC
Thermal Characteristics					
R_{thjc}	per IGBT	-	-	0,4	°C/W
R_{thjc}	per diode	-	-	0,7	°C/W
R_{thch}	per module	-	-	0,05	°C/W

SKM 50 GB 123 D ...

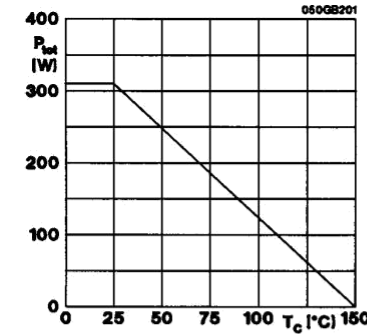


Fig. 1 Rated power dissipation $P_{tot} = f(T_c)$

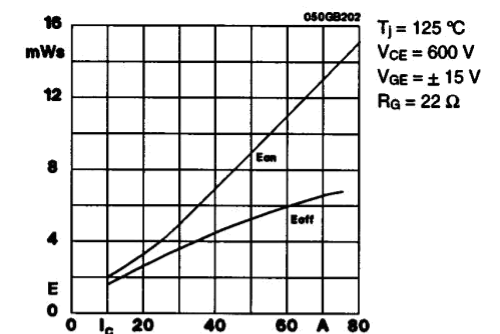


Fig. 2 Turn-on /-off energy $E = f(I_c)$

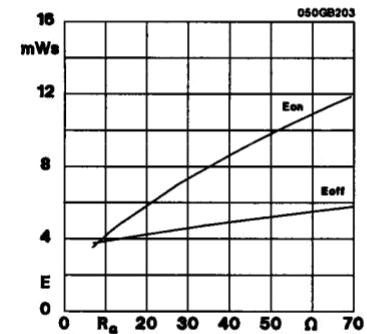


Fig. 3 Turn-on /-off energy $E = f(R_g)$

$T_j = 125 \text{ °C}$
 $V_{CE} = 600 \text{ V}$
 $V_{GE} = \pm 15 \text{ V}$
 $I_C = 40 \text{ A}$

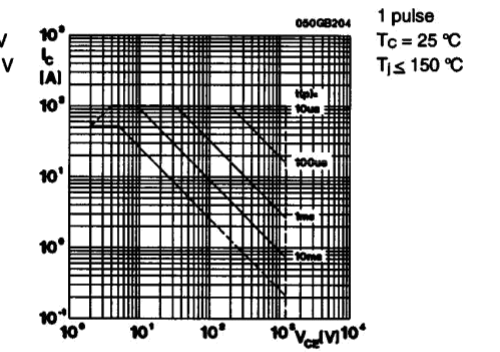


Fig. 4 Maximum safe operating area (SOA) $I_C = f(V_{CE})$

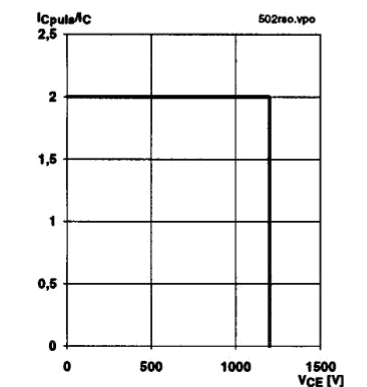


Fig. 5 Turn-off safe operating area (RBSOA)

$T_j \leq 150 \text{ °C}$
 $V_{GE} = \pm 15 \text{ V}$
 $R_{g(off)} = 22 \text{ } \Omega$
 $I_C = 40 \text{ A}$

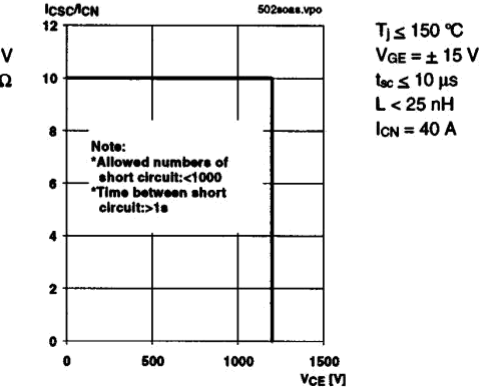


Fig. 6 Safe operating area at short circuit $I_C = f(V_{CE})$

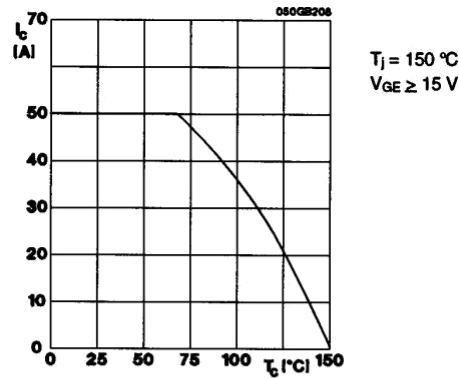


Fig. 8 Rated current vs. temperature $I_c = f(T_c)$

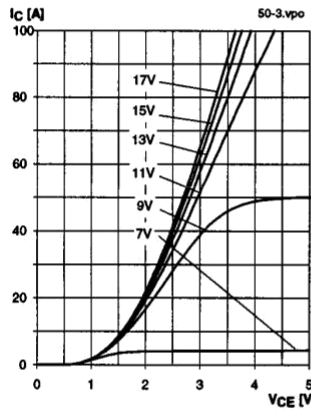


Fig. 9 Typ. output characteristic, $t_p = 80\ \mu\text{s}$; 25°C

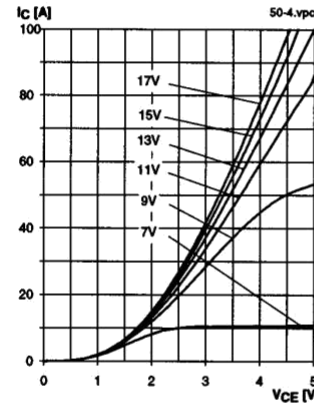


Fig. 10 Typ. output characteristic, $t_p = 80\ \mu\text{s}$; 125°C

$$P_{\text{cond}(t)} = V_{\text{CEsat}(t)} \cdot I_c(t)$$

$$V_{\text{CEsat}(t)} = V_{\text{CE}(T_0)(T_j)} + r_{\text{CE}(T_j)} \cdot I_c(t)$$

$$V_{\text{CE}(T_0)(T_j)} \leq 1,5 + 0,002 (T_j - 25) \text{ [V]}$$

$$r_{\text{CE}(T_j)} = 0,025 + 0,00010 (T_j - 25) \text{ [\Omega]}$$

$$\text{valid for } V_{\text{GE}} = +15 \pm 2 \text{ [V]; } I_c > 0,3 I_{\text{Cnom}}$$

Fig. 11 Typ. saturation characteristic (IGBT)
Calculation elements and equations

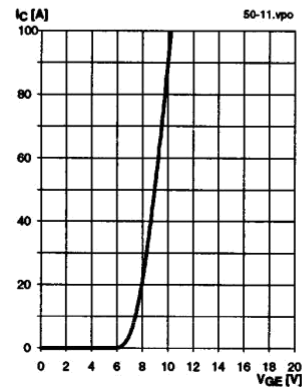


Fig. 12 Typ. transfer characteristic, $t_p = 80\ \mu\text{s}$; $V_{CE} = 20\text{ V}$

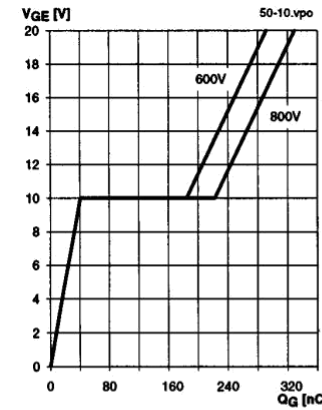


Fig. 13 Typ. gate charge characteristic

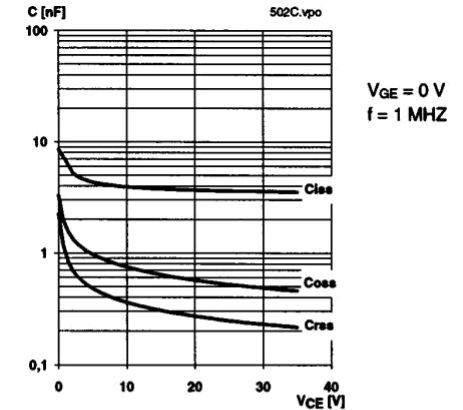


Fig. 14 Typ. capacitances vs. V_{CE}

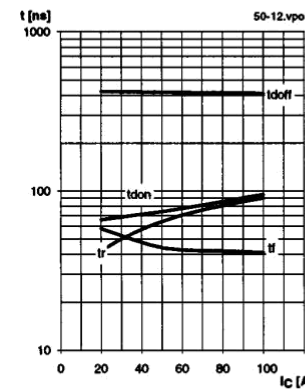


Fig. 15 Typ. switching times vs. I_c

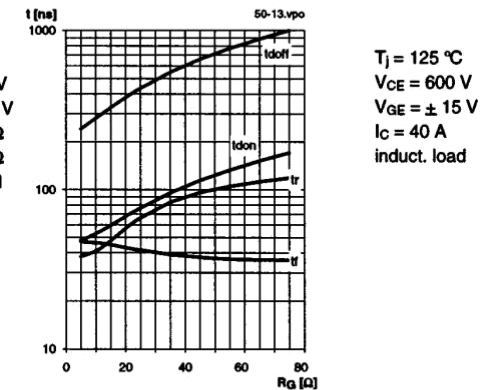


Fig. 16 Typ. switching times vs. gate resistor R_g

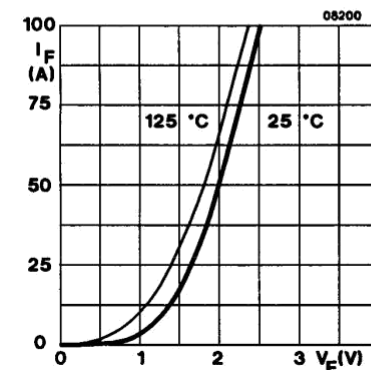


Fig. 17 Typ. CAL diode forward characteristic

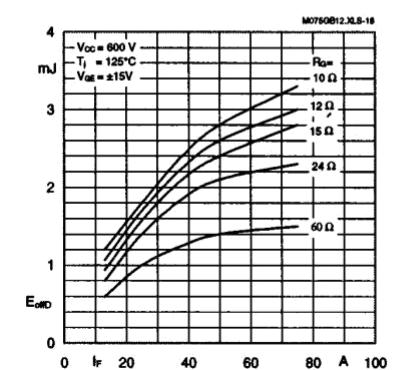


Fig. 18 Diode turn-off energy dissipation per pulse

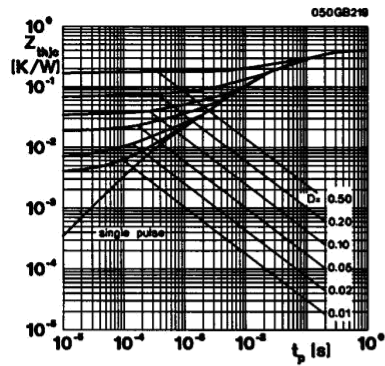


Fig. 19 Transient thermal impedance of IGBT
 $Z_{th(jc)} = f(t_p)$; $D = t_p / t_c = t_p \cdot f$

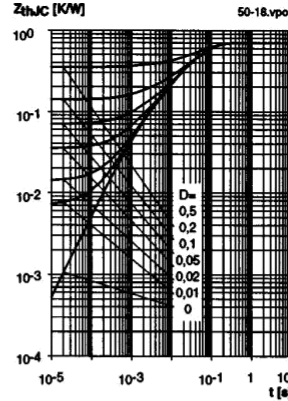


Fig. 20 Transient thermal impedance of inverse CAL diodes
 $Z_{th(jc)} = f(t_p)$; $D = t_p / t_c = t_p \cdot f$

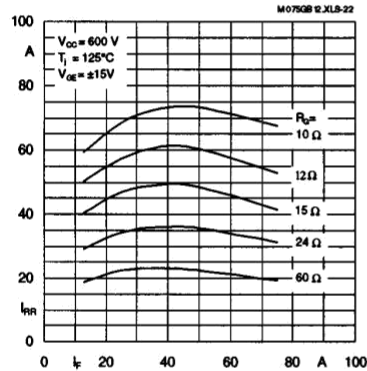


Fig. 22 Typ. CAL diode peak reverse recovery current
 $I_{RR} = f(I_F, R_{\theta})$

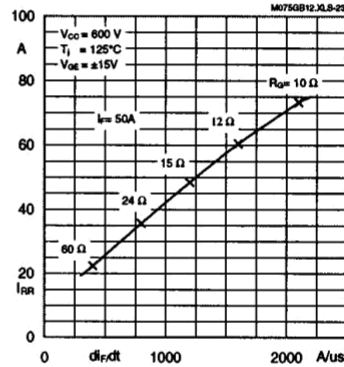


Fig. 23 Typ. CAL diode peak reverse recovery current
 $I_{RR} = f(di_F/dt)$

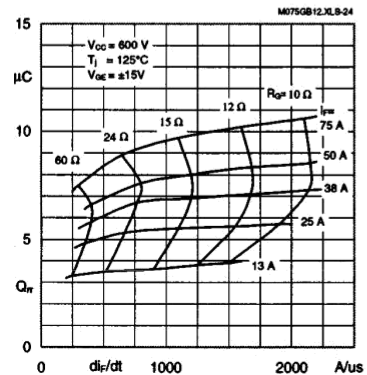


Fig. 24 Typ. CAL diode recovery charge

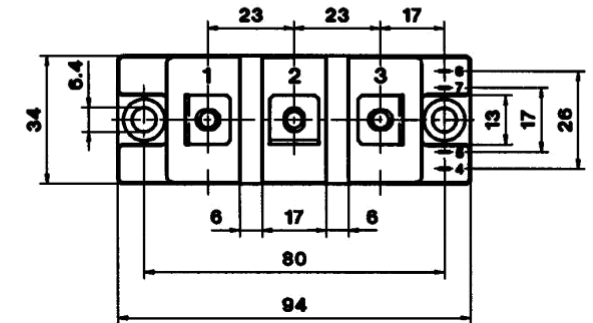
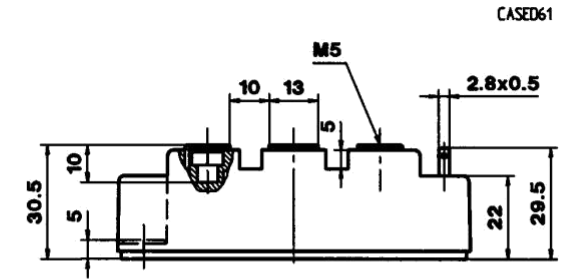
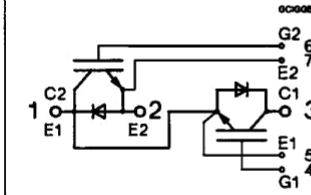
Typical Applications include

- Switched mode power supplies
- DC servo and robot drives
- Inverters
- DC choppers
- AC motor speed control
- Inductive heating
- UPS Uninterruptable power supplies
- General power switching applications
- Electronic (also portable) welders
- Pulse frequencies also above 15 kHz

SKM 50 GB 123 D ...

SEMITRANS 2

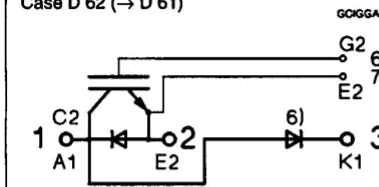
Case D 61
 UL Recognized
 File no. E 63 532
SKM 50 GB 123 D



Dimensions in mm

SKM 50 GAL 123 D

Case D 62 (→ D 61)



Case outline and circuit diagrams

Symbol	Conditions	Values			Units
		min.	typ.	max.	
M ₁	to heatsink, SI Units (M6)	3	-	5	Nm
	to heatsink, US Units	27	-	44	lb.in.
M ₂	for terminals, SI Units (M5)	2,5	-	5	Nm
	for terminals US Units	22	-	44	lb.in.
a		-	-	5x9,81	m/s ²
w		-	-	250	g

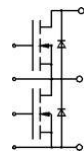
This is an electrostatic discharge sensitive device (ESDS). Please observe the international standard IEC 747-1, Chapter IX.

Eight devices are supplied in one SEMIBOX A without mounting hardware, which can be ordered separately under Ident No. 33321100 (for 10 SEMITRANS 2). Larger packaging units of 20 or 42 pieces are used if suitable. Accessories → page B 6 - 4. SEMIBOX → page C - 1.

SEMITRANS[®] M Power MOSFET Modules SKM 254 F



SEMITRANS 2



Features

- N Channel, enhancement mode
- Fast inverse diodes
- Short internal connections avoid oscillations
- Switching kW's in less than 1 μ s
- Isolated copper baseplate
- All electrical connections on top for easy busbaring
- Large clearances and creepage distances
- UL recognized, file no. E 63 532

Typical Applications

- Switched mode power supplies
- DC servo and robot drives
- DC choppers
- Resonant and welding inverters
- Induction heaters
- AC motor drives
- Laser power supplies
- UPS equipment
- Plasma cutting
- Not suitable for linear amplification

This is an electrostatic discharge sensitive device (ESDS). Please observe the international standard IEC 747-1, Chapter IX.

Screws \rightarrow page B 6 - 4

Absolute Maximum Ratings			
Symbol	Conditions ¹⁾	Values	Units
V _{DS}		500	V
V _{DGR}	R _{GS} = 20 k Ω	500	V
I _D		35	A
I _{DM}		140	A
V _{GS}		± 20	V
P _D		400	W
T _J , T _{stg}		-55 ... +150	$^{\circ}$ C
V _{isol}	AC, 1 min	2 500	V
humidity	DIN 40 040	Class F	
climate	DIN IEC 68 T.1	55/150/56	
Inverse Diode			
I _F = - I _D		35	A
I _{FM} = - I _{DM}		140	A

Characteristics					
Symbol	Conditions ¹⁾	min.	typ.	max.	Units
V _{(BR)DSS}	V _{GS} = 0, I _D = 0,25 mA	500	-	-	V
V _{GS(th)}	V _{GS} = V _{DS} , I _D = 1 mA	2,1	3,0	4,0	V
I _{DSS}	V _{GS} = 0, T _J = 25 $^{\circ}$ C	-	50	250	μ A
	V _{DS} = 500 V, T _J = 125 $^{\circ}$ C	-	300	1000	μ A
I _{GSS}	V _{GS} = 20V, V _{DS} = 0	-	10	100	nA
R _{DS(on)}	V _{GS} = 10V, I _D = 22A	-	140	170	m Ω
g _{fs}	V _{DS} = 25V, I _D = 22A	13	20	-	S
C _{CHC}	per MOSFET	-	-	100	pF
C _{iss}	V _{GS} = 0	-	18	24	nF
C _{oss}	V _{DS} = 25V	-	1,3	1,9	nF
C _{rss}	f = 1 MHz	-	0,48	0,7	nF
L _{DS}		-	-	20	nH
t _{d(on)}	V _{DD} = 250 V	-	60	-	ns
t _r	I _D = 22A	-	30	-	ns
t _{d(off)}	V _{GS} = 10V	-	270	-	ns
t _f	R _{GS} = 3,3 Ω	-	55	-	ns
Inverse Diode					
V _{SD}	I _F = 70A, V _{GS} = 0	-	1,2	1,6	V
t _{rr}	T _J = 25 $^{\circ}$ C ²⁾	-	200	280	ns
	T _J = 150 $^{\circ}$ C ²⁾	-	350	500	ns
Q _{rr}	T _J = 25/150 $^{\circ}$ C ²⁾	-	1,5/8,5	2,5/12	μ C
I _{RRM}	T _J = 25/150 $^{\circ}$ C ²⁾	-	12/28	-	A
Thermal Characteristics					
R _{thjc}	per MOSFET	-	-	0,31	$^{\circ}$ C/W
R _{thch}	per module	-	-	0,07	$^{\circ}$ C/W

Mechanical Data					
M1	to heatsink, SI Units	4	-	5	Nm
	to heatsink, US Units	35	-	44	lb.in.
M2	for terminals, SI Units	2,5	-	3,5	Nm
	for terminals, US Units	22	-	24	lb.in.
a		-	-	5x9,81	m/s ²
w		-	-	250	g
Case	\rightarrow page B 5 - 2			D 70	

¹⁾ T_{case} = 25 $^{\circ}$ C, unless otherwise specified.

²⁾ I_F = - I_D, V_R = 100 V, - di_F/dt = 100 A/ μ s

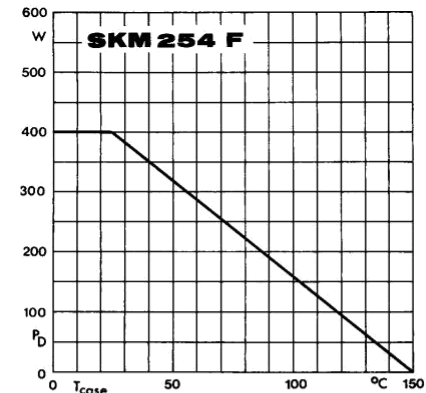


Fig. 1 Rated power dissipation vs. temperature

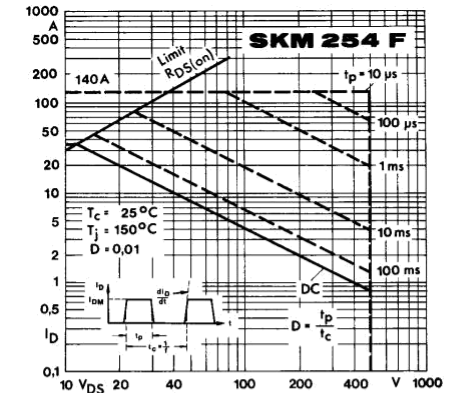


Fig. 2 Maximum safe operating area

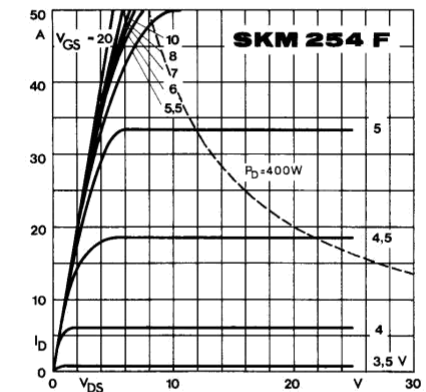


Fig. 3 Output characteristic

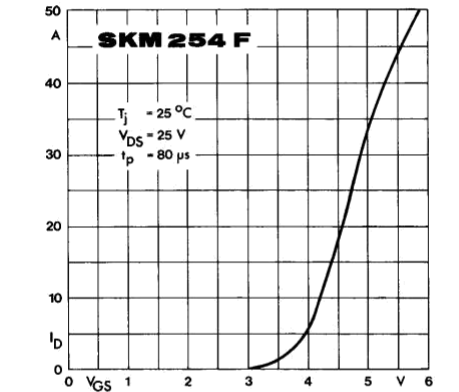


Fig. 4 Transfer characteristic

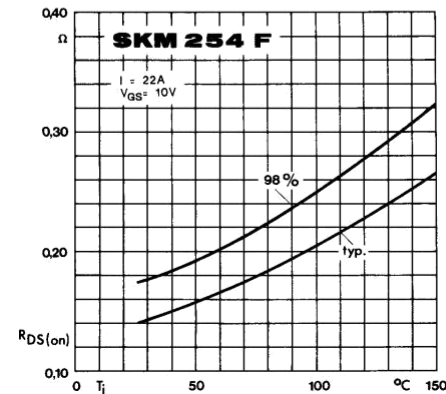


Fig. 5 On-resistance vs. temperature

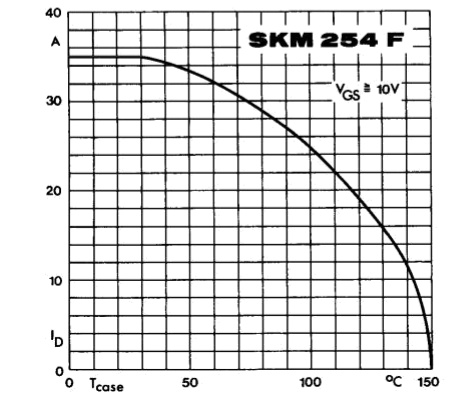


Fig. 6 Rated current vs. temperature

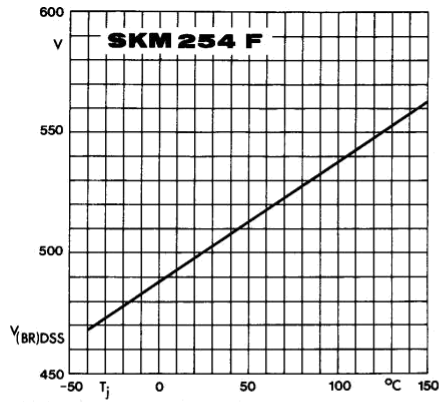


Fig. 7 Breakdown voltage vs. temperature

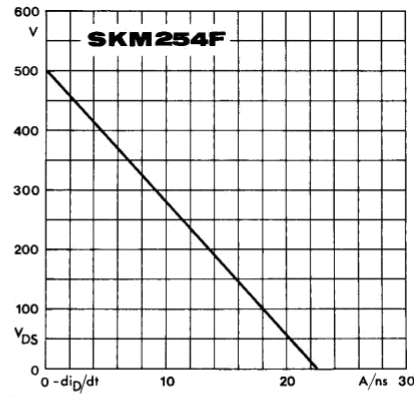


Fig. 8 Drain-source voltage derating

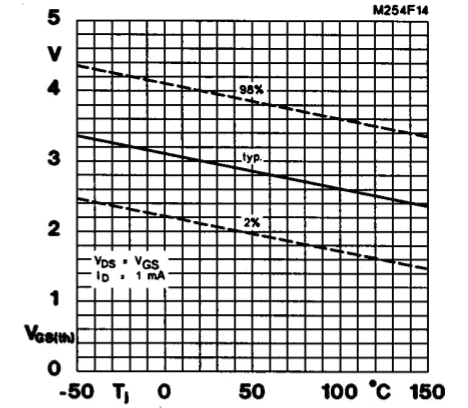


Fig. 14 Gate-source threshold voltage

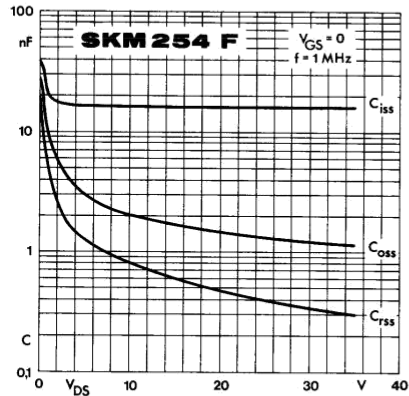


Fig. 9 Capacitances vs. drain-source voltage

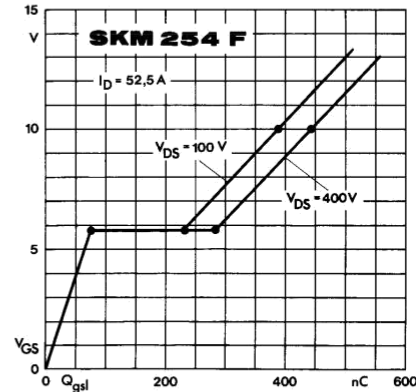


Fig. 10 Gate charge characteristic

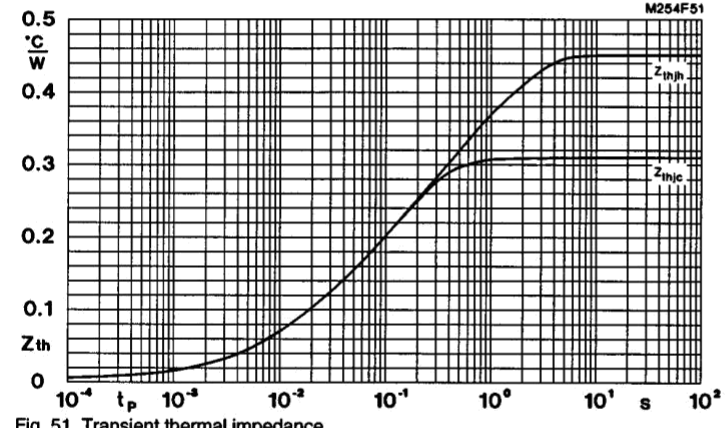


Fig. 51 Transient thermal impedance

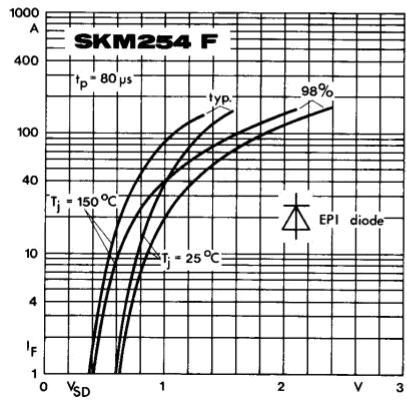


Fig. 11 Diode forward characteristic

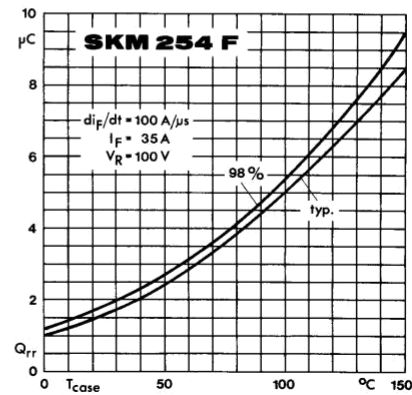


Fig. 12 Diode recovered charge

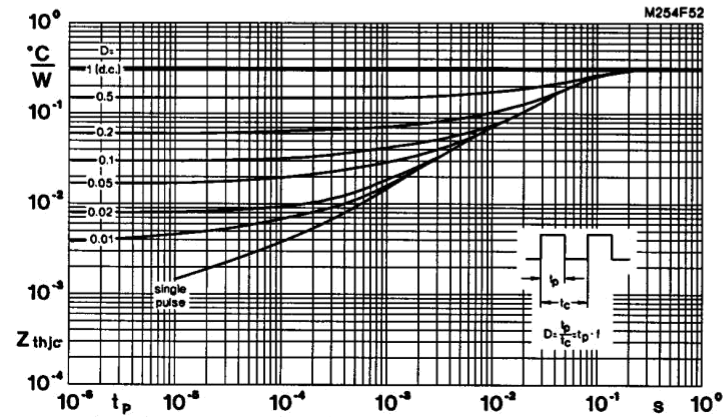
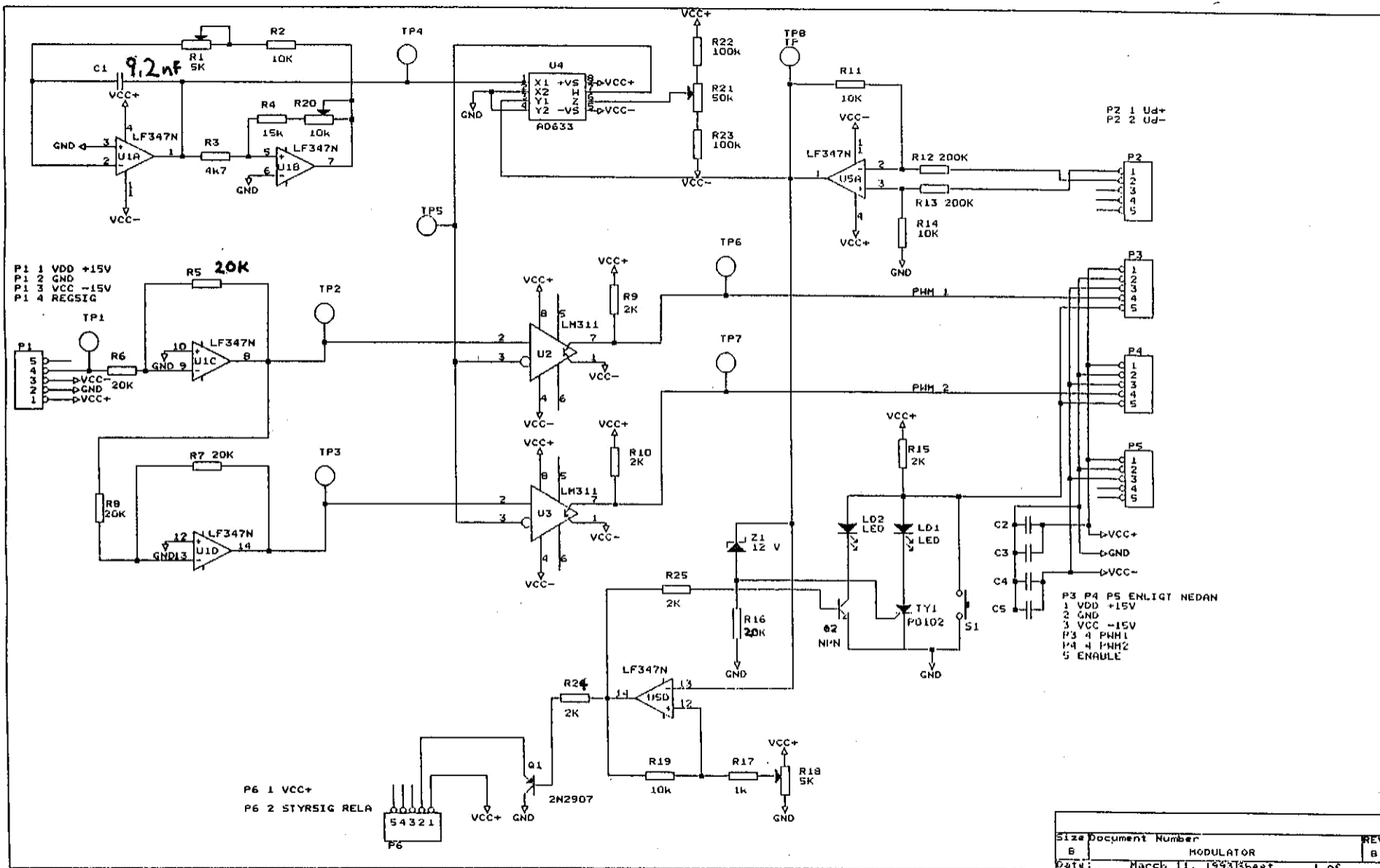


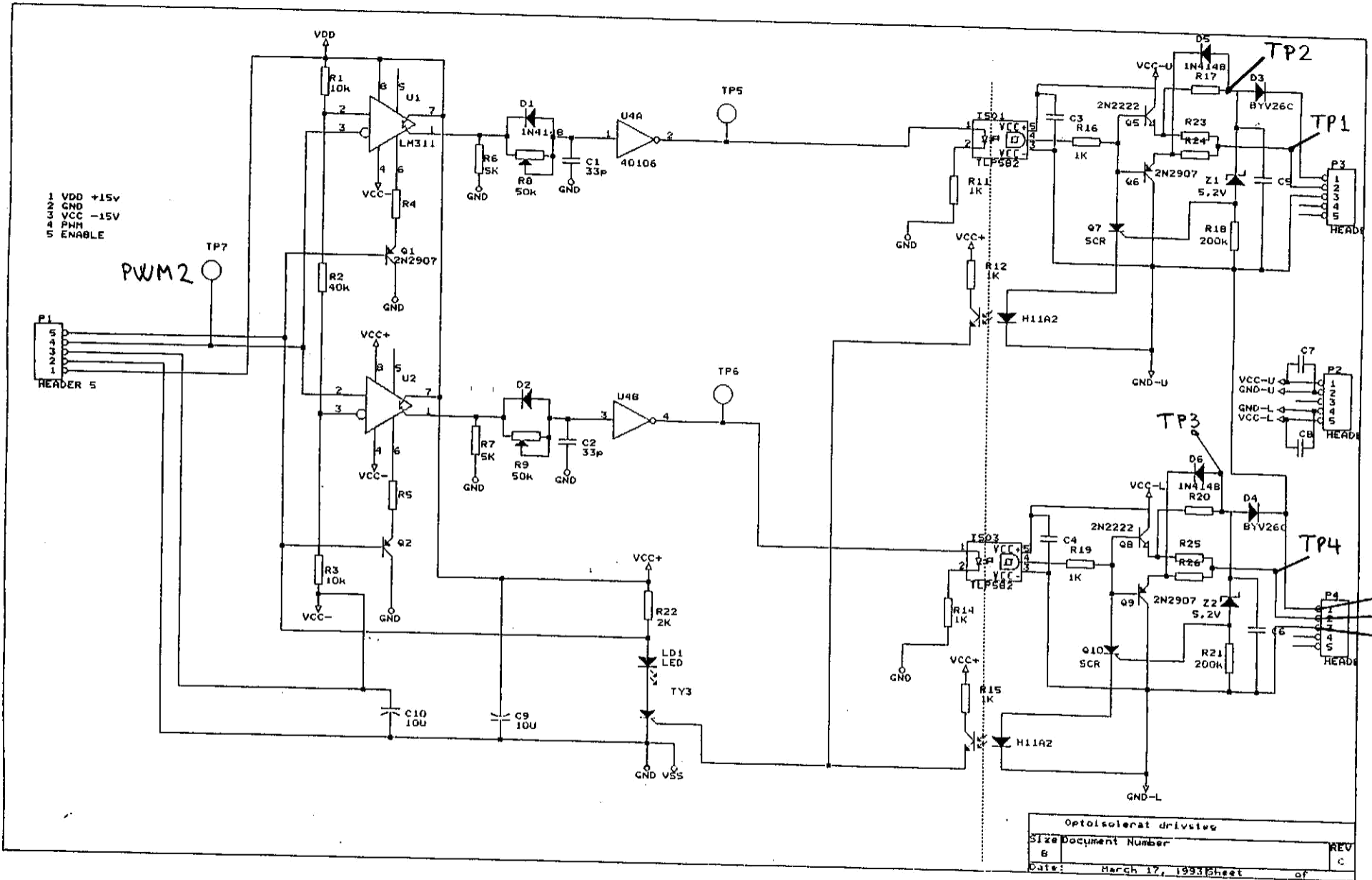
Fig. 52 Thermal impedance under pulse conditions

Appendix B Kretsschema för modulator

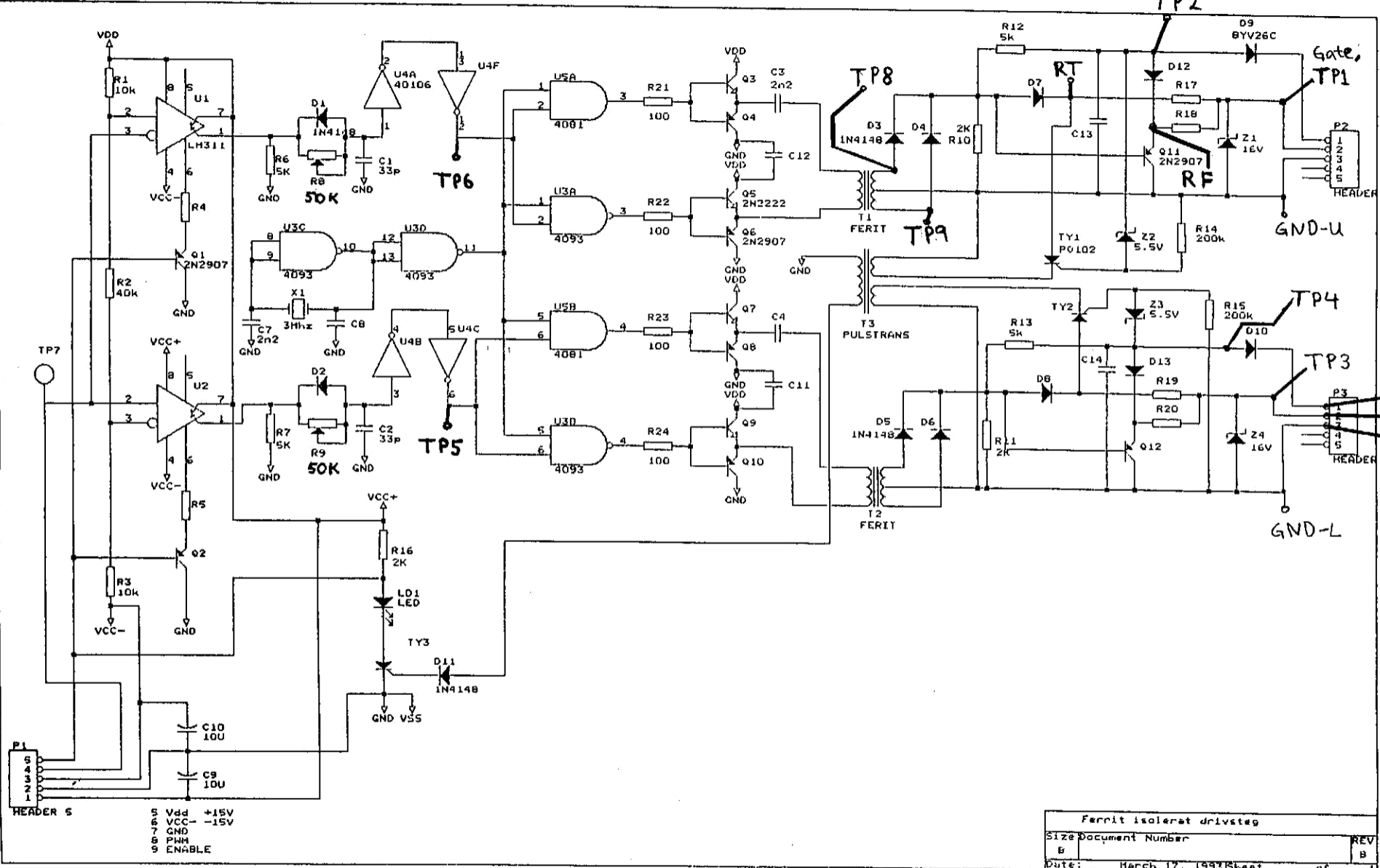


Size Document Number		REV
B	MODULATOR	B
Date:	March 11, 1993	Sheet 1 of 1

Appendix C Kretsschema för optisolerat drivsteg



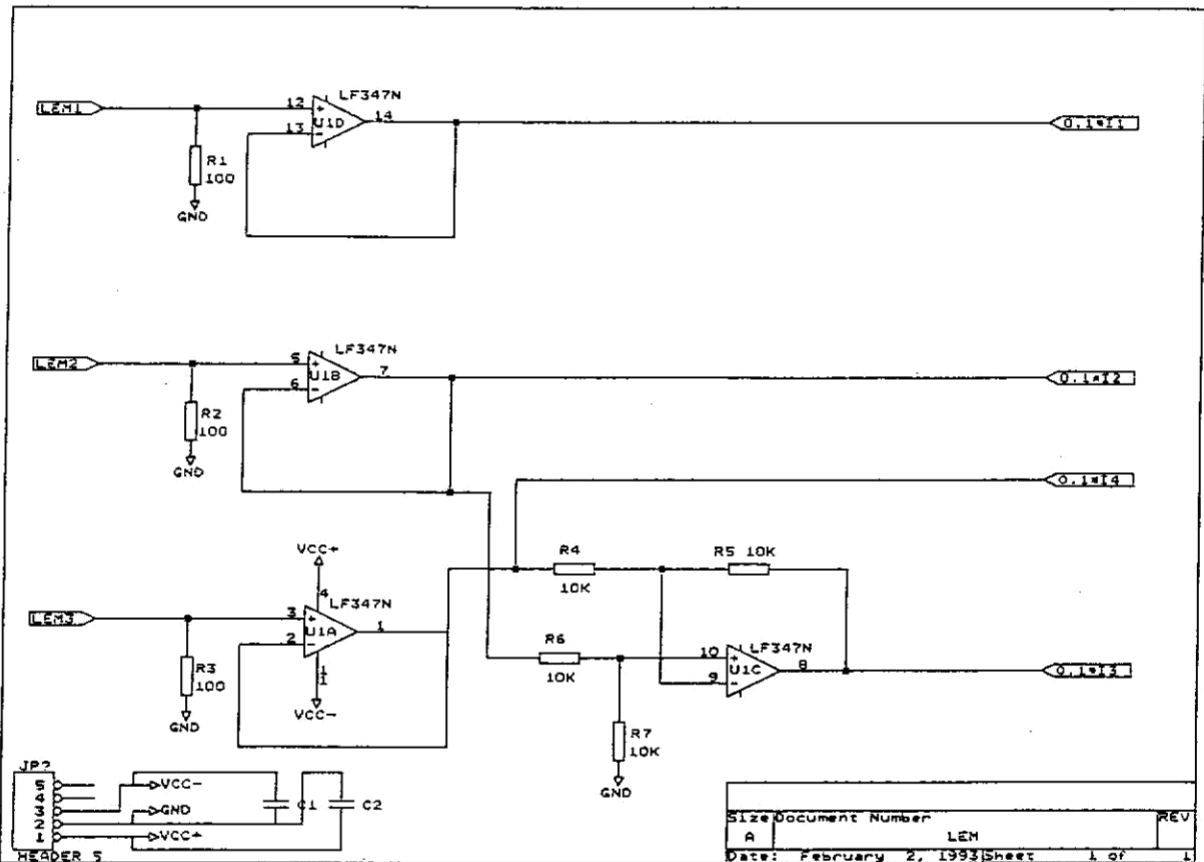
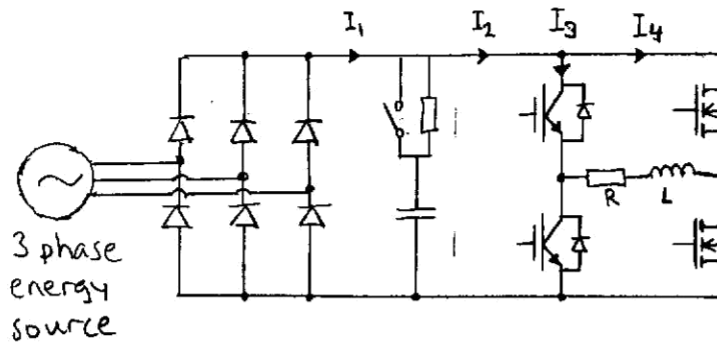
Appendix D Kretsschema för ferritkänneslöserat drivsteg



Collector
Gate
Emitter

Ferrit isolerat drivsteg	
Size	Document Number
B	REV B
Date:	March 17, 1993 Sheet of 1

Appendix E Krettschema för strömmätning med LEM-element



Appendix F Kretsschema för nätaggregat

