CHAPTER 19

HV Direct-Current Transmission

Originally electrical power generation, transmission, and distribution systems were direct current. The advent of the three-phase induction motor and the ability of transformers to converter one ac voltage to another ac voltage level (at the same frequency), saw the unassailable rise to dominance of ac electrical power systems. But for long distance electrical power overhead line transmission, of just a few hundred kilometres of typically about 300 to 550km, a dc transmission system is a viable possibility. For underwater or underground electrical power transmission, ac may not be viable at just 50km due to high capacitive charging currents because of the close proximity of the cables (particularly subsea cables).
The 1980km HVDC link between Xiangjiaba and Shanghai is the largest dc overhead line in the world, with a capacity of 6400MW and a ±800kV DC link voltage.
A Brazilian functional HVDC transmission system is rated at ±600kV on 785km and 805km transmission lines. Each of the two bipolar dc transmission systems carry 3.15GW. Also involved are three, three-phase 765kV ac lines which are 1GVAr variable capacitor series compensated (FACTS) at two intermediate substations.

19.1 HVDC Electrical Power Transmission

Electrical power is generated in ac form and is also usually distributed and consumed in an ac form. Its long distance transmission between these two stages may be an ac or a dc transmission system. In a high-voltage dc (HVDC) system the generated 50/60Hz ac is controlled-rectified to dc, transmitted, then at the receiving end, converted from dc back to 50/60Hz ac. A HVDC system is two ac systems connected by a dc transmission system, where the ac systems can be totally independent.

The dc-link of a HVDC transmission system is either

- a controlled voltage dc-link or
- a controlled current dc-link.

A HVDC controlled *current link* has the following characteristics.

The link in highly inductive, achieved with series inductance at each end.
The converter/inverter technology is operated in a controlled current mode, thus the converter/inverter devices require reverse voltage blocking ability. Symmetrical blocking thyristor devices are applicable, but such devices are restricted to line commutation and phased control.

A HVDC controlled *voltage link* has the following characteristics.

The link in highly capacitive, achieved with parallel connected capacitance at each end.
The converter/inverter technology is operated in a controlled voltage mode, thus the converter/inverter devices can be uni-directional voltage blocking IGBT technology. Since devices are gate commutatable, a switching frequency of kHz's is possible, thus PWM techniques can be employed for harmonic minimisation.

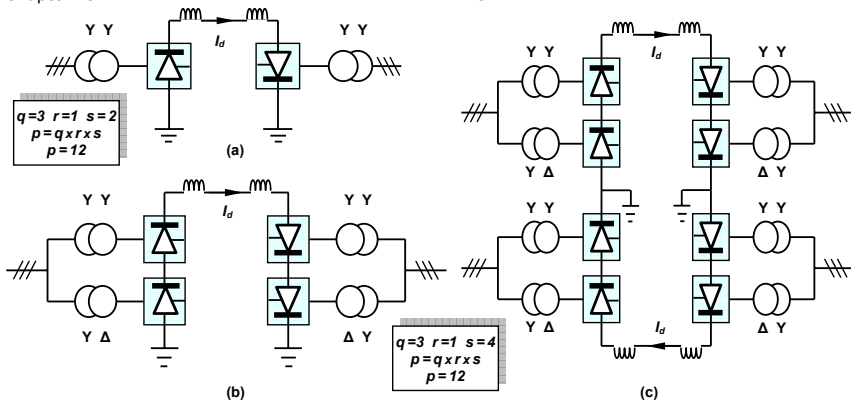


Figure 19.1. *HVDC transmission systems: (a) 6 pulse monopole; (b) 12 pulse monopole; and (c) 12 pulse bipolar, converter bridge configurations.*

19.2 HVDC Configurations

There are a number of different configurations for transmitting dc power, depending on the number of cables employed. Each uses a three-phase fully-controlled thyristor converter (rectifier) coupled through a dc link to another identical three-phase fully-controlled thyristor converter (inverter). Both converters have the same modular structure except the converter connections to the dc link are interchanged for one converter, hence power flow is fully reversible. Since the valves can only conduct current in one direction, power reversal is achieved by changing the polarity of the dc link terminal voltages through control of the converter thyristor firing delay angles. The rectification mode (positive dc link voltage) is achieved with thyristor firing angles of $0 < \alpha < \frac{1}{2}\pi$ while inversion (negative dc link voltage) is achieved with firing angles of $\frac{1}{2}\pi < \alpha < \pi$. Because one converter terminal connection is reversed, a rectifying voltage ($0 < \alpha < \frac{1}{2}\pi$) is opposed by an inverting voltage ($\frac{1}{2}\pi < \alpha < \pi$) – subtractive not additive voltages.

19.2i - Monopole and earth return

The monopole configurations shown in figure 19.1 parts a and b (6 pulse and 12 pulse respectively) use just one transmission cable and earth is used as the negative return. Occasionally, a metal earth return may be used, but importantly any return is at ground potential thus does not need the full transmission voltage insulation. The converter output terminals are reversed relative to one another, as indicated by the direction of the thyristors in the symbol blocks.
Issues involved in using a ground return are

- Electrochemical corrosion of buried metals objects, like pipelines
- Electrode chemical reaction under the sea
- Magnetic field disturbances when the go and return paths become unbalanced

The monopole system is limited in power handling capability, typically 1.5GW above the ground, and 600MW below the ground or under the sea.

19.2ii - Bipolar

In the bipolar arrangement two high voltage conductors, at opposite potentials with respect to ground, are used as shown in figure 19.1c. Any pole imbalance uses an earth return, if a low-voltage metal ground return is not used. The bipolar configuration has a number of advantages over the monopole arrangement.

- Normally no earth-current flows which minimises earth losses and any earth related environmental effects, including minimal corrosion of underground system metal components
- If a fault develops on one pole, the other pole can continue to operate in a monopole arrangement, using the earth as the return path
- For a given power rating, each conductor has half the cross-sectional area of the monopole line, thus reducing the extra cost of using a second conductor
- The same dc transmission line towers can carry two lines with a small additional capital cost

A homopolar hvdc link is formed if the two high voltage conductors have the same polarity, with, undesirably, a high ground or metal return current.
The bipolar system is capable of higher transmission powers than the monopole configuration. Bipolar systems can carry over 3GW at voltages of over ±500kV, over distances well in excess of 1000km.

19.2iii - Tripole
Two of the three conductors of an ac system are used in a bipolar configuration, with the third conductor used as a parallel monopole with bidirectional power flow capability. The bidirectional capability of the third conductor allows each of the two bipolar conductors to carry higher than rated current when each in turn is relieved periodically by the monopole system, such that all three conductors do not exceed rated I^2R losses. In this way each of the three conductors experience the same thermal losses. This is achieved if the bipolar currents are cycled every few minutes between 0.366pu $½\left(\sqrt{3}-1\right)$ and 1.366 pu $½\left(\sqrt{3}+1\right)$, with ±1 pu being appropriately alternated in the monopole. As a result, 80% more power can be transmitted compared with the ac equivalent, using the same conductors, towers, etc. Unlike the ac equivalent, the dc system can be fully loaded without system instability or need for reactive power compensation.

19.2iv - Back-to-back
Two different asynchronous ac systems in close proximity, possibly operating at different frequencies, can be interconnected by either a monopole or bipolar system. Since no dc transmission cables are necessary, because of the close proximity of the two systems, the system type and voltage level are not restrictive.

19.2v - Multi-terminal
More than two converters are connected to the same dc link, where simultaneously, at least one converter operates in the rectification mode and at least one other converter operates in an inversion mode. Mechanical switching of the converter terminals is necessary. The control system is more elaborate than for normal point-to-point transmission and power reversal is affected by current reversal, (as opposed to the usual voltage reversal used in point-to-point transmission).

Current Source converter HVDC transmission systems

The thyristor current source converter approach is well established and its reliability has been proven. Most existing DC transmission systems are based on current source converter technology. HVDC transmission systems based on current source technology can use line-commutated converters LCC or capacitor commutated converters CCC. Fig. 19.2 shows the line and capacitor commutated converter HVDC transmission systems. In the CCC converter case, the series commutation capacitors can be on either side of the line voltage transformers and generate reactive power proportional to the load current. When series capacitors are used on the line side, before the AC filters, the configuration may include parallel reactors and TCSC thyristor valves, forming a Controlled Series Capacitor Converter, CSCC.

The capacitor commutated converter extends the applications of the HVDC transmission systems based on current source converters to systems with a low short circuit ratio. This converter improves system immunity to the risk of commutation failure; replaces the switch capacitors by a combination of fixed capacitors and reactors for filtering purposes only, and reduces transformer rating and size. As a result, the size of the converter station in CCC-HVDC transmission systems is reduced compare to a LCC-HVDC system with the same power rating. The capacitor-commutating converter can be connected to ac systems with a short circuit ratio as low as 1.0 without the need for a synchronous condenser or static synchronous compensator (STATCOM) to provide additional reactive power and can maintain constant voltage at the point of common coupling.

According to IEEE Standard 1204-1997, the system short circuit ratio (SCR) and effective short circuit ratio (ESCR) are defined as:

$$SCR = \frac{S}{P_{dc}}$$

$$ESCR = \frac{S - Q_C}{P_{dc}}$$

where S is the ac system three-phase symmetrical short circuit level in MVA at the converter terminal (ac bus) calculated at rated terminal voltage (1 pu), P_{dc} is the rated dc power of the terminal in MW, and Q_C is the three-phase fundamental MVAr at rated P_{dc} and rated terminal voltage. This includes ac filters and shunt connected reactive power capacitors used to compensate for the reactive power absorbed by the converter. The system strength is classified as follows:

- system is strong if $SCR > 3$ or $ESCR > 2.5$
- system is weak if $3 > SCR > 2$ or $2.5 > ESCR > 1.5$
- system is very weak (very low SCR) if $SCR < 2$ or $ESCR < 1.5$

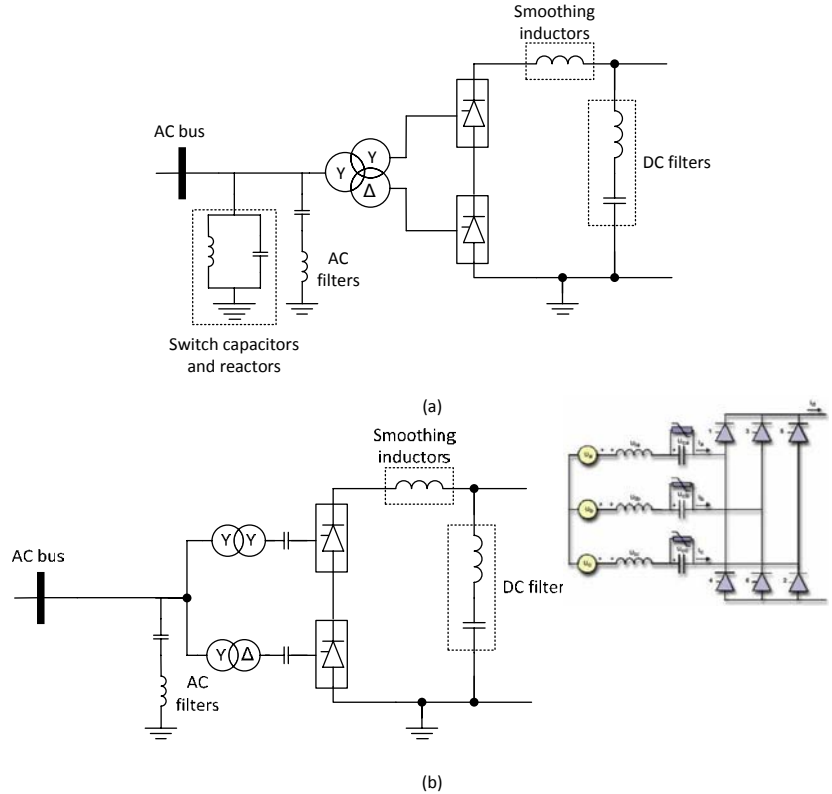


Figure 19.2: *Converter station technologies for the current source based HVDC transmission systems: (a) line commutated high voltage dc (LCC-HVDC) transmission system and (b) series capacitor (valve side) commutated high voltage dc (CCC-HVDC) transmission system.*

19.3 Typical thyristor HVDC transmission system

A fully modular hardware structure is used. The few watts needed for gate power is harvested from thyristor anode level components.

Each 8.8kV symmetrically blocking thyristor is configured in a module with its gate electronics and RC snubber as shown in figure 19.3. Many thyristors are connected in series to form a valve, with internal static voltage sharing resistors and a saturable reactor turn-on snubber as shown in figure 19.3a. The saturable reactor usually incorporates shunt damping to control turn-on current oscillation at saturation.

Six valves are needed to form the 6 pulse valve group converter bridge in figure 19.4a, while 12 valves are used to form the twelve pulse value group converter in figure 19.4b. Each group of four valves in a single vertical stack form quadrivalves as shown in figure 19.4b. Each quadrivalve may contain hundreds of series connected thyristors to give the necessary hundreds of kV pole voltage rating.

Typical six and twelve pulse valve group configurations are shown in figure 19.4, which form the unipolar converters in figure 19.1 parts a and b respectively. A more detailed circuit diagram of the 12-pulse converter and its MOV voltage protection and dc and ac harmonic filtering circuitry, in a substation installation, is shown in figure 19.5. The dc inductors L_{dc} in each pole assist in filtering harmonic currents and smooth the dc side current thereby reducing the current level for the onset of discontinuous current flow. Because the inductors control the dc link side di/dt, converter commutation is more robust. No dc filters may be necessary with the back-to-back HVDC converter configuration.

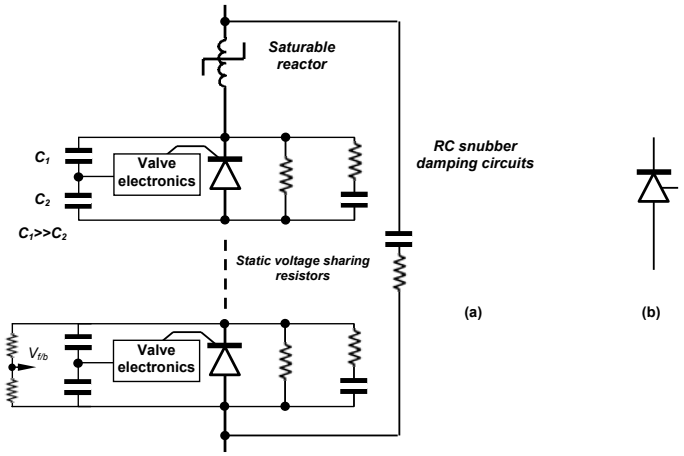


Figure 19.3. *Thyristor valve: (a) modules components assembled into a valve and (b) valve symbol.*

19.4 Twelve-pulse ac line frequency converters

The six-pulse line-frequency fully-controlled thyristor converter was discussed in chapter 12.6. Harmonic filters are required on both the ac and dc side of the converter as shown in figure 19.5. The ac side harmonics occur at 6*n*±1 the fundamental, while the dc side harmonics are generated at 6*n*. To reduce the filtering requirements, and increase the effectiveness of the filtering, on both the ac and dc sides, most high power HVDC systems use 12-pulse, 30° phase-shifted transformer/converter arrangements. The ac side harmonics now occur at 12*n*±1 and the dc components are generated at 12*n*.
Twelve-pulse converter operation is achieved by using the series bridge connection in conjunction with Δ-Y and Y-Y compound connected transformers as shown in figure 19.4b. (A delta connection is usually employed on the lower voltage side of the transformer.) Figure 19.9a shows the arrangement in more detail, with the necessary transformer turns ratio to ensure each converter bridge produces the same output voltage at the same thyristor firing delay angle. Voltage matching between the ac line and required dc link voltage is achieved with the transformer turns ratio *N*, shown in figure 19.9a. The series thyristors in each bridge provide paths which allow both converter currents to be equal.

As a result of the transformer configuration, the corresponding upper and lower transformer voltages are displaced by 30°, where $Va_{Ys\text{-}nY}$ leads $Va_{\Delta s\text{-}n\Delta}$ by $\frac{1}{6}\pi$ radians. The dc-link current I_d is assumed constant because of the large smoothing inductor L_{dc} (linear and typically ½H). If source impedance is neglected, then the various circuit current waveforms are constituted from rectangular current blocks as shown in figure 19.9b. Each converter operates with the same firing delay angle α, with respect to the voltage references shown in figure 19.9b. Because the transformer primaries are in parallel, the input current is the sum of the appropriate two transformer phase currents, namely $i_a = i_{Ya} + i_{\Delta a}$ for phase a. The Fourier series for each transformer primary phase current is obtained from analysis of the appropriate six-pulse converter current, for each converter

$$i_{Ya} = \frac{2\sqrt{3}\,I_d}{N\pi}\left(\cos\theta - \frac{1}{5}\cos 5\theta + \frac{1}{7}\cos 7\theta - \frac{1}{11}\cos 11\theta + \frac{1}{13}\cos 13\theta .....\right) \qquad (19.1)$$

and

$$i_{\Delta a} = \frac{2\sqrt{3}\,I_d}{N\pi}\left(\cos\theta + \frac{1}{5}\cos 5\theta - \frac{1}{7}\cos 7\theta - \frac{1}{11}\cos 11\theta + \frac{1}{13}\cos 13\theta .....\right) \qquad (19.2)$$

Because of the symmetry of a three-phase system, no triplens exist in each input current. The total line current drawn is

$$i_a = i_{Ya} + i_{\Delta a} = \frac{4\sqrt{3}\,I_d}{N\pi}\left(\cos\theta - \frac{1}{11}\cos 11\theta + \frac{1}{13}\cos 13\theta - \frac{1}{23}\cos 23\theta .....\right) \qquad (19.3)$$

The 12-pulse transformer/converter arrangement cancels harmonic components 6×(2*n*-1) ±1.

The line current i_a rms value is $\left(1 + \frac{1}{\sqrt{3}}\right) I_d / N$ and the rms fundamental is $2\sqrt{6}\,I_d / N\pi$.

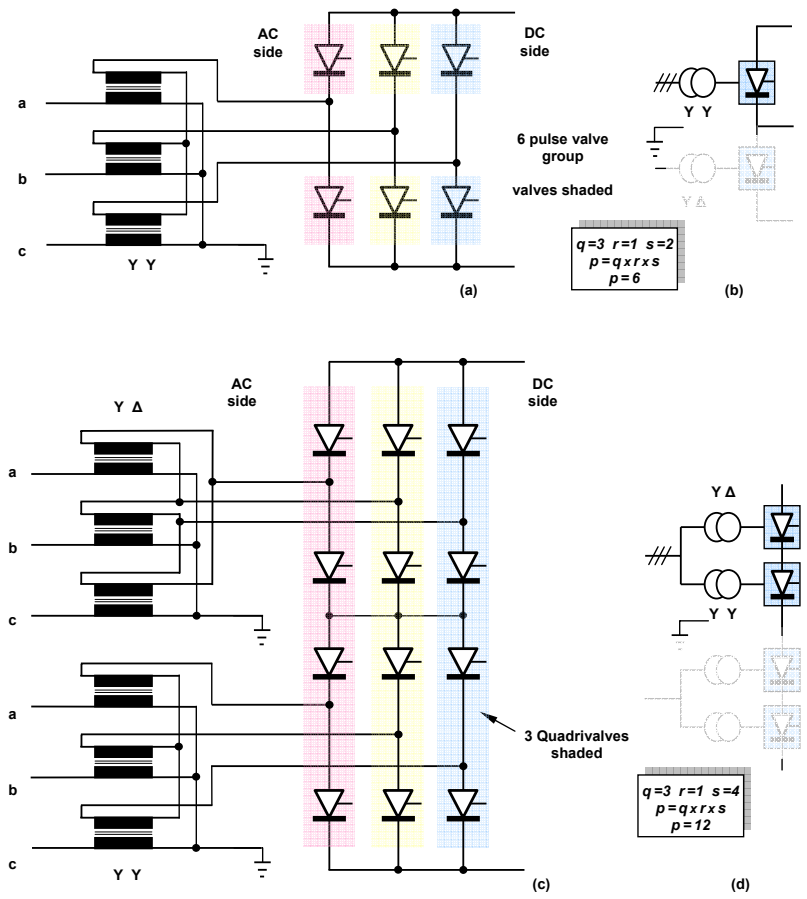


Figure 19.4. *Monopole converter bridges:*
Six-pulse valve group (a) converter bridge schematic and (b) six-pulse valve group converter symbol; Twelve-pulse valve group converter configuration with star-star and star-delta connected converter transformers: (c) converter schematic and (d) twelve-pulse valve group converter symbol.

The ac line current harmonics occur at 12*n*±1. The valve side ac line current, shown as $N\times I_{Ysa}$ (or $N\times I_{\Delta sa}$) in figure 19.9b has an rms value of $I_d\sqrt{2/3}$, and once rectified, the valve unipolar current has an rms value of $I_d/\sqrt{3}$.
More general equations are for the general case of asymmetrical converter firing when $\alpha_1 \neq \alpha_2$. Assuming a turns ratio between the phase windings of the star connected primary and the star connected secondary is 2:1, and the turns ratio between the primary and the delta connected secondary is 2:√3, then

$$i_a = \tfrac{1}{2} i_{Ya} + \tfrac{\sqrt{3}}{2} i_{\Delta a} \qquad (19.4)$$

Due to waveform symmetry, no dc component or even harmonics exist.

The Fourier coefficients a_{nY} and b_{nY} of i_{Ya} (= a_{nY} + j b_{nY}) are

$$a_{nY} = \frac{1}{\pi}\int_0^{2\pi} i_a(t)\cos n\omega t\, d\omega t = \frac{1}{\pi}\left[\int_{\frac{\pi}{6}+\alpha_1}^{\frac{5\pi}{6}+\alpha_1} I_d \cos n\omega t\, d\omega t - \int_{\frac{7\pi}{6}+\alpha_1}^{\frac{11\pi}{6}+\alpha_1} I_d \cos n\omega t\, d\omega t\right] \tag{19.5}$$

$$= -\frac{4I_d}{n\pi}\sin\frac{n\pi}{3}\sin n\alpha_1 \qquad n = 1, 3, 5, \ldots$$

$$b_{nY} = \frac{1}{\pi}\int_0^{2\pi} i_a(t)\sin n\omega t\, d\omega t = \frac{1}{\pi}\left[\int_{\frac{\pi}{6}+\alpha_1}^{\frac{5\pi}{6}+\alpha_1} I_d \sin n\omega t\, d\omega t - \int_{\frac{7\pi}{6}+\alpha_1}^{\frac{11\pi}{6}+\alpha_1} I_d \sin n\omega t\, d\omega t\right] \tag{19.6}$$

$$= \frac{4I_d}{n\pi}\sin\frac{n\pi}{3}\cos n\alpha_1 \qquad n = 1, 3, 5, \ldots$$

The Fourier coefficients $a_{n\Delta}$ and $b_{n\Delta}$ of the delta winding current $i_{\Delta a}$ (= $a_{n\Delta}$ + j $b_{n\Delta}$) are

$$a_{n\Delta} = \frac{1}{\pi}\int_0^{2\pi} i_a(t)\cos n\omega t\, d\omega t$$

$$= \frac{2}{\pi}\left[\int_{0+\alpha_2}^{\frac{\pi}{3}+\alpha_2} \frac{I_d}{3}\cos n\omega t\, d\omega t + \int_{\frac{\pi}{3}+\alpha_2}^{\frac{2\pi}{3}+\alpha_2} \frac{2I_d}{3}\cos n\omega t\, d\omega t + \int_{\frac{2\pi}{3}+\alpha_2}^{\pi+\alpha_2} \frac{I_d}{3}\cos n\omega t\, d\omega t\right] \tag{19.7}$$

$$= \frac{2I_d}{3n\pi}\left[-\sin n\alpha_2 - \sin n(\frac{\pi}{3}+\alpha_2) + \sin n(\frac{2\pi}{3}+\alpha_2) + \sin n(\pi+\alpha_2)\right]$$

$$b_{n\Delta} = \frac{1}{\pi}\int_0^{2\pi} i_a(t)\sin n\omega t\, d\omega t$$

$$= \frac{2}{\pi}\left[\int_{0+\alpha_2}^{\frac{\pi}{3}+\alpha_2} \frac{I_d}{3}\sin n\omega t\, d\omega t + \int_{\frac{\pi}{3}+\alpha_2}^{\frac{2\pi}{3}+\alpha_2} \frac{2I_d}{3}\sin n\omega t\, d\omega t + \int_{\frac{2\pi}{3}+\alpha_2}^{\pi+\alpha_2} \frac{I_d}{3}\sin n\omega t\, d\omega t\right] \tag{19.8}$$

$$= \frac{2I_d}{3n\pi}\left[\cos n\alpha_2 + \cos n(\frac{\pi}{3}+\alpha_2) - \cos n(\frac{2\pi}{3}+\alpha_2) - \cos n(\pi+\alpha_2)\right]$$

$$n = 1, 3, 5, \ldots$$

The Fourier coefficients for the line current are then defined by

$$a_n = ½a_{nY} + ½a_{n\Delta}$$
$$b_n = ½b_{nY} + ½b_{n\Delta} \tag{19.9}$$

From which the input line current is defined by

$$i_a(t) = \sum_{n=1,2,3,\ldots}^{\infty} \sqrt{2}\, I_{an}\sin(n\omega t + \varphi_n) \tag{19.10}$$

Output voltage

The converter outputs are series connected, hence the output voltage is additive for each pole, namely $V_{dr} = V_{dr1} + V_{dr2}$. The converter output voltage, with the constraint that both converters have a trigger delay of α, is

$$V_{dr} = V_{dr1} + V_{dr2} = \frac{6\sqrt{2}}{\pi N}V_{LL}\cos\alpha = 2.70\frac{V_{LL}}{N}\cos\alpha \tag{19.11}$$

The peak output voltage occurs midway between the peak voltage from each converter, and for $\alpha = 0$

$$\hat{V}_{dr} = 2\sqrt{2}\,\frac{V_{LL}}{\pi N}\cos 15° = 1.932\sqrt{2}\,\frac{V_{LL}}{\pi N} \tag{19.12}$$

Each converter delivers six current blocks of magnitude I_d, comprised of two ⅔π current blocks π radians apart in each converter arm. Since each converter output is the same but shifted by $\frac{1}{6}$π radians, provided the two converters have equal delay angles, the resultant 12 current block per cycle results in the dc side voltage harmonics in V_{dr} being of the order 12n.

If the two delay angles are controlled individually, the two outputs add but with harmonic components given by two six pulse converter, displaced by $\frac{1}{6}$π, where

$$V_{dr1} = \frac{3V_{max}}{\pi}\left(\cos\alpha_1 + \sum_{n=1}^{\infty}\sqrt{\frac{1}{(6n-1)^2} + \frac{1}{(6n+1)^2} - \frac{2\cos 2\alpha_1}{(6n-1)(6n+1)}}\sin\left(6n\omega t + \lambda_{6n1}\right)\right)$$
$$V_{dr2} = \frac{3V_{max}}{\pi}\left(\cos\alpha_2 + \sum_{n=1}^{\infty}\sqrt{\frac{1}{(6n-1)^2} + \frac{1}{(6n+1)^2} - \frac{2\cos 2\alpha_2}{(6n-1)(6n+1)}}\sin\left(6\left(n\omega t - ⅙\pi\right) + \lambda_{6n2}\right)\right) \tag{19.13}$$

where

$$\lambda_{6n1} = -n\pi + \tan^{-1}\left[\frac{\frac{\cos(6n+1)\alpha_1}{(6n+1)} - \frac{\cos(6n-1)\alpha_1}{(6n-1)}}{\frac{\sin(6n+1)\alpha_1}{(6n+1)} - \frac{\sin(6n-1)\alpha_1}{(6n-1)}}\right]$$

$$\lambda_{6n2} = -n\pi + \tan^{-1}\left[\frac{\frac{\cos(6n+1)\alpha_2}{(6n+1)} - \frac{\cos(6n-1)\alpha_2}{(6n-1)}}{\frac{\sin(6n+1)\alpha_2}{(6n+1)} - \frac{\sin(6n-1)\alpha_2}{(6n-1)}}\right]$$

When the two delays angles differ, $\alpha_1 \neq \alpha_2$, the output voltage harmonics occur at order 6n.

The dc link ripple current depends on the total dc link inductance L_T and the ripple magnitude varies with the rectifier and inverter converter firing angles, α_r and α_i. Provided the minimum link current is greater than the ripple magnitude, each 12-pulse converter contributes a component given by

$$I_{d\min} > I_{d\,ripple} = \frac{3}{\pi}\frac{\sqrt{2}\,V_{LL}}{\omega L_T}0.023\sin\hat{\alpha}$$

The total ripple current is the sum of the connected converter component. Each converter can be operating at a different frequency, ω, be connected to different line voltages V_{LL}, and be operating in different modes so is operating at different delay angles, α.

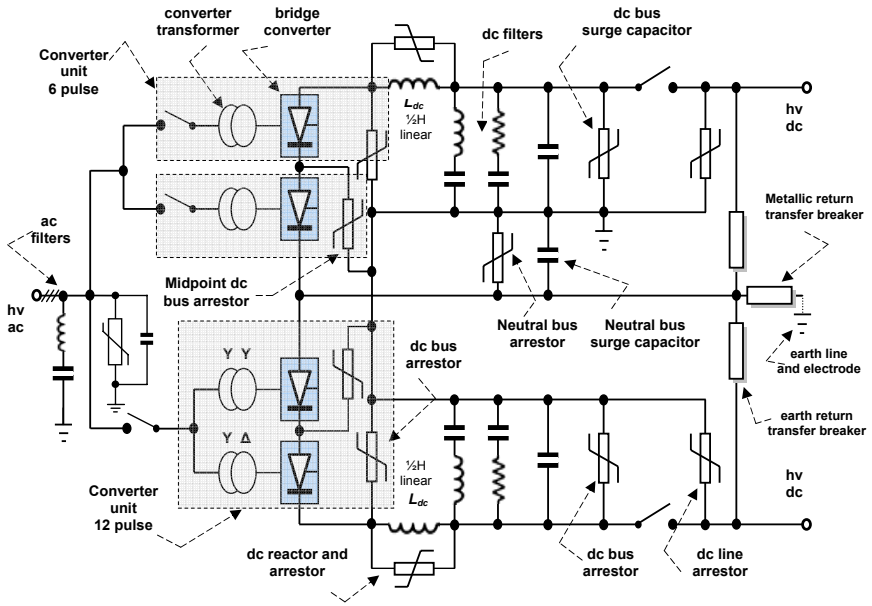


Figure 19.5. *Thyristor HVDC substation.*

19.4.1 Rectifier mode

Figure 19.9b shows that the angle between the input ac voltage and its fundamental current I_{a1} is determine by and equals, the phase delay angle α_r. The phasor diagram for rectification is shown in figure 19.10a. For a constant link current I_d, the fundamental ac input power factor is cos α_r while the input reactive power is given by

$$\begin{aligned} Q_r &= \sqrt{3}\, V_{LL} I_{a1} \sin\alpha_r = P_r \tan\alpha_r \\ &= \sqrt{3}\, V_{LL} \times \frac{2\sqrt{6}}{N\pi} I_d \times \sin\alpha_r = 2.7 \times V_{LL} \times \frac{I_d}{N} \times \sin\alpha_r \end{aligned} \tag{19.14}$$

The rms of the fundamental line current I_{a1} is $2\sqrt{6}I_d / N\pi$.

The real power transfer, which is the rectifier output power, is given by

$$\begin{aligned} P_r &= V_{dr} I_d = \sqrt{3}\, V_{LL} I_{a1} \cos\alpha_r = Q_r / \tan\alpha_r \\ &= \sqrt{3}\, V_{LL} \times \frac{2\sqrt{6}}{N\pi} I_d \times \cos\alpha_r = 2.7 \times V_{LL} \times \frac{I_d}{N} \times \cos\alpha_r \end{aligned} \tag{19.15}$$

To maximize the power flow and minimize the reactive power, the delay angle α_r should be small. From equation (19.15), to minimise the link I^2R loss, both I_d and the delay angle α_r should be small. That is, from equation (19.11), the rectifier output voltage should be maximised.

A low converter firing angle minimise the reactive power, reduce snubber losses, and reduces the harmonic content.

19.4.2 Inverter mode

The same basic rectifier mode equations hold in the inversion mode except that $\alpha_i > ½\pi$. Operational waveforms and the phasor diagram for this mode are shown in figure 19.10b. The reactive power is

$$\begin{aligned} Q_i &= \sqrt{3}\, V_{LL} I_{a1} \sin\alpha_i = \sqrt{3}\, V_{LL} \times \frac{2\sqrt{6}}{N\pi} I_d \times \sin\alpha_i = 2.7 \times V_{LL} \times \frac{I_d}{N} \times \sin\alpha_i \\ &= P_i \tan\alpha_i \end{aligned} \tag{19.16}$$

and the real power transfer, which is inverted into the ac system is given by

$$\begin{aligned} P_i &= V_{di} I_d = \sqrt{3}\, V_{LL} I_{a1} \cos\alpha_i = \sqrt{3}\, V_{LL} \times \frac{2\sqrt{6}}{N\pi} I_d \times \cos\alpha_i = 2.7 \times V_{LL} \times \frac{I_d}{N} \times \cos\alpha_i \\ &= Q_i / \tan\alpha_i \end{aligned} \tag{19.17}$$

To maximize the ac system power and minimize the reactive power, the delay angle α_i should be large ($\rightarrow \pi$). From equation (19.17), to minimise the link I^2R loss, I_d should be minimised (maximise dc link voltage) and the delay angle α_i should be large ($\rightarrow \pi$). Thus the inversion voltage should be as large as possible, avoiding commutation failure. Then the maximum α_i decreases as current increases since thyristor commutation time increases with current (and temperature).

P-Q operation of the twelve pulse series connected converter

The theory of controlled active and reactive power operation of a series connected 12-pulse converter assumes an ideal input transformer, negligible source impedance, and a constant current from the converter dc output bus. The output voltage contribution due to each constituent 6-pulse converter is given by

$$V_{dri} = \frac{3V_{max}}{\pi} \cos\alpha_i \tag{19.18}$$

where V_{max} is the peak line voltage of the voltage applied to each converter, α_i is the firing angle of the constituent converter, and i represents either converter 1 or 2.

By multiplying (19.18) by the dc load current I_{dc}, the active power is given by

$$Q_i = P_{max} \sin\alpha_i \tag{19.19}$$

where

$$P_{max} = \frac{3}{\pi} \bar{I}_o V_{max}$$

which represents the maximum power delivered from each converter at $\alpha_i = 0$. Similarly, the reactive power absorbed by the converter is given by

$$Q_i = P_{max} \sin\alpha_i \tag{19.20}$$

The active power P_d and reactive power Q_d, drawn by the 12-pulse converter are the sum of the contribution made by each converter, namely

$$\begin{aligned} P_d &= P_{max}(\cos\alpha_1 + \cos\alpha_2) \\ Q_d &= P_{max}(\sin\alpha_1 + \sin\alpha_2) \end{aligned} \tag{19.21}$$

From these two equations, the 12-pulse converter draws active power of $2P_{max}$ and zero reactive power at $\alpha_1 = \alpha_2 = 0$. Similarly, at $\alpha_1 = \alpha_2 = ½\pi$, the converter draws reactive power of $2P_{max}$ and zero active power. Therefore, $2P_{max}$ is the base power, 1 pu, and the equations in (19.21) become

$$\begin{aligned} P_{pu} &= ½(\cos\alpha_1 + \cos\alpha_2) \\ Q_{pu} &= ½(\sin\alpha_1 + \sin\alpha_2) \end{aligned} \tag{19.22}$$

The variation of P_{pu} and Q_{pu} with simultaneous variation of α_1 and α_2 is shown in the three-dimensional plots figure 19.6.

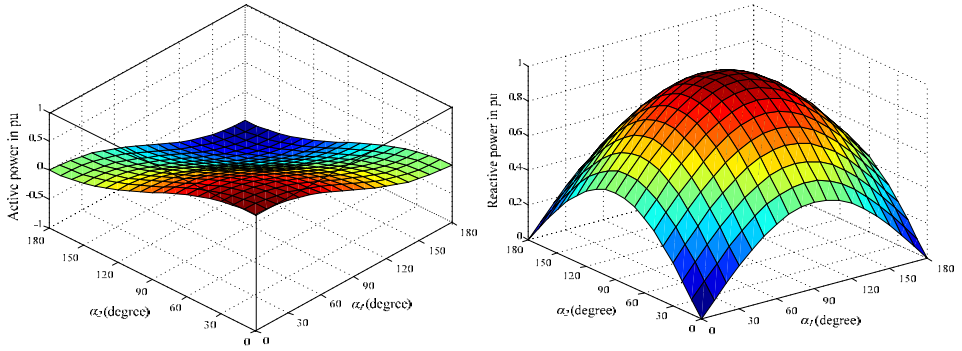
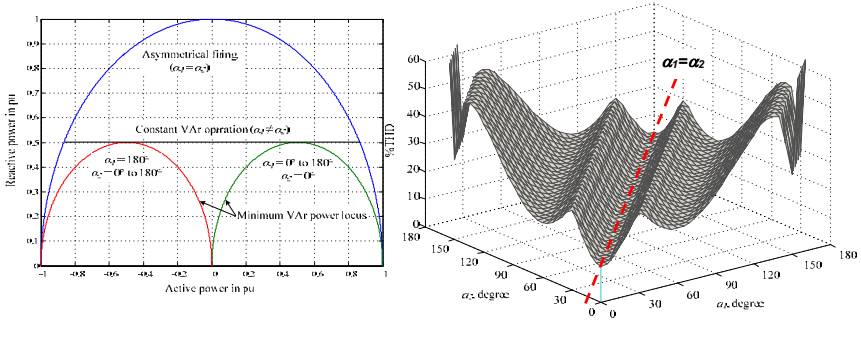


Figure 19.6. *Effects of varying of α_1 and α_2 on: (a) active power and (b) reactive power.*

The 12-pulse converter may operate with symmetrical firing of each 6-pulse converter, where $\alpha_1 = \alpha_2$ or with asymmetrical firing where $\alpha_1 \neq \alpha_2$ (or a combination of both). Different power loci can be realized by different combinations of firing angles (α_1 *and* α_2). Three power loci are shown in part 'a' of figure 19.7. The symmetrical firing *P-Q* locus is represented by the outer semicircle with centre '0' and radius of 1 pu, and is obtained by the symmetrical firing of α_1 and α_2 from 0 to π using the parts of equation (19.22). All points in the *P-Q* plane within the outer semicircle can be achieved by unique combinations of α_1 and α_2. The figure also shows power loci for asymmetrical firing which are represented by the circumference of the two inner semicircles with radii of 0.5 pu. These are obtained by varying α_1 from 0 to π while α_2 is held at '0' in the case of rectification and by varying α_2 from 0 to π while α_1 is held at π in the case of inversion. Part 'a' also shows the power locus for constant VAr operation indicated by the line parallel to the P_{pu} axis. With asymmetrical firing the maximum reactive power is decreased to one-half the case for symmetrical firing. Part 'b' of figure 19.7 shows the variation of input current THD with varied delay angles and reflects the adverse effect of asymmetrical firing on the THD.



(a) (b)

Figure 19.7: *Twelve-pulse fully-controlled converter: (a) power loci and (b) input current THD.*

The symmetrical firing power locus is associated with the best THD and the worst supply current power factor. On the other hand, asymmetrical firing decreases the reactive power flowing in the system, which improves the input power factor but deteriorates the input current THD, which limits the power factor improvement. As a result, asymmetrical firing of the 12-pulse converter offers the possibility of a smaller reactive power compensator for power factor compensation, at the expense increased input current harmonics.

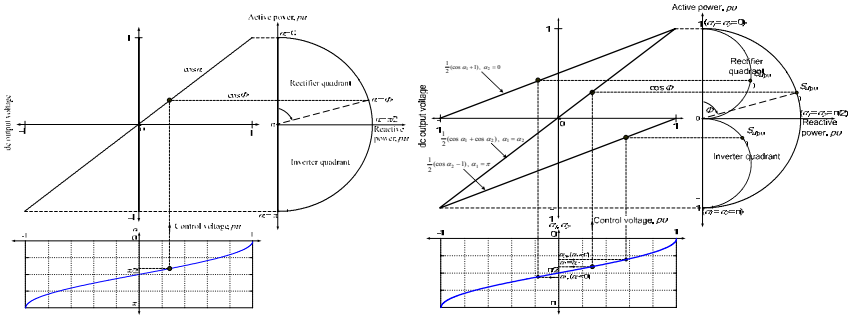


Figure 19.8: *Power locus of 6-pulse and 12-pulse converters and per unit output voltage.*

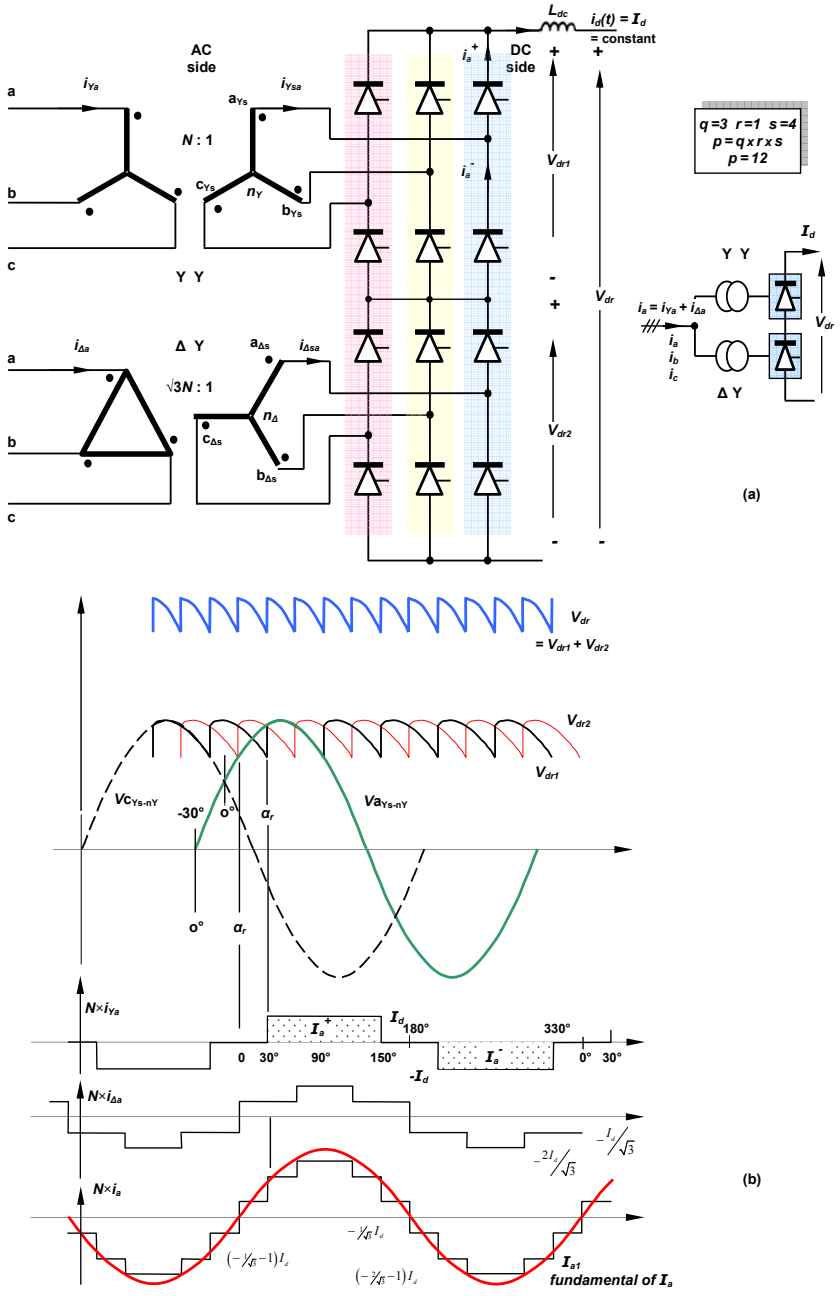


Figure 19.9. *Twelve-pulse valve group converter configuration with star-star and star-delta connected converter transformers: (a) converter schematic and (b) twelve-pulse valve group waveforms.*

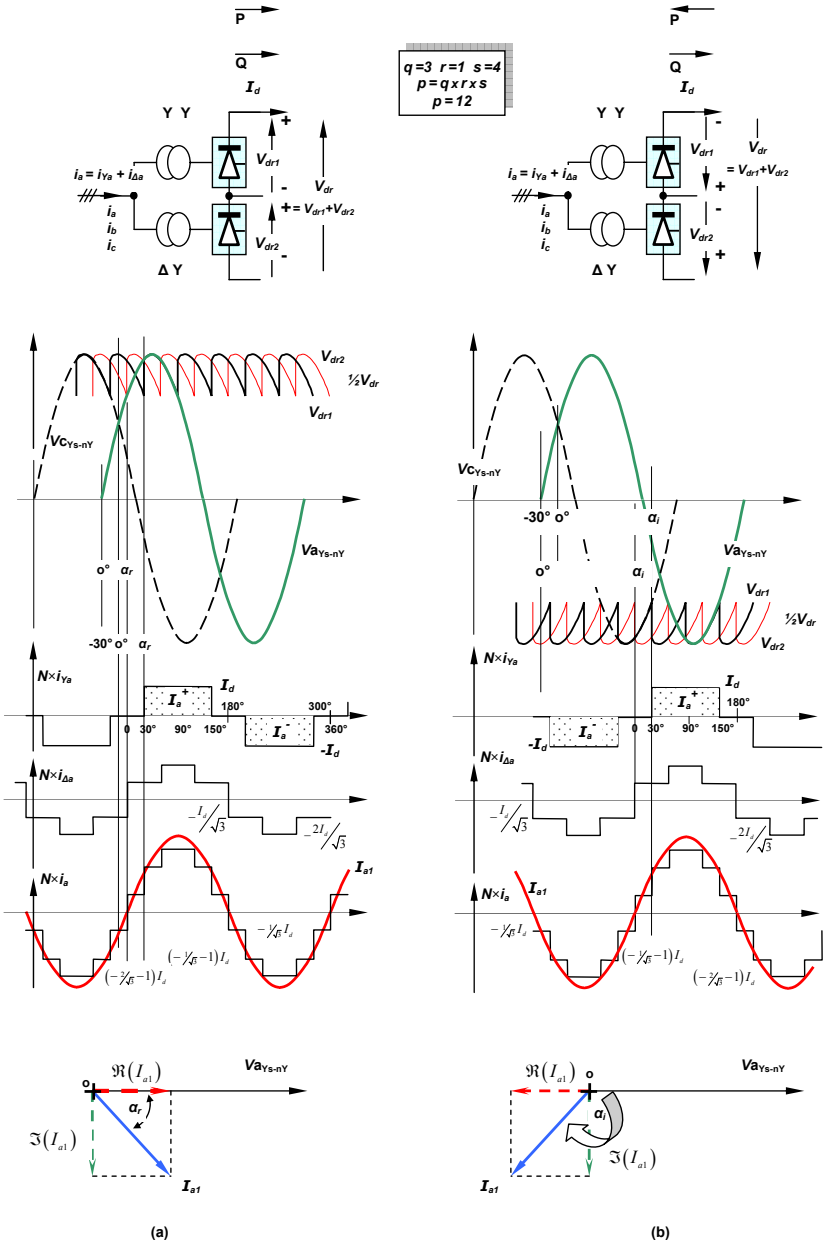


Figure 19.10. *Twelve-pulse valve group converter configuration with star-star and star-delta connected converter transformers operating in: (a) a rectifying mode and (b) an inverting mode.*

19.5 Twelve-pulse ac line frequency converter operation control

Rectification and inversion modes of converter operation and the line (or natural) commutation process of the three-phase fully-controlled thyristor converter have been considered in chapter 12.4 for rectification, with overlap in 12.5, and 12.6 for inversion with overlap.
One converter operates as a rectifier (power flow from ac to dc) and the other dc link converter operates as an inverter (power flow from dc to ac). Either terminal converter can operate as an inverter or rectifier, since the delay angle determines the mode (voltage) of operation. The power flow between the two ac systems connected to the HVDC link is controlled by controlling the delay angle of each converter. Current only flows in one direction in the dc link, from the rectifier to the inverter. A simple system model is shown figure 19.11 where the link dc resistance is represented by R_{dc} and source reactance, hence overlap effects have been neglected. Let the transformer turns ratio factor N equal 1. The dc current I_d is

$$I_d = \frac{V_{dr} + V_{di}}{R_{dc}} \tag{19.23}$$

where

$$V_{dr} = \frac{3}{\pi}\sqrt{2}\,V_{LL}\cos\alpha_r \quad \text{for} \quad 0 \le \alpha_r \le ½\pi$$
$$V_{di} = \frac{3}{\pi}\sqrt{2}\,V_{LL}\cos\alpha_i \quad \text{for} \quad ½\pi \le \alpha_i \le \pi \tag{19.24}$$

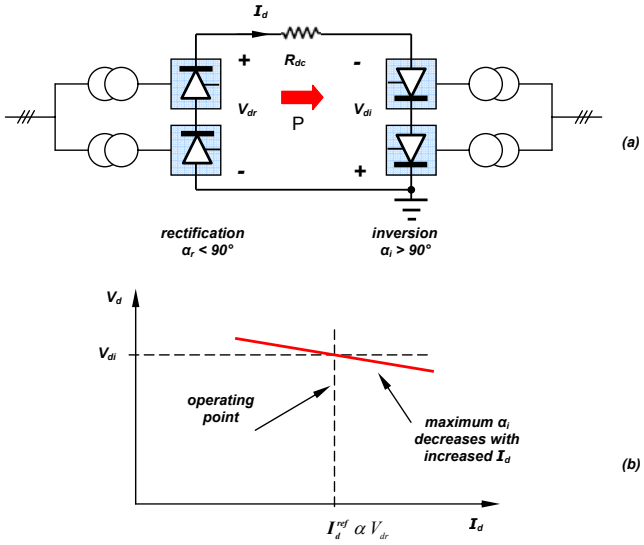


Figure 19.11. *Basic HVDC transmission system: (a) circuit diagram and (b) load line characteristics.*

The rectifier output power is

$$P_r = V_{dr} I_d \tag{19.25}$$

while the power supplied to the inverter is

$$P_i = V_{di} I_d \tag{19.26}$$

where

$$P_r = V_{dr} I_d = V_{di} I_d + I_d^2 R_{dc} = P_i + I_d^2 R_{dc} \tag{19.27}$$

If transformer per phase leakage inductance L_s, referred to the converter side, is accounted for, then the resultant overlap at commutation reduces the output voltage for each six-pulse converter.

$$V_{dr} = 2\times\left(\frac{3}{\pi}\sqrt{2}\,V_{LL}\cos\alpha_r - \frac{3\omega L_s}{\pi} I_d\right) = \frac{6}{\pi}\times\left(\sqrt{2}\,V_{LL}\cos\alpha_r - \omega L_s I_d\right) \tag{19.28}$$

Both the rectifier and inverter dc output voltages can be compensated for leakage reactance commutation overlap. Remember the overlap voltage component is not a loss element in the resistor sense. It represents a 'lossless' loss of voltage which increases with current.
If the link voltage is controlled by the inverter and the dc current controlled by the rectifier, then the load line characteristic in figure 19.11c results. The inverter voltage is kept slightly below the rectifier voltage. As the load current increases, the inverter terminal voltage is reduced. This is because the time to safely commutate the inverter thyristors increases with current, hence α_i must decrease, as shown by the droop in the output characteristics in figure 19.11b. The more detailed practical approach to HVDC power transport control is considered in section 19.5.1.

19.5.1 Control and protection

HVDC transmission systems must operate under tightly controlled conditions. Dc-link current and the two terminal voltages are precisely controlled to affect the desired power transfer. Accurate system quantity measurements are required, which include at each converter bridge, the dc-link current, the dc-side voltages, and the delay angle α for each converter/inverter.
Two terminal dc transmission systems have a preferred control mode during normal operation.

Inverter

Under steady-state conditions, the inverter controls the dc voltage by one of two methods.

- The inverter maintains a constant delay angle $\alpha_i > 90°$, or extinction angle γ, where $\gamma = \pi - \alpha_i$, This constant angle maintenance causes the dc voltage V_d to droop with increasing dc current I_d, as shown in the minimum constant extinction angle $\breve{\gamma}$ characteristic in figure 19.12b and labelled A-B-C-D in figure 19.12c. The weaker the ac system at the inverter, the steeper the droop characteristic.
- Alternatively, the inverter may operate in a dc voltage controlling mode which is the constant V_d characteristic shown dashed in figure 19.12b and labelled B-H-E in figure 19.12c. To achieve this, the extinction angle γ must increase beyond its minimum value characterised in figure 19.12b as $\breve{\gamma}$.

Rectifier

If the inverter is operated in either a minimum constant γ or constant V_d mode, then the rectifier is used to control the dc link current I_d. This is achievable provided the delay angle α_r is not at its minimum limit. The steady-state constant current characteristic of the rectifier is shown in figure 19.12a as the vertical section of the characteristic S-T and is labelled S-C-H-T in figure 19.12c. The rectifier delay angle is increased toward $\alpha_r = 90°$ if the link current attempts to increase beyond the reference level I_d^{ref}. During an attempted short circuit fault, the rectifier delay angle reaches 90° which sets the rectifier output voltage to zero, as shown by equation (19.24), and controls the fault current to I_d^{ref} as shown by trajectory S-T in figure 19.12a.

The operating point of the HVDC system is where the rectifier characteristic intersects the inverter characteristics, either at point C or point H on figure 19.12c, depending on which of the two inverter control methods is being employed. The operating point is tuned over a period of tens of seconds by adjusting the line-side tap changers of the converter transformers.
The inverter controls the dc-link voltage as follows.

- The inverter establishes the desired dc voltage V_d by tap changer adjustment, if it is operated in a constant minimum γ mode.
- If the inverter is operated in a constant V_d mode, the tap changer is adjusted to produce constant V_d with an extinction angle slightly larger than the minimum $\breve{\gamma}$.

The ac-side tap changers on the rectifier end transformers are adjusted so that the delay angle α is small but with a 5° working range, whilst maintain the constant current I_d^{ref}. If the inverter is constant dc voltage operated at the operating point H, and if the dc current I_d^{ref} is increased so that the operating point H moves towards A, the inverter control mode reverts to constant extinction angle γ control when operating in the droop region A-B. The voltage V_d droops to less than the desired value, so the inverter end transformer tap changer progressively boosts the dc-side voltage until dc voltage control recommences, in region B-C-D.

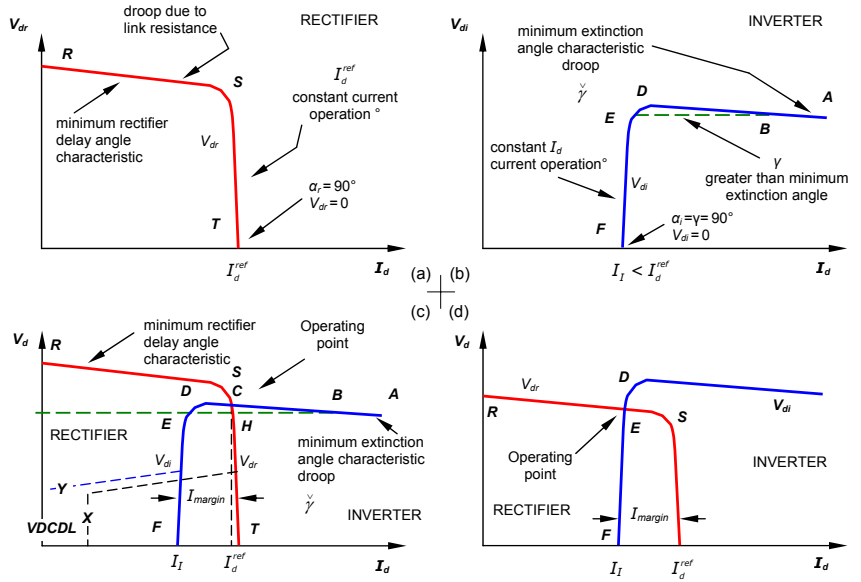


Figure 19.12. *Steady-state V_d - I_d characteristics for a two terminal HVDC system.*

Not all HVDC transmission systems use constant dc voltage control, which is the horizontal characteristic B-H-E in figure 19.12c. Instead, the tap changer in conjunction with the constant extinction angle γ control characteristic A-B-C-D in figure 19.12c, provides dc voltage control.

Current margin

The rectifier and inverter controllers both receive the dc current demand I_d^{ref} but the inverter current demand is decreased by an amount termed the current margin I_{margin}, as shown in Figure 19.12c. This current margin is usually a constant magnitude of about 10% of rated current. The inverter current controller endeavours to control the dc link current to $I_I = I_d^{ref} - I_{margin}$ but the rectifier current controller dominates and maintains the dc current at I_d^{ref}. In steady-state the rectifier controller overrides the inverter controller which is not able maintain a dc current I_d^{ref} - I_{margin}. The inverter current controller only becomes active when the rectifier current controller has reduced its delay angle α_r to the minimum limit. This rectifier minimum delay angle limit is characterised by R-S in figure 19.12c.

Control characteristic performance

Variations in the ac voltages change the control operating point of the system as follows.
i. When the rectifier side ac voltage decreases and/or the inverter side ac voltage increases, then the transformer tap adjustment mechanisms on both the rectifier and inverter transformers should attempt to remedy this ac voltage regulation problem. If the disturbance is large enough, the new stable operating point is shown in figure 19.12d. The R-S characteristic falls below points D or E, the operating point will shift from point H to somewhere on the vertical characteristic D-E-F where it is intersected by the lowered minimum α_r R-S characteristic as shown in figure 19.12d. The inverter converts to current control, controlling the dc current I_d to the value $I_I = I_d^{ref}$ - I_{margin}, approximately 10% of rated current and the rectifier effectively controls the dc voltage provided it is operating at its minimum delay angle characteristic R-S. The dc power flow is relatively unaffected and safely returns to the normal operating condition shown in figure 19.12c, once the ac disturbances have subsided.
ii. If the rectifier ac voltage increases, the reference current, which is set by the rectifier, is unaffected. Since the link voltage is set by the inverter, any increase in rectifier ac voltage does not affect the power flow. This can be seen in figure 19.12c where increasing the rectifier characteristic R-S does not affect the intersection of the operating point C, whence power flow is unaffected by an increase in the rectifier ac-side voltage.

iii. If the inverter side ac voltage is decreased, the link voltage decreases proportionally, but the current is unaffected because it is set by the rectifier. The power flow is therefore decreased in line with the inverter ac voltage decrease. This can be seen in figure 19.12c where the inverter side ac voltage decrease will lower the inverter characteristic A-B-C-D. The operating point C, the operating voltage, decreases but the current is unaffected. Thus the power transferred is decreased in-line with the inverter ac-side voltage.

vi. Worst case conditions are a dc-link short circuit. As seen in figure 19.12a, the rectifier maximum current is I_d^{ref}, while figure 19.12b shows that the maximum inverter current is I_I. The maximum fault current is therefore limited to the operational current margin I_{margin}. As seen in figures 19.12a and 19.12b, the control angle of both converters moves to 90°, which produces 0V converter output voltages, as shown by equation (19.24). Hence the power associated with any short circuit fault is low, unlike short circuit faults in ac transmission systems.

Voltage dependant current demand limit (VDCDL)

If the ac voltages sag significantly because of weak ac systems, it may not be possible to maintain full load current. In such a case the dc-link voltage is decreased, and the controller characteristics are dictated by the trajectories X and Y in figure 19.12c. A controller which reduces the maximum current demand in such conditions, is termed a voltage dependant current demand limiter, or VDCDL. The current is not reduced to zero so that recovery response is faster once the dc-link voltage has sufficiently recovered.

Power flow reversal

The controllers can be designed such that the transition from the rectifier controlling current to the inverter controlling current, is automatic and smooth. That is, seamless automatic power flow reversal is achieved by interchanging the inverter and rectifier functions, as seen in figure 19.13. This is realised by appropriate control of the delay angles, hence terminal polarities, but the dc link current direction does not reverse. Such a bi-directional power flow requirement may be necessary when two ac systems are required to bi-directionally interchange power. The rectifier delay angle is progressively increased while the inverter delay angle is decreased, such that the rectifier and inverter voltage difference is control to be virtually constant. This is achieved if $\alpha_r + \alpha_i \approx 180°$ is maintained.

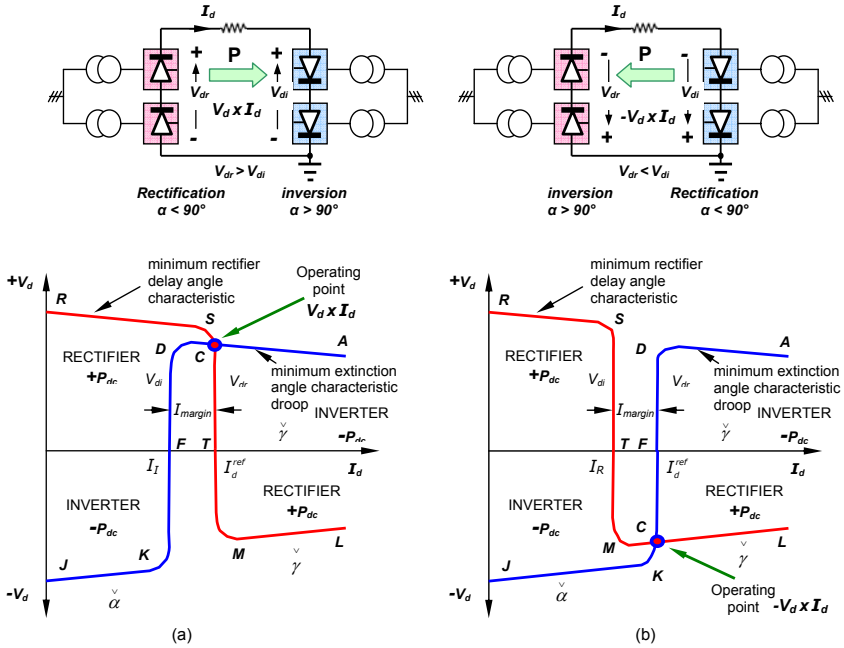


Figure 19.13. *Power reversal in HVDC systems by voltage polarity reversal, not current reversal.*

19.5.2 HVDC Control objectives

The fundamental objectives of a CSI-based HVDC control system are as follows:

- to control basic system quantities such as dc line current, dc voltage, and transmitted power accurately and with sufficient speed of response;
- to maintain adequate commutation margin in inverter operation so that the valves can recover their forward blocking capability after conduction before their voltage polarity reverses;
- to control higher-level parameters such as frequency in isolated mode or provide power oscillation damping to help stabilize the ac network;
- to compensate for loss of a pole, a generator, or an ac transmission circuit by rapid readjustment of power;
- to ensure stable operation with reliable commutation in the presence of system disturbances;
- to minimize system losses and converter reactive power consumption; and
- to ensure proper operation with fast and stable recovery from ac system faults and disturbances.

19.6 Delta/Delta/Double Polygon 18 pulse converter

Six-pulse bridge circuits can be in series or parallel to create an 18-pulse converter. In series, as in figure 19.14, power source harmonic voltages can be eliminated. The series connection does not need inter-phase transformers, unlike parallel connected converters.

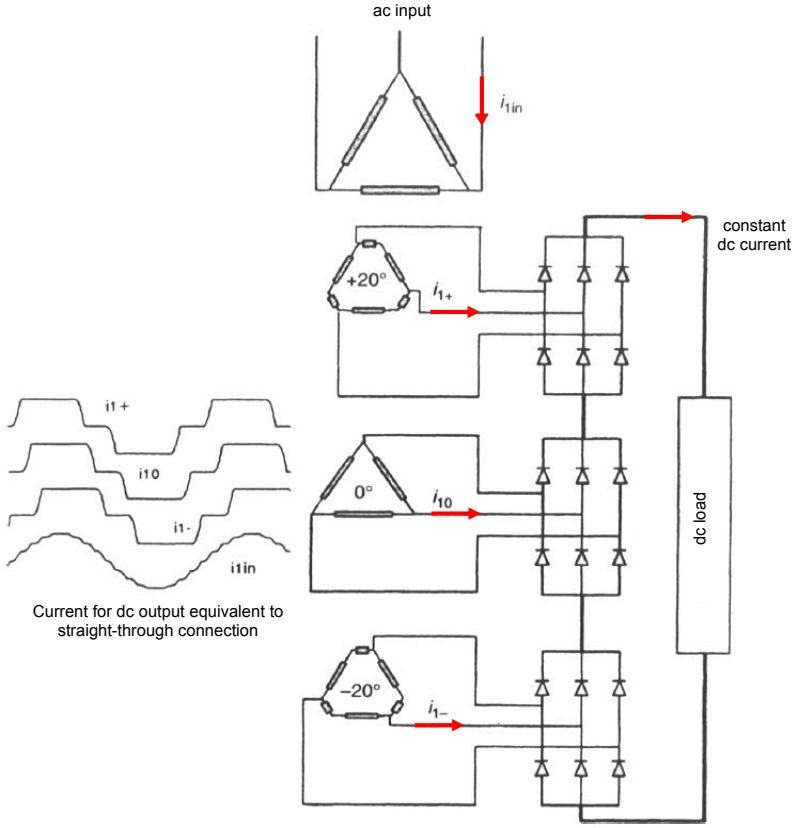


Figure 19.14. *Delta/delta/double polygon for 18 pulse rectifiers.*

Transformer leakage inductances are an important practical feature in the design. An alternative method using physically separate phase-shifting transformers is also feasible. In principle this connection can be extended to higher pulse numbers by increasing the number of polygon windings and modifying the phase shift accordingly. Practical limitations occur due to reactance effects, efficiency, and the limit on available turns ratios.
Appropriate zig-zag and forked connections could also be employed to provide similar 18 pulse characteristics. However, polygons are easier to use for low-voltage outputs because the higher number of turns facilitates selection of the turns ratios.

19.6.1 Analysis of Double-Wound Polygon

Analysis of closed polygon connections tends to be more cumbersome than that for open (fork) connections. Thus the procedure for the general polygon case is presented.
Let Φ be the phase shift between polygon output line-to-line voltage V_{Ls} and the delta input line-to-line voltage V_{Lin}. Let the turns/phase on the delta winding be N_p and polygon windings have N_l turns for the long winding and N_s turns for the short winding. Figure 19.15 shows the arrangement for reference.

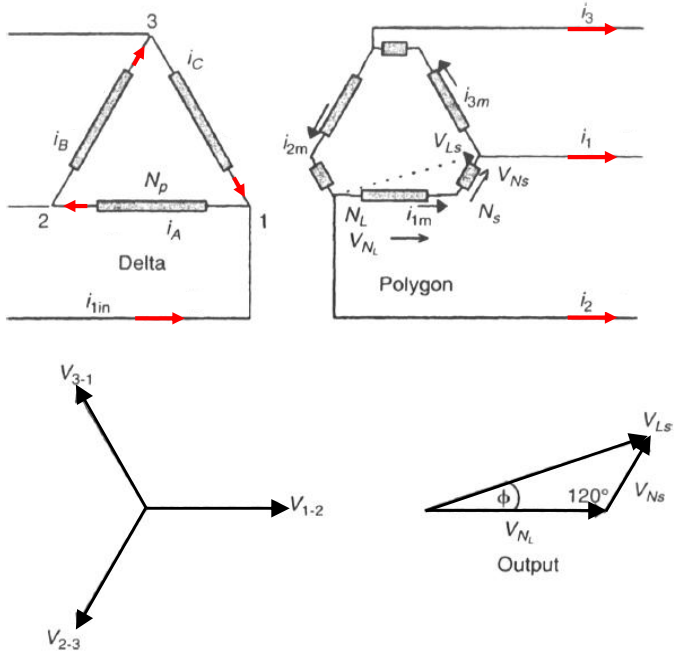


Figure 19.15. *Double-wound polygon connection phasor diagram.*

Polygon voltages and phase shift

From the polygon vector drawing in figure 19.15

$$\frac{V_{Ls}}{\sin 120^\circ} = \frac{V_{Ns}}{\sin\phi} = \frac{V_{Nl}}{\sin 60^\circ - \phi}$$

Thus

polygon long winding voltage: $V_{N1} = \frac{2}{\sqrt{3}} V_{Ls} \sin(60^\circ - \phi)$

and

polygon short winding voltage: $V_{Ns} = \frac{2}{\sqrt{3}} V_{Ls} \sin\phi$ (4.2)

From the figure 19.15

$$\tan\phi = \frac{V_{Ns}\sin 60^\circ}{V_{Nl} + V_{Ns}\cos 60^\circ}$$

Thus for a turns ratio given by $n = V_{Nl} / V_{Ns}$

$$\phi = \tan^{-1}\frac{\sqrt{3}}{1+2n}$$

Polygon winding currents

$$i_{1m} - i_{3m} = i_1$$
$$i_{2m} - i_{1m} = i_2$$

Subtracting these equations gives

$$i_{1m} - i_{3m} - i_{2m} + i_{1m} = i_1 - i_2$$

Incorporate $i_{1m} + i_{2m} + i_{3m} = 0$

$$i_{1m} = \frac{i_1 - i_2}{3}$$

Also

$$i_{2m} = \frac{i_2 - i_3}{3} \text{ and } i_{3m} = \frac{i_3 - i_1}{3}$$

In general, the converter input currents consist of current pulses with amplitude I_d. They incorporate harmonics of the form $(6k \pm 1)$, which include positive-and negative-sequence currents. To calculate the rms current in the winding, these harmonics are considered individually then summed $(\sqrt{\Sigma i^2})$ to determine the total rms value. The fundamental and rms currents in each converter line are displaced by $\pm\frac{2}{3}\pi$ depending on their sequence. Thus, each component, hence the total, is multiplied by

$$\left[\left(1-\cos\pm\tfrac{2}{3}\pi\right)^2 + \left(\sin\pm\tfrac{2}{3}\pi\right)^2\right]^{1/2}$$

that is, √3, as it flows into the secondary windings. The idealized converter line current is a 120° conduction square wave with rms value of $I_d\sqrt{\frac{2}{3}}$. Substituting these results into the equation for i_{1m}, yields

$$\text{secondary winding rms current } \sqrt{3}\,\frac{1}{3}\sqrt{\frac{2}{3}} I_d = 0.471 I_d$$

When load currents; i_1, i_2, and i_3 which are characteristic of a three-phase bridge rectifier, are present, the line input current to the delta winding is calculated as follows. The sum of ampere-turns on the transformer core must be zero. Thus

$$i_A N_p - i_{1m} N_l + i_{3m} N_s = 0$$

from which

$$i_A = i_{1m}\frac{N_l}{N_p} - i_{3m}\frac{N_s}{N_p}$$

and, similarly

$$i_C = i_{3m}\frac{N_l}{N_p} - i_{2m}\frac{N_s}{N_p}$$

The delta winding line input current is given by

$$i_{1in} = i_A - i_C$$

Thus

$$i_{1in} = \frac{N_l}{N_p}(i_{1m} - i_{3m}) + \frac{N_s}{N_p}(i_{2m} - i_{3m})$$

From Figure 19.15

$$i_{1m} - i_{3m} = i_1 \text{ and } i_{2m} - i_{1m} = i_2$$

Thus

$$i_{2m} - i_{3m} = i_1 - i_2$$

Therefore

$$i_{1in} = i_1\left[\frac{N_l}{N_p} + \frac{N_s}{N_p}\right] + i_2\frac{N_s}{N_p}$$

When the voltage ratio output to input is 1:1,

$$\frac{N_l}{N_p} = \sqrt{2/3} \text{ and } \frac{N_s}{N_p} = \frac{\sqrt{3}-1}{\sqrt{6}}$$

The phase shift is governed by the ratio of the secondary turns and is determined to be 15°.
Using these ratios, the line input current is

$$i_{1in} = 1.1153 i_1 + 0.299 i_2 \quad \text{for } 15^\circ$$

Extending this analysis, the polygon winding kVA can be determined in respect to the dc load power. The result is

$$\frac{\text{D.W.polygon winding } VA}{V_{do}I_d} = 1.209\left(\sin(60° - \phi) + \sin\phi\right)$$

19.7 Filtering and power factor correction

As shown in figure 19.5, both ac and dc side filtering is used to reduce radiated EMC on the dc link and conducted EMC on the ac sides which causes power losses and interference.

On the dc-side, the large link inductance at each converter (typically between 0.2H and 0.5H) is supplemented with *LC* filters, tuned to eliminate selected 12*n* current harmonics in a 12-pulse system. A filter is notch tuned to eliminate (shunt) one specific harmonic, usually the most dominate 12^{th}. At 50/60Hz, these filters are capacitive thus provide reactive power absorbed by the converters.
Harmonics occur at 12*n*±1 on the ac-side. Again, tuned *LC* filters eliminate (shunt) specific low order harmonics and a general high pass shunt filter is used for components above the 11^{th} and 13^{th}. Generally, higher pulse order (>12) transformer/converter arrangements are not attractive in HVDC because of the difficulties in producing high-voltage transformers (auto-transformers tend to be used).
Additional to the VAr compensation provided by the ac harmonic filters, pure capacitance may also be used. In order to avoid overcompensation voltage regulation problems which can occur at low power transmission levels, the extra capacitance tends to be switched in-circuit as needed.

The main transformers may be provided with ac-side voltage taps to adjust the secondary voltage, as considered in section 19.5.1. The taps are switched automatically by motorised tap-changing drives, which only operate when large voltage changes occur for prolonged periods of time. If the transformers have only Y-Y winding configurations, they may also have a low-voltage delta tertiary winding for VAr compensation, provide ancillary supplies, and suppression of transformer core triplen harmonic fluxes.

Feature summary of Line Commutated Thyristor Systems

With the exception of multi-terminal HVDC the basic steady state operation required of FACTS and HVDC systems may be achieved through the use of thyristor based systems. There are however limits on the performance and functionality that may be achieved.

Advantages

a) High voltage thyristor devices give low losses and are available in robust high-current capacity single-wafer capsules that fail short circuit.
b) Line commutated HVDC and FACTS have an established track record at transmission voltage and power levels.

Disadvantages

a) Line commutated systems inject significant low frequency harmonics which must be eliminated by large (physically and electrically) passive filter arrangements. The presence of these filters may lead to circulating harmonic currents which must be mitigated by damping networks. Filters and damping networks may have to be designed specifically for each location and may not be optimal for all operating conditions.
b) Line commutated systems are inherently limited in response time (limited to line frequency switching) and may suffer control capability limits. For example thyristor based HVDC:
   i. cannot decouple the real and reactive power injected into the network.
   ii. may have limited operating range depending on the source impedance provided by the ac network at the point of connection.
c) Line commutated circuits tend to require large passive components leading to large footprint systems.

Example 19.1: *Basic six-pulse converter based hvdc transmission*

The basic six-pulse converter dc transmission system represented by figure 19.16 connects a 230kV ac rms, 50Hz system to a 220kV, 60Hz system. The 6-pulse converters at each transmission line end are interface by a Δ_{ac}-Y_{dc} transformers of turns ratio √3:2, as shown, such that the transformer dc-side line voltage is double the ac side line voltage. The power transmission is 500MW to the inverter which is maintained at a dc voltage level of 500kV. The total dc-line resistance is 8Ω.

Determine

i. The inverter delay angle, α_i.
ii. The dc-link current, hence rectifier output voltage, thence rectifier delay angle, α_r.
iii. The rectifier input power and VAr, and inverter VAr, thence system efficiency.

Solution

Because of the transformer turns ratio, the transformer dc-side ac voltages are double the ac-side voltages.

i. The inverter delay angle is derived from equation (19.24)

$$V_{di} = \frac{3}{\pi}\sqrt{2}\,V_{LL}\cos\alpha_i$$

$$500\text{kV} = \frac{3}{\pi}\sqrt{2}\;2\times 220\text{kV}\times\cos\alpha_i$$

$$\text{that is } \alpha_i = 147.3°$$

ii. From $P_i = V_{di} \times I_d$, the link current is

$$I_d = \frac{500\times10^6\ \text{W}}{500\times10^3\ \text{V}} = 1000\ \text{A}$$

The rectifier output voltage is given by equation (19.23), rearranged

$$V_{dr} = -V_{di} + I_d R_{dc}$$

$$= -\ -500\text{kV} + 1000\text{A}\times1\Omega = 508\text{kV}$$

The rectifier delay angle is derived from equation (19.24)

$$V_{dr} = \frac{3}{\pi}\sqrt{2}\,V_{LL}\cos\alpha_i$$

$$508\text{kV} = \frac{3}{\pi}\sqrt{2}\times2\times230\text{kV}\times\cos\alpha_r$$

$$\text{yields } \alpha_r = 35°$$

iii. The input power is the output plus dc-link resistive losses, that is

$$P_r = I_d^2 \times R_{dc} + P_i$$

$$= 1000^2\times8\Omega + 500\text{MW} = 508\text{MW}$$

The input VAr from the ac side is

$$Q_r = P_r \tan\alpha_r$$

$$= 508\text{MW}\times\tan35° = 355.7\text{MVAr}$$

Similarly, the inverter VAr into the ac side (indicated by the negative sign) is

$$Q_i = P_i \tan\alpha_{ir}$$

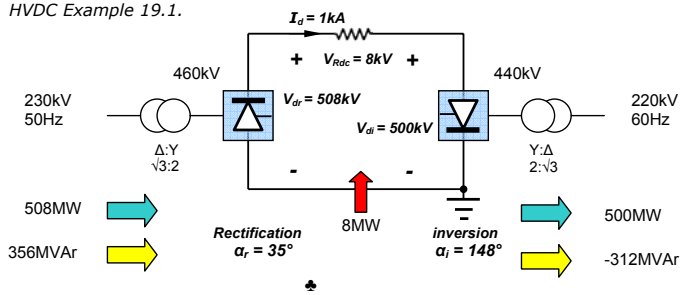
$$= 500\text{MW}\times\tan148° = -312.4\text{MVAr}$$

The efficiency is

$$\eta = \frac{P_i}{P_o}$$

$$= \frac{500\text{MW}}{508\text{MW}}\times100 = 98.43\%$$

Figure 19.16. *HVDC Example 19.1.*



The following example is based on example 19.1.

Example 19.2: ***12-pulse hvdc transmission***

The dc transmission line represented by figure 19.11 connects a 230kV ac rms, 50Hz system to a 220kV, 60Hz system. The 12-pulse bipolar converters at each transmission line end are interface by a Y-Y transformer of turns ratio 1:1 and a Δ-Y transformer of turns ratio 1:√3, each with a converter side inductance of 1mH. The rectifier delay angle is α = 30° for 500MW power transmission and the inverter advance angle is α = 160° (in order to avoid any reactive power increase), which maintains the dc voltage level at 500kV at the inverter end.
The total line resistance is 8Ω and the dc link smoothing inductance is large enough to initially consider the dc current to be ripple free.

Determine

i. The transformer tap ratios at each end, the dc link efficiency, I^2R losses, and both terminal VAr
ii. If the rectifier tap ratio of 0.866 results in the transmission current limit giving a power of 600MW, find the delay angle and line efficiency for 500kV at the inverter.
iii. The value of the dc link inductance L_{dc} such that the link peak to peak current is 0.1pu the average load current at full load (1200A), assuming the normalised magnitude of the dc side harmonic V_{12} is 0.15pu maximum (with respect to the 50Hz supply).

Solution

i. From $P_i = V_{di} \times I_d$, the link current is

$$I_d = \frac{500\times10^6\ \text{W}}{500\times10^3\ \text{V}} = 1000\ \text{A}$$

The inverter voltage, accounting for the transformer tapping a_i is given by an equation similar to equation (19.28), that is

$$V_{di} = 2\times\left(\frac{3}{\pi}\sqrt{2}\,a_i V_{LL}\cos\alpha_r - \frac{3\omega L_s}{\pi}I_d\right)$$

$$500\times10^3\,\text{V} = 2\times\left(\frac{3}{\pi}\sqrt{2}\,a_i\,220\times10^3\,\text{V}\cos(180°-160°) - \frac{3\times2\times\pi\times60\text{Hz}\times1\times10^{-3}\text{H}}{\pi}1000\text{A}\right)$$

which gives a transformer tap ratio at the inverter end of a_i = 0.896.
From equation (19.23), the rectifier voltage is

$$V_{dr} = V_{di} + R_{dc}I_d$$
$$= 500\text{kV} + 8\Omega\times1000\text{A} = 508\text{kV}$$

and the necessary transformer tap ratio a_r is derive from

$$V_{dr} = 2\times\left(\frac{3}{\pi}\sqrt{2}\,a_r V_{LL}\cos\alpha_r - \frac{3\omega L_s}{\pi}I_d\right)$$

$$508\times10^3\,\text{V} = 2\times\left(\frac{3}{\pi}\sqrt{2}\,a_r\,230\times10^3\,\text{V}\cos30° - \frac{3\times2\times\pi\times50\text{Hz}\times1\times10^{-3}\text{H}}{\pi}1000\text{A}\right)$$

which gives a transformer tap ratio at the rectifier end of a_r = 0. 945.

The link efficiency is

$$\eta = \frac{P_i}{P_r}\times100 = \frac{V_iI_d}{V_rI_d}\times100$$
$$= \frac{500\text{kV}}{508\text{kV}}\times100 = 98.4\%$$

The I^2R losses are 1000A^2×8Ω = 8MW or (508-500)^2/8 Ω, dissipated, distributed along the line.

The rectifier reactive power is given by equation (19.14), that is

$$Q_r = P_r\tan\alpha_r$$
= (500MW + 1000A^2×8Ω)×tan30° = 293.3MVAr

This is 293.3MVAr from to rectifier ac side.

The inverter reactive power is given by equation (19.16), that is

$$Q_i = P_i\tan\alpha_i$$
= 500MW × tan160° = - 182MVAr

This is 182MVAr to the ac side of the inverter.

ii. At 500kV and 600MW:

$$I_d = \frac{P_i}{V_{di}} = \frac{600\text{MW}}{500\text{kV}} = 1200\text{A}$$

Accounting for the link resistive voltage drop

$$V_{dr} = V_{di} + R_{dc}I_d$$
$$= 500\text{kV} + 8\Omega\times1200\text{A} = 509.6\text{kV}$$

The efficiency is

$$\eta = \frac{P_i}{P_r}\times100 = \frac{V_iI_d}{V_rI_d}\times100$$
$$= \frac{500\text{kV}}{509.6\text{kV}}\times100 = 98.1\%$$

The necessary rectifier angle, accounting for transformer reactive inductance, is

$$V_{dr} = 2\times\left(\frac{3}{\pi}\sqrt{2}\,a_i V_{LL}\cos\alpha_r - \frac{3\omega L_s}{\pi}I_d\right)$$

$$509.6\times10^3\,\text{V} = 2\times\left(\frac{3}{\pi}\sqrt{2}\times0.866\times230\times10^3\,\text{V}\cos\alpha_r - \frac{3\times2\times\pi\times50\text{Hz}\times1\times10^{-3}\text{H}}{\pi}\times1200\text{A}\right)$$

which gives a rectifier delay angle of α_r = 18.5°.

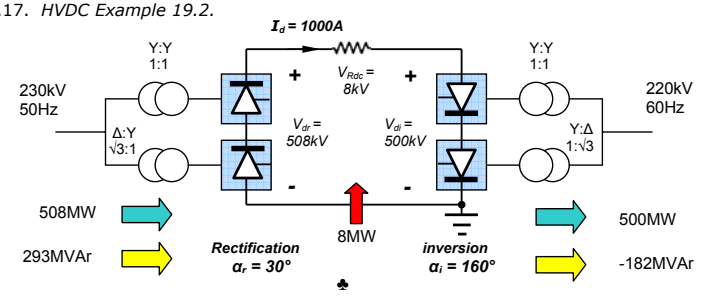
iii. The maximum link voltage from the 50Hz rectifier, accounting for leakage at maximum current is

$$V_{dr} = 2\times\left(\frac{3}{\pi}\sqrt{2}\,V_{LL}\cos\alpha_r - \frac{3\omega L_s}{\pi}I_d\right)$$
$$= 2\times\left(\frac{3}{\pi}\sqrt{2}\,230\text{kV}\times\cos0° - \frac{3\times2\pi50\text{Hz}\times1\times10^{-3}\text{H}}{\pi}1200\text{A}\right)$$
$$= 620.5\text{kV}$$

The magnitude of the 600Hz component (12×50Hz) is 15% of 620.5kV, namely 93.1kV, which produces a ripple current of 10% of rated current, 1200A, namely 120A. Thus from $v = Ldi/dt$

$$L_{dc} = v_{12}\frac{\Delta t_{12}}{\Delta i_{12}}$$
$$= 93.1\text{kV}\times\frac{1}{12\times50\text{Hz}\times120\text{A}} = 1.3\text{H}$$

Figure 19.17. *HVDC Example 19.2.*



19.8 VSC-Based HVDC

Voltage source converters (VSC) for dc-transmission are one of two-level, neutral point clamped or modular multi-level converters.

Voltage source converter-based (VSC) dc-transmission consists of a bipolar two-wire HVDC system with self-commutatable converters connected pole-to-pole, as shown in figure 19.18. DC capacitors are used at each VSC dc-side to provide a stiff dc voltage source. The dc capacitors are grounded at their electrical centre point to establish the earth reference potential for filtering and the transmission system. The VSC is effectively mid-point grounded and DC filters and a zero-sequence blocking inductor are used to mitigate interference on any metallic communication circuits adjacent to the DC cables. There is no earth return operation. The converters are coupled to the ac system through ac phase inductors and power transformers, with harmonic filters located between the phase inductor and the transformer. The AC filters are tuned to multiples of the switching frequency, as shown in figure 19.22. This arrangement minimizes harmonic currents and avoids dc voltage stresses in the transformer, which allows use of a standard AC power transformer for matching the 50/60Hz AC network voltage to the converter AC voltage necessary to produce the desired DC transmission voltage.

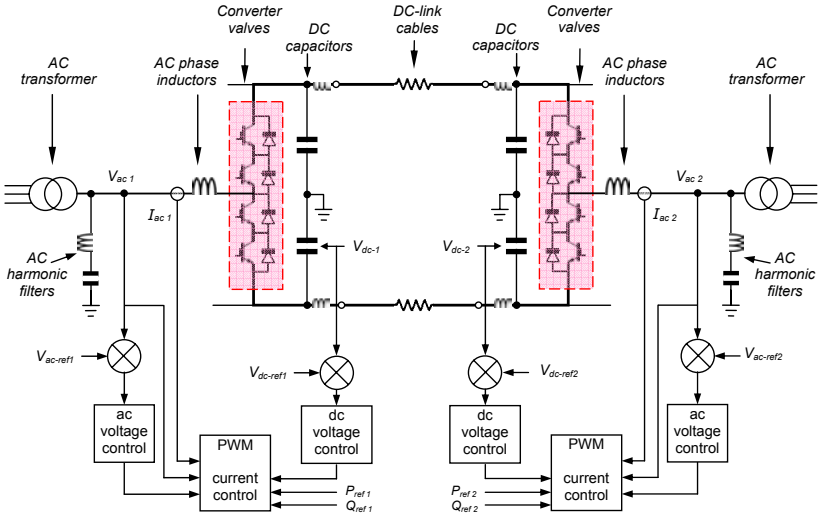


Figure 19.18. *VSC HVDC transmission, using three-level (NPC) voltage source inverters.*

The IGBT valves used in VSC converters are comprised of series-connected IGBT cells. Present technology uses 2.5kV igbt die, with a 4.5kV objectives, parallel connected on a common electrically-conducting substrate in 2500A sub-modules, with 30 series connected sub-modules in a string cell. Strings are then series connected to produce the required link valve voltage requirement. The IGBT switching frequency is limited to about 2 kHz. The valves are cooled with circulating water and water to air heat exchangers.
The structure is constructed to shield electromagnetic interference (EMI) radiation.

19.8.1 VSC-Based HVDC control

Power flow between the VSC and ac network can be controlled by changing the phase angle of the converter ac voltage V_S with respect to the filter bus ac voltage V_T, whereas the reactive power can be controlled by changing the magnitude of the fundamental component of the converter ac voltage V_T with respect to the filter bus ac voltage V_S. By independently controlling these two aspects of the converter voltage, operation in all four quadrants is possible. This means that the converter can be operated in the middle of its reactive power range near unity power factor to maintain dynamic reactive power reserve for contingency voltage support similar to a static VAr compensator. This also means that the real power transfer can be changed rapidly without altering the reactive power exchange with the ac network or waiting for switching of shunt compensation.

Reactive power control can be used for dynamic voltage regulation to support the ac interconnection, by synthesising a balanced set of three phase voltages. Black start (restoring system operation without an external energy source) capability is also a feature.

Independent control of the VSC ac voltage magnitude and phase relative to the system voltage decouples the active and reactive power control loops for HVDC system regulation. The active power control loop can be set to control either the active power (dc-link current) or the dc-side voltage. In a dc link, one station is selected to control the active power while the other controls the dc-side voltage. The reactive power control loop controls either the reactive power or the ac-side voltage. Either of these two modes can be selected independently at either end of the dc link. Figure 19.18 shows the characteristic ac voltage phasors including the controlled variables V_{dc}, I_d, Q, and V_L.

19.8.2 Power control concept

dc-link power
The dc-link power flow concepts are not complicated by ac phasor considerations. No reactive power is involved with dc, only the real power flows. Consider the HVDC configuration depicted in figure 19.19 involving converter #1 and converter #2.

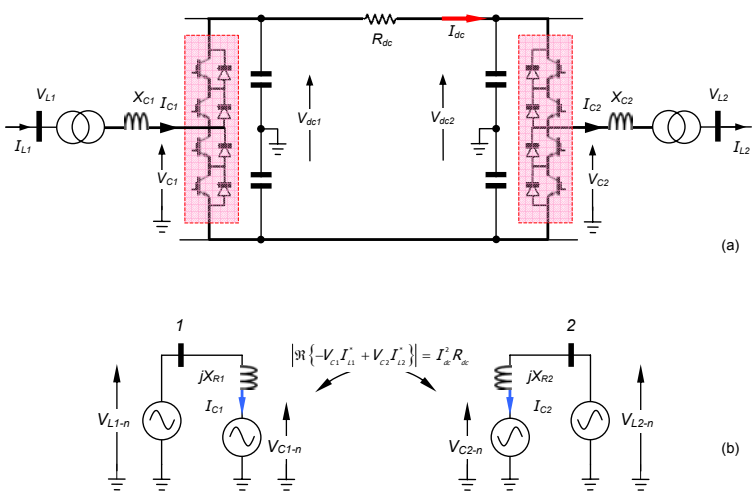


Figure 19.19. *VSC HVDC transmission dc-side, using two-level voltage source inverters.*

If converter #1 produces an ac voltage represented by

$$V_{C1} = |V_{C1}|(\cos\delta_1 + j\cos\delta_1) = |V_{C1}|\angle\delta_1 \tag{19.29}$$

while the other, converter #2, is represented by the voltage source

$$V_{C2} = |V_{C2}|(\cos\delta_2 + j\cos\delta_2) = |V_{C2}|\angle\delta_2 \tag{19.30}$$

Then if the power transmitted equals the power received, then

$$\Re\left\{-V_{C1}I_{L1}^{*}+V_{C2}I_{L2}^{*}\right\} = 0 \tag{19.31}$$

If the dc link resistive losses are incorporated equations (19.31) becomes

$$\left|\Re\left\{-V_{C1}I_{L1}^{*}+V_{C2}I_{L2}^{*}\right\}\right| = I_{dc}^{2}R_{dc} \tag{19.32}$$

ac-side powers
The fundamental base apparent power S_T at the filter bus between the converter reactor and the AC filter is defined as follows (see figure 19.20):

$$S_T = P_T + jQ_T = \sqrt{3}\times V_T \times I_R \tag{19.33}$$

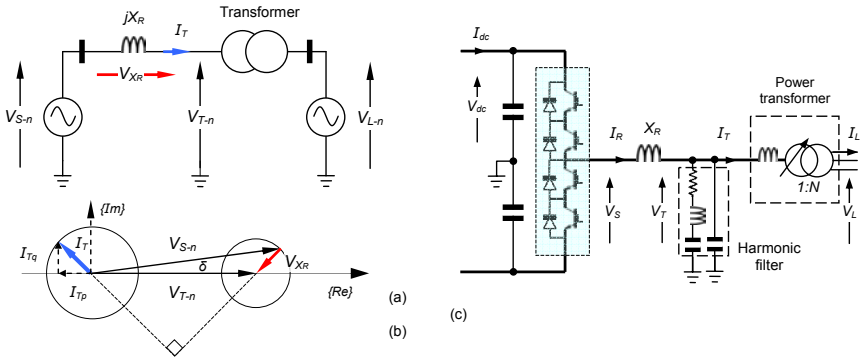


Figure 19.20. *VSC HVDC transmission ac-side.*

The active and reactive power components on the grid-side are defined as (see section 20.3 of ac power transmission):

$$P = \frac{V_T \times V_S \times \sin\delta}{\omega L} = \frac{V_T \times V_S \times \sin\delta}{X_R}$$
$$Q_T = V_T \frac{V_S \times \cos\delta - V_T}{X_R} \qquad (19.34)$$

where: δ = phase angle between the filtered voltage V_T and the converter output voltage V_S
L = inductance of the converter ac line inductance

Changing the phase angle δ controls the active power flow P between the converter and the filter bus and consequently between the converter and the AC network.

As shown in figure 19.21a, for active power flows:

- if the V_S phase-lags V_T, active power P flows from the AC to the DC side (rectifier)
- if the V_S phase-leads V_T, the active power P flows from the DC to the AC side (inverter)

Changing the amplitude difference between the filter voltage V_T, and the converter voltage V_S controls the reactive power flow between the converter and the AC network.

As shown in figure 19.21b, for reactive power flows:

- if $V_T > V_S$, there is reactive power consumed from the ac network
- if $V_S > V_T$, there is reactive power generated into the ac network

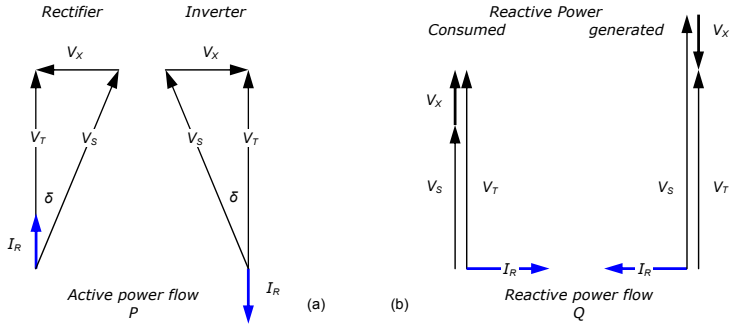


Figure 19.21. *Active and reactive power phasor diagrams.*

With the PWM (Pulse-Width-Modulation, see Section 15.2.3) controlled VSC it is possible to create any phase angle and voltage amplitude (within limits set by the dc-link voltage magnitude) by changing the PWM modulation depth and the relative phase displacement respectively, by using phase-locked-loop grid synchronised displacement. This allows independent control of the active and reactive power.

The typical P-Q diagram, which is valid within the whole steady-state AC network voltage, is shown in the figure 19.22. This figure illustrates the grid real power, P, and reactive power, Q, capability of the HVDC VSC converter terminal, measured at the interconnection point)point of common coupling, PCC), as a function of ac system voltage.

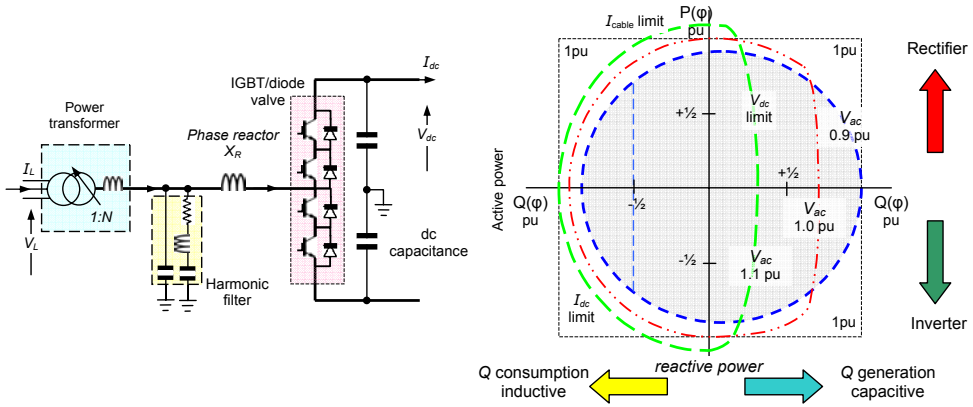


Figure 19.22. *P-Q active and reactive power control locus, showing varying voltage limits.*

The 1st and 2nd quadrants represent rectification and the 3rd and 4th inversion. A positive Q indicates delivery of reactive power to the AC network. Because the dc-link decouples the two converters, reactive power can be controlled independently at each station. There are dc-link voltage (Q generation restrictions) and current (inverter - igbt - power) limitations that have been taken into account in this typical P-Q diagram. Depending on the cable design, the cable dc current maximum may restrict the rectifier power limit. There is also a steady state minimum dc-voltage level limit, which may prevent continuous absorption of large amounts of reactive power.

The capacitive reactive power capability increases with decreasing voltage when it is needed most. Similarly, the inductive reactive power capability increases with increasing network voltage when it is needed most. For a given ac system voltage the converter can be operated at any point within its respective 'circle'. At low ac voltages the VA limit dominates. For high ac voltages, the dc-voltage limit is restrictive but it is not desirable to inject reactive power when ac voltage already is high.

19.9 HVDC Components

i. Power transformer

Because of the use of the converter ac inductors and the use of VSC PWM, the current in the transformer windings contains minimal harmonics and is not exposed to any DC voltage. The transformer is a 50/60Hz single or three phase power transformer, with taps and a tap-changer. The secondary voltage, the filter bus voltage, is controlled by the tap changer to achieve the maximum active and reactive power from the VSC, both consumed and generated. The tap changer is located on the secondary side, which has the largest voltage swing, and also to ensure that the ratio between the line winding and a possible tertiary winding is fixed. This tertiary winding feeds the station auxiliary power system and if delta connected suppresses any core triplen fluxes.
In order to maximize the active power transfer, the converter generates a low frequency zero-sequence voltage (<0.2pu) which is blocked by the ungrounded transformer secondary winding.

ii. Converter line inductors

There is one converter inductor per phase, with EMC shields to eliminate magnetic fields outside the windings. The converter line inductor is a key components in a voltage source converter with which continuous and independent control of active and reactive power is possible.
The main purposes of the converter ac inductors are:

- to provide low-pass filtering of the PWM voltage to give the desired fundamental frequency voltage. The converter generates harmonics related to the switching frequency. The harmonic currents are blocked by the converter inductor and the harmonic content on the AC bus voltage is reduced by an AC shunt filter, which diverts the harmonic currents;

- to provide active and reactive power control. The fundamental frequency voltage across the inductor defines the power flow (both active and reactive) between the AC and DC sides. The P-Q diagram in figure 19.21 shows the active and reactive power definitions;
- to limit line short-circuit currents. The short-circuit voltage of the converter inductor is typically 15%;
- to prevent dc circuit resonance; and
- minimises intermittent dc-link current flow.

The stray capacitance across the line inductor is minimised in order to minimize the harmonics coupled into the ac filter side of the inductor. The high *dv/dt* on the bridge terminals at switching results in current pulses (*i=C dv/dt*) through all stray capacitances to ground. As these currents pass through the valve, and should be minimized. The ac filter side of the inductor is effectively at ground at high frequencies and the capacitance across the inductor should therefore be low. To achieve low capacitance the converter inductors have air coils rather than magnetic cores.

iii. DC-Capacitors

The primary objective of the valve DC-link side capacitor is:

- to provide a low-inductance path for switch turn-off current;
- act as a temporary energy store; and
- to reduce the harmonic ripple on the dc-link voltage. Disturbances in the system, such as AC faults, cause DC-link voltage variations.

The high-voltage DC capacitor uses a dry, self-healing, metallised film design, as opposed to oil filled technologies. The dry capacitor design offers, long life, high capacity and low inductance, in a non-corrosion, non-radiating plastic housing.

iv. AC-filters

Two basic shunting filter characteristics are applicable to HVDC, namely high Q tuned filters (band pass) for filtering (shunting) of a specific harmonic and low Q damping filters (high pass) for attenuation (shunting) of more than one high order harmonic..

In a typical HVDC scheme, AC filters contain two or three grounded and/or ungrounded tuned filter branches. A typical second order filter and its frequency characteristics are shown in figure 19.23.
AC filters for VSC HVDC converters have lower ratings than those for conventional HVDC converters and are not required for reactive power compensation. These filters are permanently connected to the converter bus and not switched with transmission loading, as in conventional HVDC.

Voltage source converters can be operated with different control schemes, most of which use pulse width modulation to control the ratios (magnitude and phase) between DC and AC side fundamental frequency voltages. At the AC side converter terminal, the voltage to ground is not sinusoidal. The most frequent application of voltage source converters is as a machine drive (in industrial applications) where this is of less concern. However, connecting a voltage source converter to a transmission or distribution system requires the voltage to be sinusoidal. This necessary filtering is achieved by means of the converter inductor and AC filters.

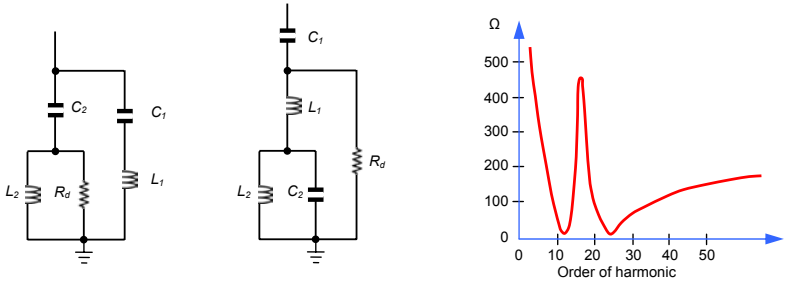


Figure 19.23. *Single phase equivalent circuit diagram and harmonic impedance characteristic of a double tuned filter.*

The distorted waveform of the converter terminal voltage can be described as a series of harmonic voltages

$$V_s = \sum_{h=1} V_h \cos(h\omega_o t + \alpha_h)$$

where V_h is the h^{th} harmonic voltage.

The magnitude of the harmonic voltages vary with the DC voltage, the switching frequency (or pulse number) of the converter and converter PWM technique.
Harmonic cancellation PWM or optimal PWM utilizes a sinusoidal PWM with 3rd harmonic (triplen) injection. A 3rd harmonic is added to the fundamental frequency to increase the voltage, hence power rating of the converter, as considered in chapter 15.1.3vii.

Example 19.3: ***HVDC transmission with voltage source controlled dc-link***

The VSC dc-voltage transmission line represented by figure 19.23 connects a 130kV ac rms, 50Hz three-phase system to a 120kV, 60Hz three-phase system, some 100km apart. The voltage-controlled converter at each nominal ±80kV transmission line end are interface by a Δ-Y transformer with 25mH of line and leakage reactance referred to the grid side, and with a turns ratio to match the converter voltage requirements for the ±80kV dc link. The cable is rated at 625A with 300mm^2 of copper giving a total line resistance is 2Ω.

The 50Hz load end grid draws a total of 100MVA at a 0.75 power factor, while source end VSC draws the power requirement from the 60Hz network at unit power factor.

Determine the phasor diagram for:

i. the 50Hz receiving end
ii. the 60Hz transmitting end.

Solution

i. The total active 50Hz power at the load end is

$$P_{50Hz} = S_{50Hz} \times pf_{50Hz}$$
$$= 100\text{MVA} \times 0.75 = 75\text{MW}$$

The 50Hz reactive power flow into the dc link is

$$Q = \sqrt{VAr^2 - P^2}$$
$$= \sqrt{100^2 - 75^2} = 66.1\text{MVAr}$$

The 50Hz ac line current is

$$I_{L50Hz} = \frac{S_{50Hz}}{\sqrt{3} \times V_{L50Hz}}$$
$$= \frac{100\text{MVA}}{\sqrt{3} \times 130\text{kV}} = 441\text{A}$$

The necessary phasor diagram is referenced with respect to neutral.

The reference 50Hz phase voltage is

$$V_{L-N_{50Hz}} = \frac{V_{L50Hz}}{\sqrt{3}}$$
$$= \frac{130\text{kV}}{\sqrt{3}} = 75.06\text{kV} \angle 0°$$

The angle between the line current and the phase voltage is

$$\theta = \cos^{-1} 0.75 = 41.4°$$

The line reactance at the 50Hz end is

$$X_{L50Hz} = 2\pi f \times L$$
$$= 2\pi \times 50\text{Hz} \times 25\text{mH} = 7.85\Omega$$

The 50 Hz converter line to neutral voltage (and load angle) is

$$V_{L-N\,conv50Hz} = V_{L-N50Hz} + jX_L I_L$$
$$= 75\text{kV} + j7.85\Omega \times 441\text{A} \angle -41.4°$$
$$= 75\text{kV} + 3.45\angle 48.6° = 77.3\text{kV} + \text{j}2.59$$
$$= 77.34\text{kV} \angle 1.92°$$

The line-to-line voltage at the 50Hz VSC converter is

$$V_L = \sqrt{3}V_{L-N}$$
$$= \sqrt{3} \times 77.34\text{kV} = 134\text{kV}$$

ii. The ±80kV dc-link has a pole-to-pole voltage of 160kV. From $P_l = V_{dl} \times I_d$, the link current is

$$I_d = \frac{75\text{MW}}{160\text{kV}} = 469.75\text{A}$$

The cable voltage drop is

$$V_{\Delta dc} = I_d \times R_{dc}$$
$$= 468.25\text{A} \times 2\Omega = 0.9375\text{kV}$$

The VSC converter dc voltage at the 60Hz transmitting end is 160kV + 0.938kV = 160.938kV such the pole voltages are ±80.469kV. These results are shown in figure 19.24.

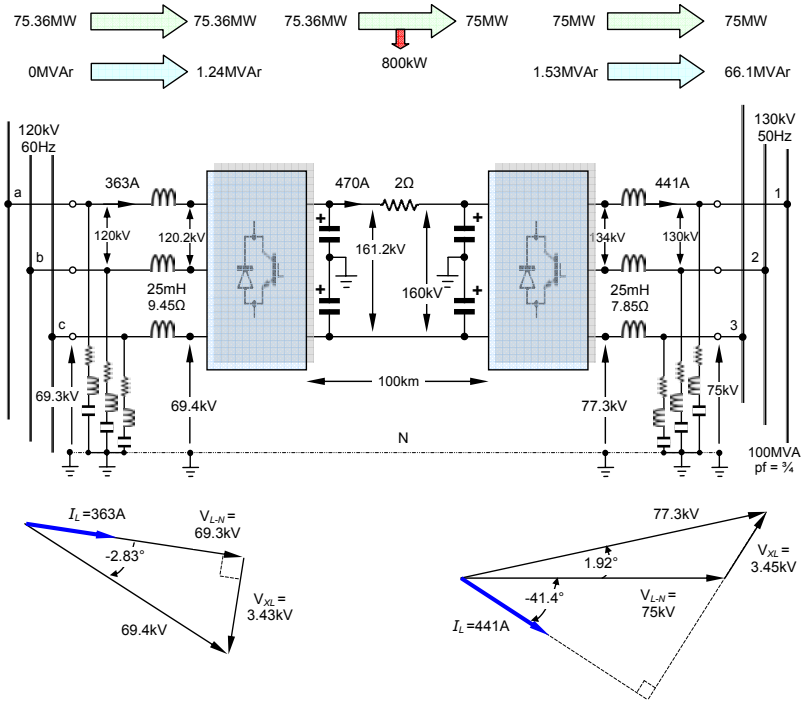


Figure 19.24. *HVDC VSC Example 19.3.*

The VSC power delivered into the link is

$$P_{dc60\text{Hz}} = I_d V_{dc60\text{Hz}}$$
$$= 468\text{A} \times 2 \times 80.47\text{kV} = 75.36\text{MW}$$

With unity power at the 60Hz sending end $P = S$, the line current is

$$I_{L60Hz} = \frac{S_{60\text{Hz}}}{\sqrt{3}V_L} = \frac{P_{60\text{Hz}}}{\sqrt{3}V_L}$$
$$= \frac{75.36\text{MW}}{\sqrt{3} \times 120\text{kV}} = 362.6\text{A}$$

For the 60Hz transmission end phase or diagram, the line to neutral voltage is required from the 120kV line voltage at the 60Hz end, thus

$$V_{L-N\ 60\text{Hz}} = \frac{V_{L60Hz}}{\sqrt{3}}$$
$$= \frac{120\text{kV}}{\sqrt{3}} = 69.3\text{kV}$$

The 60Hz line reactance is

$$X_{L60\text{Hz}} = 2\pi f \times L_{60\text{Hz}}$$
$$= 2\pi \times 60\text{Hz} \times 25\text{mH} = 9.45\Omega$$

The VSC converter side-line to neutral voltage is therefore

$$V_{L-Nconv\,60\text{Hz}} = V_{L-N\,60\text{Hz}} - jX_{L60\text{Hz}}I_{L60\text{Hz}}$$
$$= 69.3kV - j9.45\Omega \times 362.6\text{A}\angle 0°$$
$$= 69.3kV + 3.426kV\angle -90°$$
$$= 69.385\text{kV}\angle -2.83°$$

The line voltage at the sending converter is

$$V_{Lconv\,60\text{Hz}} = \sqrt{3}V_{L-Nconv\,60\text{Hz}}$$
$$= \sqrt{3} \times 69.385\text{kV} = 120.18\text{kV}$$

♣

19.10 Twelve-pulse transformer based NPC HVDC

Figure 19.25 show a HVDC configuration that takes advantage of a star-delta, phase-shifting, transformer secondary to halve the series IGBT connection problems associate with high-voltage applications. The twelve-pulse transformer arrangement also reduces the 5th and 7th ac harmonics due to the cancellation effect because of the 30° phase shift between the two secondary windings. These advantages are traded against the complexity associated with an extra high-voltage transformer winding. A VSC variation is to use multilevel configurations involving chained cells, called a capacitor clamped multilevel M2C converter. The cell comprise is a capacitor of large capacitance, which is switched in and out of the series string circuit, as introduced in chapter 15.3.4 and considered in 19.11.

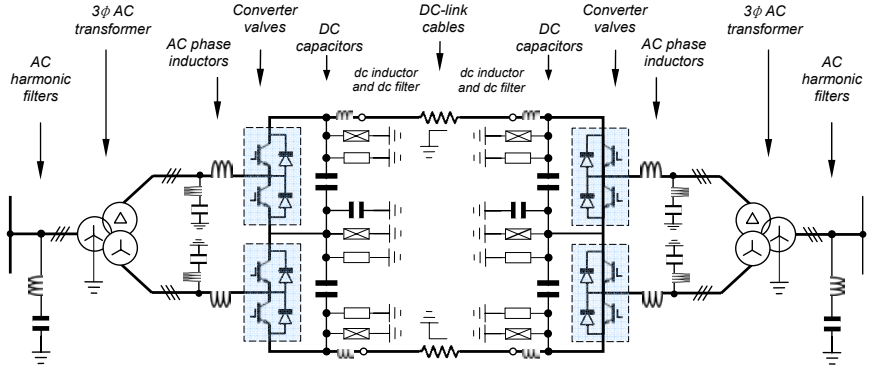


Figure 19.25. *HVDC NPC VSC using twelve-pulse transformer arrangement.*

19.11 VSC-HVDC transmission systems based on the modular multilevel converter, M2C

The M2C approach exploits the potential of a multilevel structure and pulse width modulation. The filtering requirements are reduced due to generation of high quality ac voltage (small filters are required). The use of a large number of levels with small voltage steps, results in low *dv/dt* and reduced voltage stress on the insulation of the interfacing transformers. This allows the use of standard 50/60Hz transformers without need to withstand dc link voltage or harmonic currents. The effective switching frequency per device is low, which reduces the switching losses and overall conversion losses, and

does not produce significant high frequency noise. Fig. 19.26 shows one-phase of a 7-level modular converter, which relies on the cell capacitors to create a multilevel voltage waveform at the converter terminal. As the number of levels increases, it can generate high voltage with low harmonic content, using medium voltage devices (2.5kV or 4.5kV). DC link capacitors are not required, which significantly reduces the space requirement for the converter station. As the converter depends on phase voltage redundancy to maintain approximately constant voltage across the cell capacitors, the modular multilevel converter performs better than the NPC converter during unbalanced operation, and symmetrical and asymmetrical faults, without increasing the risk of device failure or system collapse. The ability of the modular converter to ride through different types of ac faults makes it attractive in power system applications where restrictive grid codes must be met. The absence of the dc link capacitors in VSC-HVDC transmission system based on the modular converter, make sizing the cell capacitors critical. They are sized to be able to store enough energy to support the converter dc link during transient events, otherwise the system may fail to meet transient ride-through requirements. The first commercial modular multilevel converter based HVDC transmission system project is the Trans Bay cable project in USA, rated at 400MW active power transfer and ±170MVAr STATCOM functionality with a bipolar dc link voltage of ±200kV. The line is 85km of submarine cable.

For this type of multi-level converter, the cell capacitors experience the full load current, unlike the rail capacitor of a two level system. High capacitance and large physical size result. This capacitance is the dominant factor in the size of this type of converter. But the main dc link capacitors in both ends of the line are eliminated. There is dc current component in the leg current and no dc link fault protection is offered.

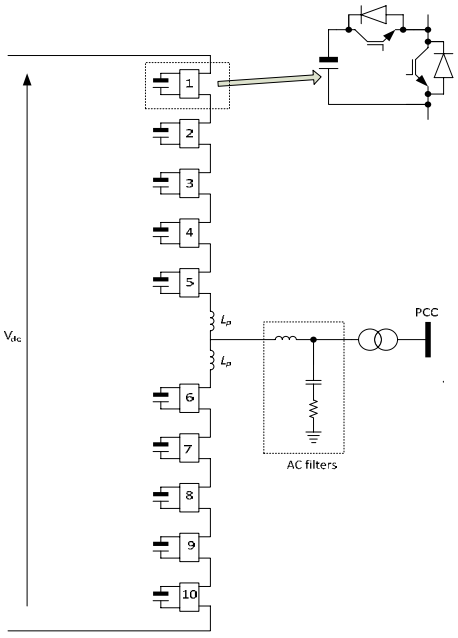


Figure 19.26: *One-phase of 7-level modular converter used as basic HVDC building block.*

Table 6 provides a comparison between high-voltage DC transmission system technologies. The comparison focuses on issues such as: control flexibility, fault ride-through capability, conversion losses, electromagnetic compatibility (EMC) issues, and provision of auxiliary functionality such as voltage, frequency, and damping support.

Table 1: Comparison between different HVDC technologies

	Current source converter based		**Voltage source converter based**		
	LCC	CCC	Two-level	Neutral-point clamped	Modular (M2C)
Switching device	Thyristor	Thyristor	IGBT	IGBT	IGBT
switching losses	negligible	negligible	high	moderate	low
On-state losses	low	low	moderate	moderate	moderate
Station size	large	Reduced due elimination of switch capacitors and their circuit breakers	Significantly reduced (30% to 50% of LCC)	Significantly reduced (30% to 50% of LCC)	Significantly reduced (30% to 50% of LCC)
Active power control	Discontinuous from ±10% to ±100%	Discontinuous from ±10% to ±100%	Continuous From 0 to ±100%	Continuous From 0 to ±100%	Continuous From 0 to ±100%
Active power reversal	DC voltage polarity must be changed and not instantaneous	DC voltage polarity must be changed and not instantaneous	Instantaneous and no change of DC voltage polarity	Instantaneous and no change of DC voltage polarity	Instantaneous and no change of DC voltage polarity
Independent control of active and reactive power	No	No	Yes	Yes	Yes
Reactive power demand	50% to 60%	50% to 60%	No	No	No
Reactive power capability	Limited (lagging VAr only) and discontinuous using switch shunt capacitors for leading VAr	Limited (lagging VAr only)	Continuous and inherent within the converter control at no additional cost	Continuous and inherent within the converter control at no additional cost	Continuous and inherent within the converter control at no additional cost
Power levels	Up to 6400MW	Up to 6400MW	Up to 1200MW	Up to 1200MW	Up to 1200MW
controllability	low	low	high	high	high
AC filters	Large	Large	small	Smaller than 2-level converter	no
DC filter	Yes	Yes	No	No	No
Converter transformer	Expensive with high insulation requirement to withstand voltage stresses during power reversal	Expensive with high insulation requirement to withstand voltage stresses during power reversal, but with reduced MVA rating	Expensive with high insulation requirement to withstand switching of large voltage steps with high frequency	Expensive with high insulation requirement to withstand switching of large voltage steps with high frequency	Cheap with standard insulation
DC cable	Expensive with high insulation requirement to withstand voltage stresses during power reversal	Expensive with high insulation requirement to withstand voltage stresses during power reversal	Cheap and light weight extruded cable	Cheap and light weight extruded cable	Cheap and light weight extruded cable
Commutation failure	Due voltage distortion and lack or reactive power during AC fault	Significantly reduced	no	no	no
Applications	Connection of strong systems only, connection of weak system is possible but at additional cost by using STATCOM or synchronous condenser	Connection of strong and weak systems with SCR>=1	Independent of systems strength and network without generation	Independent of systems strength and network without generation	Independent of systems strength and network without generation
AC fault ride-through capability	Possible with high risk of commutation failure	Possible with reduced risk of commutation failure	is excellent	Very good, but its ability to cope with asymmetrical faults depends on capacitor voltage balancing strategy used	is excellent
DC fault ride-through capability	Possible with inherent inductance in the DC side	Possible with inherent inductance in the DC side	Possible with increasing the interfacing reactor>0.25pu	Possible with increasing the interfacing reactor>0.25pu	Possible with combinations of inherent inductances within each arm and interfacing reactors

Multi-terminal configuration	is limited to 3 due to increase complexity of the control system to achieve current balancing and power reversal	is limited to 3 due to increase complexity of the control system to achieve current balancing and power reversal	is extendable to any number of terminal practically feasible	is extendable to any number of terminal practically feasible	is extendable to any number of terminal practically feasible
Delivery time	36 month	36 month	24 month	24 month	Not yet known
Redundancy	yes	yes	yes	yes	yes
Manufacturers	ABB, SIEMENS and AREVA	ABB	ABB	ABB	SIEMENS

19.12 HVDC VSC Features

IGBT based systems used in transmission are based around the voltage source inverter (VSI) principle; high frequency switching allows converter synthesised controlled voltage at its output. This voltage appears as a power frequency fundamental with harmonics at the switching frequency. With appropriate control, the voltage source inverter may appear as a controlled current source.

The attributes of HVDC voltage source converters allow for simpler ac system integration, plus the following system technological features.

- Independent, continuous control of active and reactive power at each terminal, that is, four-quadrant operational control, down to low power levels.
- Steady-state reactive power capability offers voltage control for weak ac grids.
- Independent control of reactive power at each terminal while maintaining full dc voltage for efficient transmission operation.
- Dynamic reactive power reserve capability from the voltage source converters for contingency voltage support of the interconnected ac system. The VSC can be connected to blacked-out networks and re-energize them.
- Less filtering requirements, about 15 to 20% of rated power, due to minimal injection of low frequency harmonics. This results in a reduced system installation size.
- No requirement for switched filters or shunt capacitor banks for reactive power compensation with changes in power transfer.
- No inherent fault current contribution to increase circuit breaker interrupting duty. Fault current contribution is naturally limited to maximum load current but can be reduced during faults by fast acting VSC control.
- Robust with respect to ac network faults, thereby allowing continuity of power transmission and limitation of spread of system disturbances.
- VSC HVDC is short-circuit proof for line-to-line-to-ground and line-to-line faults on the dc-side.
- Can operate in ac grids with extremely low short-circuit levels or with passive loads. Can operate in an unsymmetrical network (e.g. during ac network faults) and provide unbalance control to compensate asymmetrical loads. The faster converter response allows counteraction of network distortion and transients.

Disadvantages

- Improved control is achieved at the expense of increased losses in the power converter. Increased losses are the result of:
  i. A higher frequency switching leads to increased switching loss.
  ii. IGBT devices exhibit significantly higher on-state voltage drop compared to thyristors with similar voltage ratings. For a given application, this leads to increased conduction loss.
- IGBT modules have lower power capability than available thyristor packages, leading to increased power component count.
- IGBT devices have lower current overload capability than thyristor based systems.
- High *dv/dt* transients may be present at the output.

The progression and expansion to multi-terminal HVDC systems is hampered by the fact that VSC technology cannot inherently block the ac side from the effects of dc-side faults. This uncontrolled ac to dc rectification limitation necessitates the use of dc circuit breakers, which having a high dc current and voltage requirement, are technologically challenging.

19.13 Features of conventional HVDC and HVAC transmission

The following are comparison features between ac and conventional dc electrical power transmission:

- Increased power system stability since dc power flow is controlled by converter delay angles. Converter response times are of the order of ms, while the dc link-time constant is significantly longer. Thus, the dc-link short circuit current can be limited.
- The fast converter response times means power reversal can be achieved in ms, much faster than within ac systems.
- Steady-state power flow is related to dc-link resistance, as opposed to ac-line reactance.
- Transmission line inductance has zero impedance to dc, whereas inductive reactance is relatively large in ac systems. A minimal ac skin effect occurs with ac transmission.
- AC power is lost due to dielectric losses. Capacitance between conductors is open circuit to dc, but in ac systems capacitive reactance current paths exist which increase I^2R losses
- Under sea cables have high capacitance which has minimal effect on dc transmission
- DC back-to-back converters (with minimal link inductance, tens of milliHenry's) allow synchronisation between 50Hz and 60Hz systems or same frequency systems at different voltage phase angles
- DC transmission line and its towers are cheaper per unit length than for ac, but dc terminating stations are more complicated and expensive than ac terminating stations
- DC converters have limited overload capability and are less reliable because of the ancillaries (filters, cooling management, etc.)
- DC transmission can have a lower visual impact, plus a narrower corridor, hence lower environmental impact than ac systems
- Electric and magnetic fields for dc transmission have lower environmental implication than ac fields
- Corona effects tend to be less significant with dc that for ac conductors
- DC transmission is more robust to lightning effects, since more effective surge protection is used.
- Polymer cables age slower, giving a longer lifetime, with dc
- Maximum voltage gives lower I^2R losses for a given transmitted power level
- No unnecessary energy transfer since no reactive VAr ($S=VI^*=P+jQ$), with dc

The general advantages of ac transmission, over dc transmission, are

- No costs associated with ac-dc-ac conversion equipment
- Transformer (and autotransformer) voltage matching
- Reactive power and harmonics readily compensated
- Not restricted to only point-to-point connection, as is HVDC (there is no fully functioning exception)
- Established system control methods
- No ac transformer dc voltage stressing due to asymmetrical phase control alignment, and no I^2R and core losses due to high harmonic currents
- ac switch gear and breakers, (and particularly vacuum circuit breakers up to 33kV) are very effective - compared with the difficulties in breaking dc current
- Lower current harmonics

Reading list

Mohan, N., *Power Electronics*, 3rd Edition, Wiley International, 2003.

Acha, E., *et al*., *Power Electronic Control in Electrical Systems*, Newes, 2002.

HVDC Connecting to the future, Alstom Grid, 2010

Problems

19.1 Show that if a three-phase ac transmission system is converted to a tripole hvdc system with the third conductor transmitting a square-wave current of ±1 pu, that the other two phases can alternately conduct $\frac{1}{2}\left(\sqrt{3}+1\right)$ and $\frac{1}{2}\left(\sqrt{3}-1\right)$, yet not exceed their thermal rating.